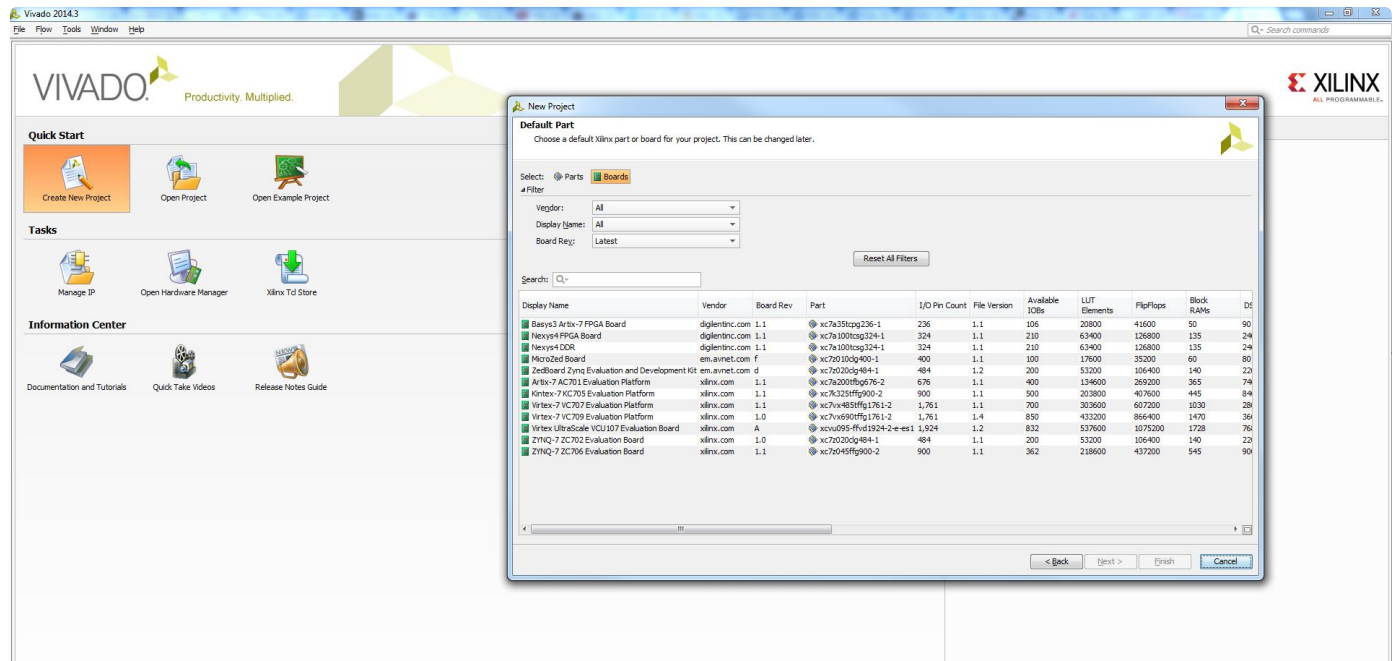


Vivado Version 2015.1 and Later Board File Installation (Legacy)

Board Files:  Download (<https://github.com/Digilent/vivado-boards/archive/master.zip>)

Description

This guide will help you obtain Vivado Board Files for the Nexys 4, Nexys 4 DDR, Basys 3, Arty, Nexys Video, Zedboard and Zybo FPGA Boards.



(https://reference.digilentinc.com/_detail/vivado/vivado_board_files_3.jpg?id=reference%3Asoftware%3Avivado%3Aboard-files)

What you need before proceeding with this guide

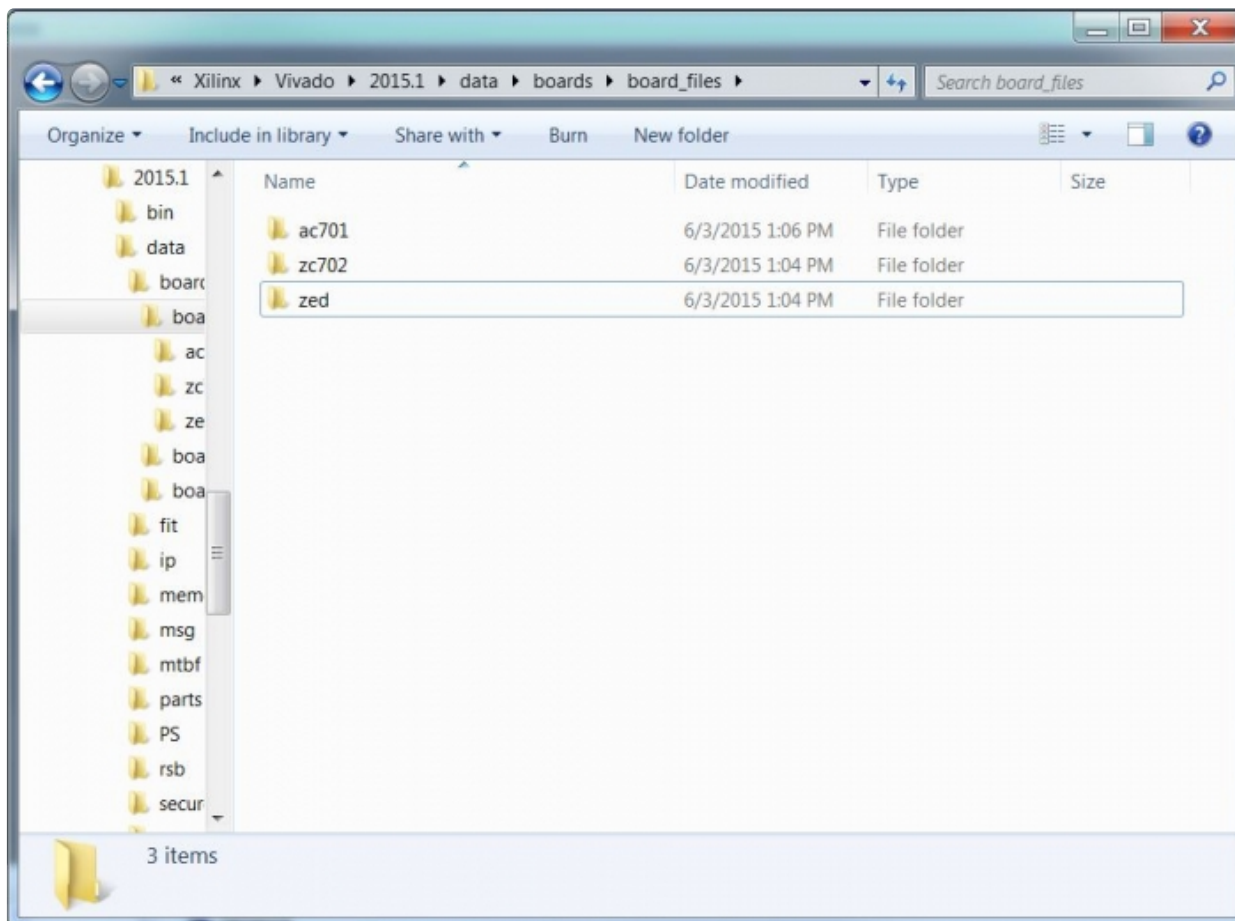
- Xilinx Vivado 2015.1 or later.

Follow this Wiki guide on how to install and activate Vivado on your PC. [Installing Vivado](https://reference.digilentinc.com/vivado/installation)
(<https://reference.digilentinc.com/vivado/installation>)

What are Board Files and why do you need them

After installing Vivado, the default installation directory on your drive will contain a folder called **board_files**. If Vivado is installed in the C drive (usually recommended), then the **board_files** folder can be found here: **C:\Xilinx\Vivado\2015.1\data\boards**.

By default this folder contains XML files for different FPGA boards manufactured by Xilinx.



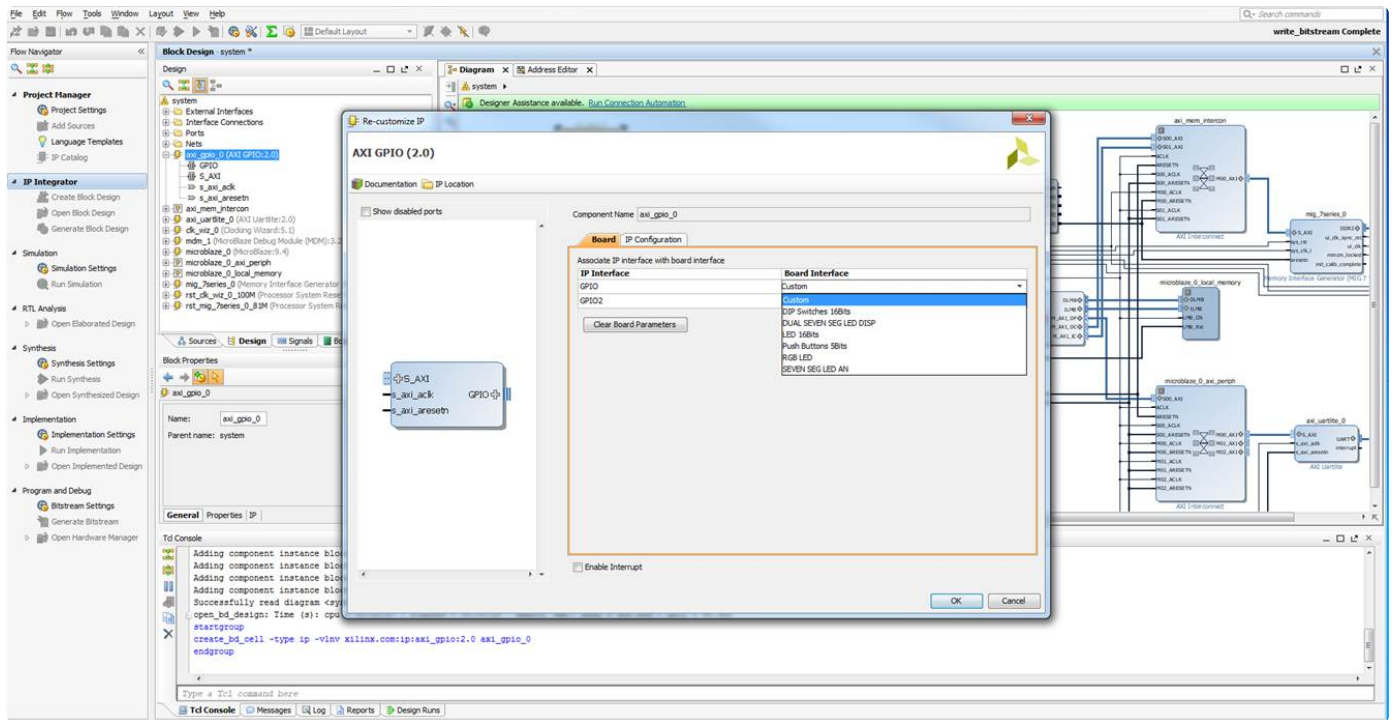
(https://reference.digilentinc.com/_detail/vivado/boardfiles2.jpg?id=reference%3Asoftware%3Avivado%3Aboard-files)

XML files define different interfaces on the board. Interfaces such as Slide Switches, Push Buttons, LEDs, USB-UART, DDR Memory, Ethernet etc.

Digilent has created XML files for the Artix 7 FPGA boards:

- Basys 3
- Nexys 4
- Nexys 4 DDR
- Arty
- Nexys Video
- Zybo
- Zedboard

In the AXI GPIO_0 IP customization window, you will be able to assign different interfaces that are available on your selected board to a specific GPIO_0 IP block.



(https://reference.digilentinc.com/_detail/vivado/vivado_bsp_files_6.jpg?id=reference%3Asoftware%3Avivado%3Aboard-files)

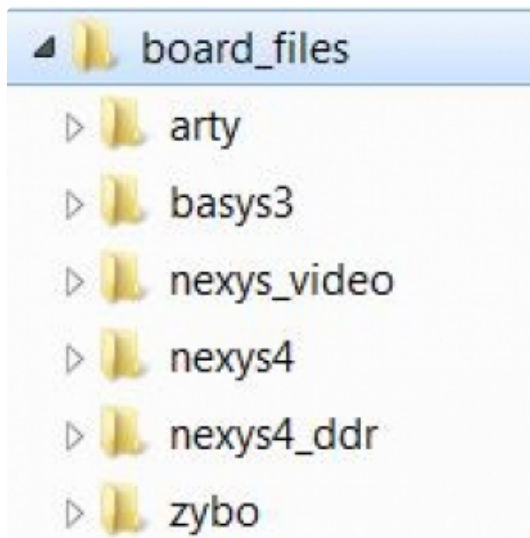
Installation

Download and extract this Zip file: <https://github.com/Digilent/vivado-boards/archive/master.zip>

(<https://github.com/Digilent/vivado-boards/archive/master.zip>)

You can also check out the repository for the board files on github located [here](https://github.com/Digilent/vivado-boards/) (<https://github.com/Digilent/vivado-boards/>)

This zip file will contain a folder called *new/board_files*. Save this in your user documents folder. We will copy this *board_files* folder, navigate to the **board_files** folder inside the Vivado Installation directory, and merge them both.



(https://reference.digilentinc.com/_detail/vivado/boardfiles1.jpg?id=reference%3Asoftware%3Avivado%3Aboard-files)

([id=reference%3Asoftware%3Avivado%3Aboard-files](https://reference.digilentinc.com/_detail/vivado/boardfiles1.jpg?id=reference%3Asoftware%3Avivado%3Aboard-files))

- Copy the contents of the *board_files* folder
- Navigate to the **board_files** folder in the Vivado Installation directory (C:\Xilinx\Vivado\2015.1\data\boards\board_files)
- Paste the contents into the board_files folder
- Restart Vivado

The newly added files will each contain a sub-folder for the current board revision. This sub-folder contains the respective XML files for each FPGA board.

The sub-folder for the **nexys4_ddr** will contain an additional file called **mig.prj** which is the Xilinx Memory Interface Generator description file for customizing the DDR2 component on the **Nexys 4 DDR**.

You are now ready to start a new IP Integrator based Vivado project for the Digilent Nexys 4, Nexys 4 DDR, Zybo, Zedboard and Basys 3 FPGA Boards.

When using the Zedboard make sure to select the board file made by Digilent.

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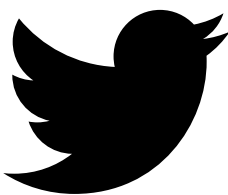
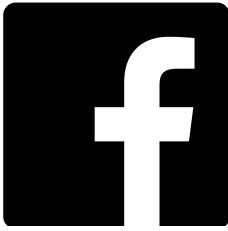

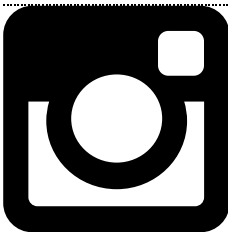
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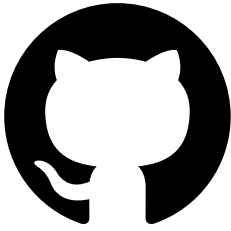
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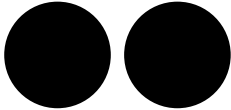
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