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VLSI: D FF using Pass Gate

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Case output resistance of 20 K for the worst-case input pattern.

1. Find out the optimized Boolean equation (If not given).
2. Draw the optimized gate level circuit diagram.
3. Draw the transistor level schematic for CMOS/MOS implementation.
4. Draw stick diagram for above implementation level using proper color code
5. State The various level of VOL corresponding to various transistor statuses
6. Find an equivalent CMOS inverter circuit.
7. For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?
8. For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?
9. Prepare the layout using Microwind tool.
10. Simulate it for various combinations of inputs.
11. Measure the rise time, fall time, propagation delay and other parameters.

ABSTRACT:

A clocked flip-flop with two stable states is known as a D-type flip-flop. When operating, a D-type flip-flop delays the input by one clock cycle. In this Special Assignment D Flip-flop using pass transistor is performed.

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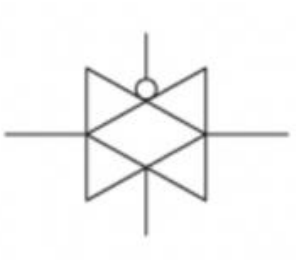
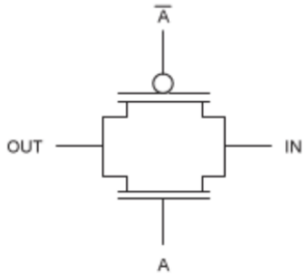
INTRODUCTION: A two-input flip-flop is the D flip-flop. The inputs consist of a clock (CLK) input and a data (D) input. The apparatus produces a timed pulse known as a clock to regulate processes. The D flip-flop is used to hold data until it is required by storing it at a specified time. This device is occasionally referred to as a delay flip-flop. The data input is therefore delayed by up to one clock pulse before it.

Transmission Gate: A transmission gate, or analog switch, is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch consists of a pMOS transistor and nMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off. Transmission gates must always be used in pairs.



a) Representation of a transmission gate



b) Circuit Symbol of Transmission gate

Optimized Boolean equation:

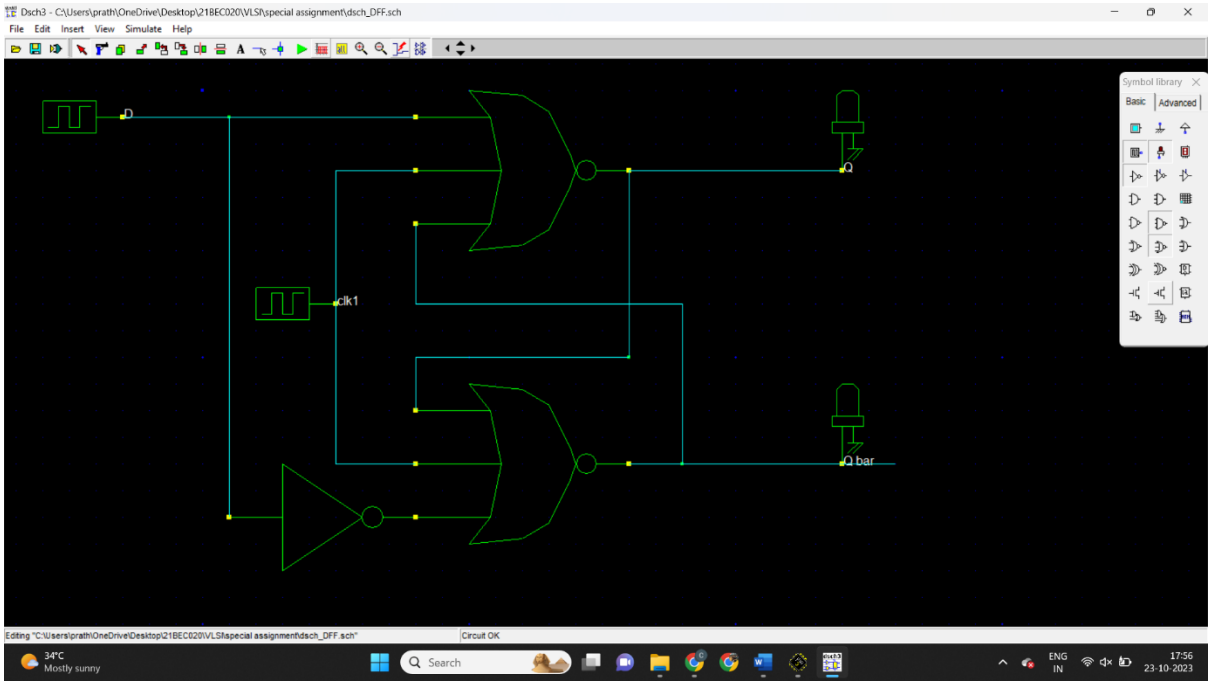
Clock	D	Q	Q’
0	0	No Change	No change
0	1	No Change	No change
1	0	0	1
1	1	1	0

The Boolean expression of the D flip-flop is:

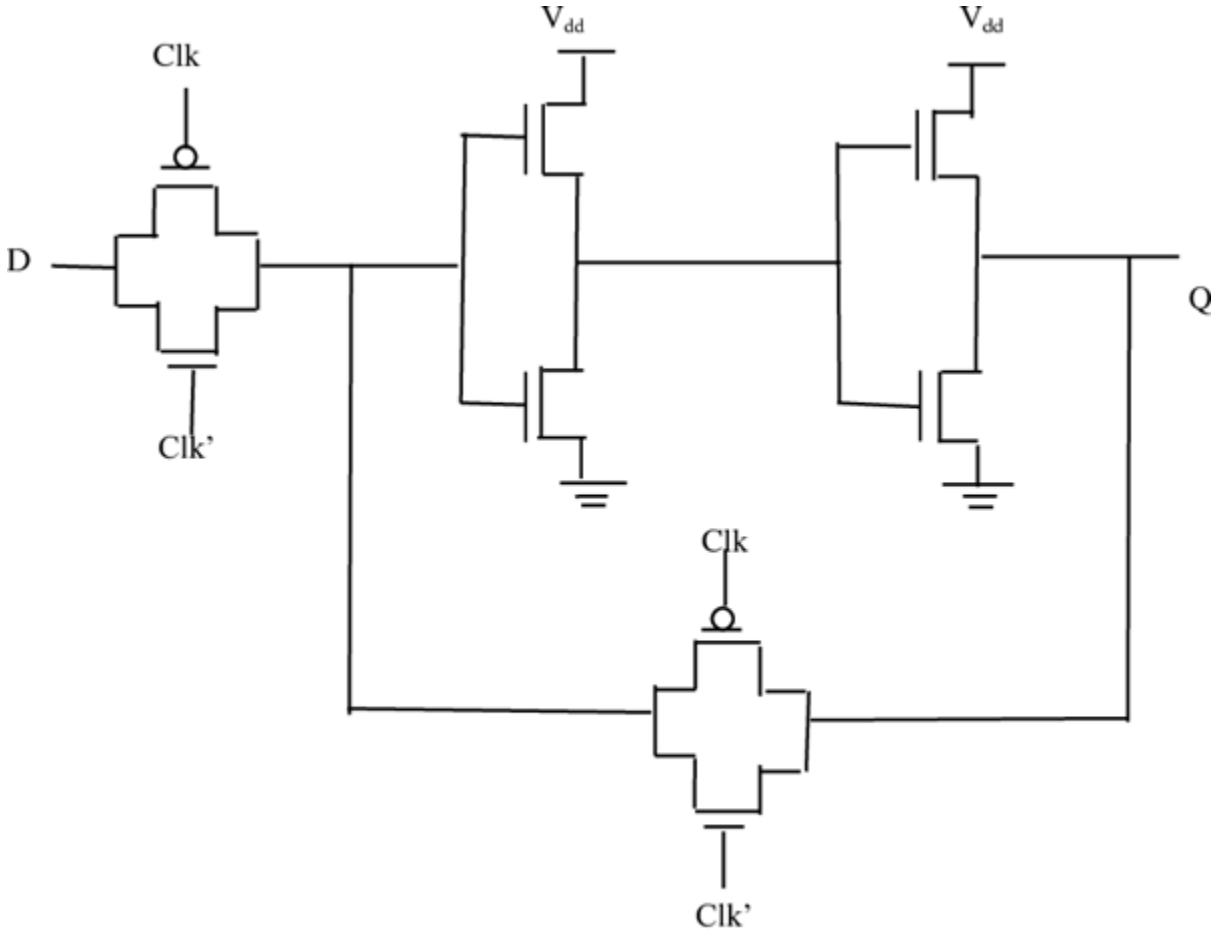
$$Q = Clk.D + \overline{Q_{n-1}}$$

$$\overline{Q_n} = \overline{Clk.D} + Q_{n-1}$$

2. Optimized gate level circuit diagram:



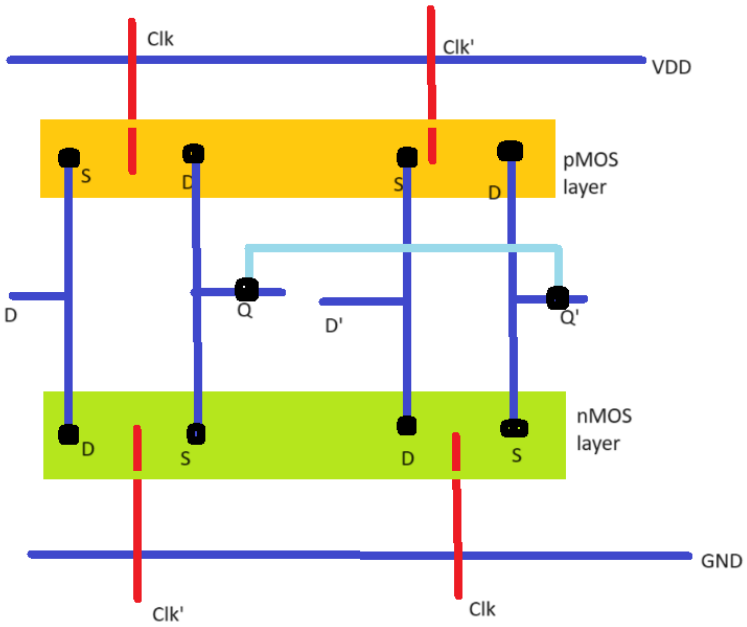
3. The transistor level schematic for CMOS/MOS implementation.



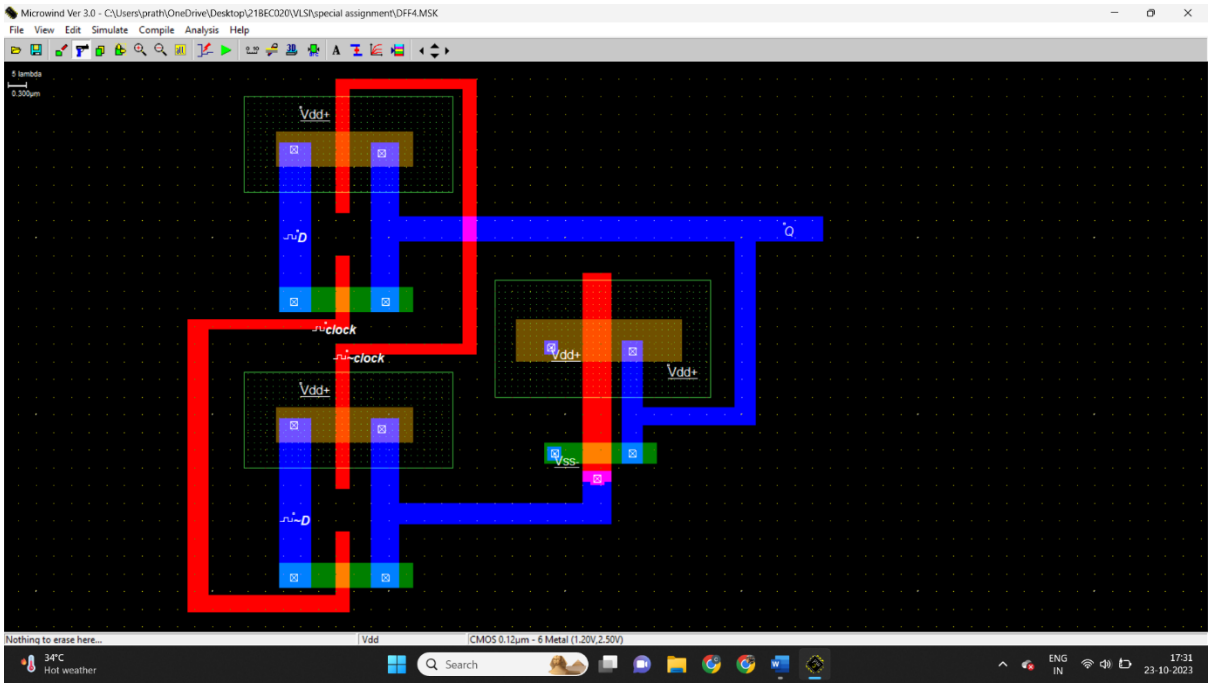
D Flip flop using Transmission Gate

4. Stick diagram for above implementation level using proper color

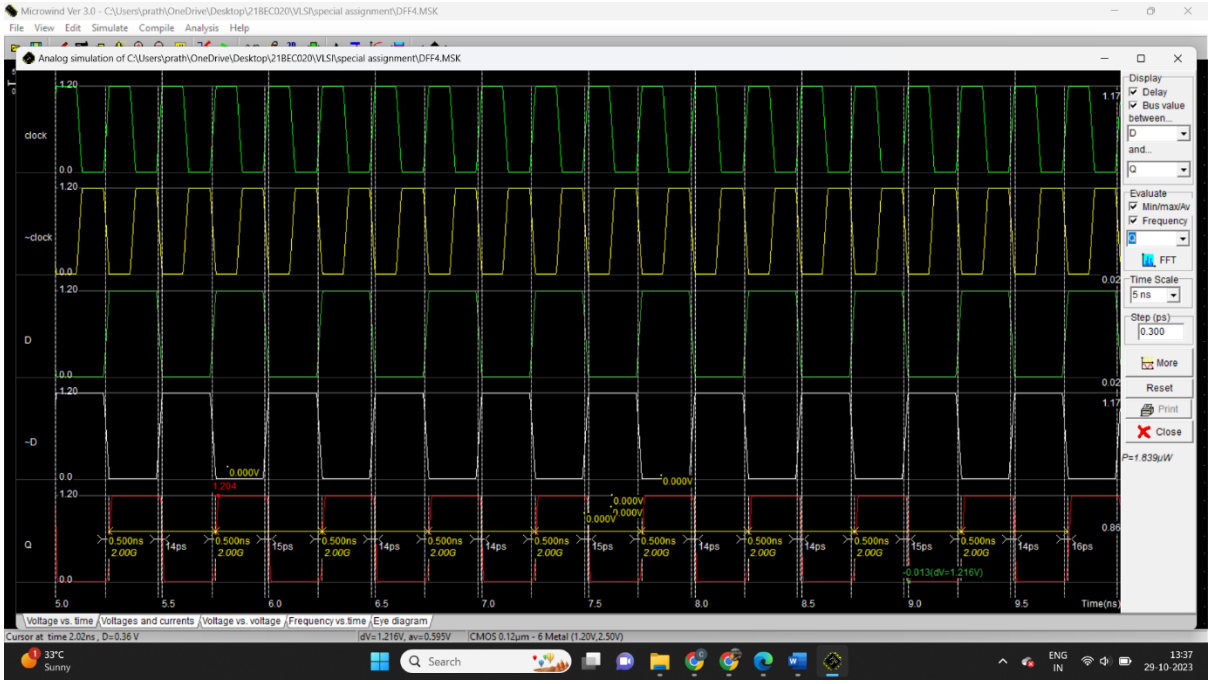
Code:



9. The layout using Microwind tool:



Output: Level Trigger



11. Measure the rise time, fall time, propagation delay and other parameters.

tpLH = 0.500 ps

tpHL=15 ps

Formulae for the Propagation delay is (tpLH+tpHL)/2.

So now putting the values in the above equation, we get Propagation Delay

= (0.500 + 15)/2 ps

= 7.75 ps

Applications of D Flip-Flop:

D flip-flops (Data or Delay flip-flops) are widely used in digital electronic circuits for a variety of applications. They are essential building blocks in sequential logic circuits. Here are some common applications of D flip-flops:

1. Data storage and latching.

2. Clock division and synchronization.

3. Frequency and phase detection.

4. Edge detection.

5. Memory elements.

6. State machines.

7. Serial-to-parallel conversion.

8. Registers.

9. Shift registers.

10. Digital clocks and timers.

11. Control logic.

They play a crucial role in sequential logic circuits and digital systems.