



## Prabath Wijethilaka

Electronic and Telecommunication Engineering  
Undergraduate  
University of Moratuwa  
Sri Lanka

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🐙 Github - github.com/PrabathBK  
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### SUMMARY

I am Prabath Wijethilaka, a Final Year undergraduate student in Electronic and Telecommunication Engineering at the University of Moratuwa, skilled in digital electronics and communications.

### Interest Areas

I have a strong interest in FPGA Hardware Accelerated Systems, Computer Architecture, Embedded Systems, AI & ML, Full Stack Developing, Entrepreneurship, Sports and Outdoor Activities.

### EDUCATION

- **BSc (Hons) Electronic and Telecommunication Engineering** 2022 - Present  
University of Moratuwa CGPA/Percentage: 3.69/4.0
- **GCE Advanced Level Examinations** 2012-2020  
Dharmaraja College - Kandy Physical Science Stream
  - Z score - 2.5258
  - District Rank - 13, Island Rank - 134

### EXPERIENCE

- **Hardware Accelerated Systems Engineer - Internship** On-site  
London Stock Exchange Group Dec 2024 – June 2025

I contributed to the verification of high-performance FPGA-based networking systems. I developed a UVM-driven Ethernet packet capture and replay tool capable of injecting .pcap files to reliably reproduce real production failures. I also migrated the full testbench architecture from nanosecond to femtosecond precision, resolving critical timing alignment issues in the TCP Offload Engine pipeline. Additionally, I explored Linux kernel driver operation for configuring the Xilinx Alveo U50 data-center FPGA and integrated Model Checking principles into the verification methodology to strengthen functional correctness and coverage.

### RECOMMENDATIONS

*"Prabath demonstrated outstanding self-learning skills, quickly adapting to our existing codebase with minimal intervention and significantly improved the test bench's running time. I highly recommend Prabath to any organization. He would be an invaluable asset to any forward-thinking organization"*

— Nuwantha Silva, Assoc. Tech Lead (FPGA), London Stock Exchange Group

(LinkedIn Recommendation)

View full recommendation on LinkedIn

### CONFERENCES & WORKSHOPS

- **DVCon India 2025 – Design and Verification Conference** Radisson Blu, Marathahalli, Bangalore  
Runners-up – Design Contest September 10–11, 2025
  - \* Awarded **1st Runners-up** at the DVCon India 2025 Design Contest organized by CDAC Trivandrum - Link.
  - \* Designed a custom accelerator for the **VEGA AT1051 SoC** and built a framework capable of running the **full Qwen3 inference pipeline on bare metal**, demonstrating strong hardware–software co-design skills while competing against top university and industry teams in a rigorous verification challenge.
- **LEAD CS 8.0 – Leadership Development Program** Hotel Ramrich, Ja-Ela  
AIESEC Society – University of Moratuwa March 2022

### PROJECTS

- **SLMs on Edge - 1st Runners-Up | DVCon India 2025 – Design and Verification Conference** Repository  
FPGA Accelerator for Qwen3 SLM Inference Jan 2025 – Sep 2025
  - \* Designed a complete hardware software co-design framework enabling **Qwen3 SLM/LLM inference on the VEGA AT1051 RISC-V SoC**, reducing latency from minutes to seconds through FPGA-accelerated GEMM offloading.
  - \* Built a full bare-metal runtime capable of executing the entire Qwen3 pipeline, including custom memory allocation, tiling schedule generation, AXI-based data movement, and CPU–FPGA synchronization for deterministic sequential inference.
  - \* Developed a lightweight systolic array accelerator featuring **INT8 GEMM**, 16×16 tiled architecture, double buffering, AXI4/AXI-Lite integration, and optimized DMA dataflow - delivering high-throughput GEMM execution on edge hardware.

- **Hardware accelerator for a Vision Transformer-based malware detection system**

*Accelerating ViT-based malware detection on edge devices with VEGA AS1061 Processor, based on RISC-V ISA.*

  - \* This project aims to deploy a ViT-based malware detection system on an edge device equipped with the VEGA AS1061 Processor
  - \* Stage 1 focuses on proposing a novel acceleration IP to enhance the ViT model's inference performance on the VEGA Processor, ensuring effective malware detection in real-world scenarios.

*Report*

Jan 2024
- **CNN Accelerator RTL Implementation**

*High-Performance INT8 CNN Accelerator for Zynq-7020 FPGA*

  - \* Designed and implemented a high-performance CNN accelerator IP core for the Xilinx **Zynq-7020** , featuring a **14×14 INT8 processing-element array** delivering **31.36 GOP/s at 80 MHz**.
  - \* Developed a custom **32-bit ISA**, hierarchical memory system (PE register files + global buffers), and **AXI4 DMA** integration for seamless ARM–FPGA communication.

*Ongoing*

Aug 2025 – Present
- **RV32I Processor Design and Implementation on FPGA**

*RV32I Single Cycle and Pipeline Core*

  - \* **Single-Cycle Core:** Developed a fully verified 32-bit RV32I single-cycle CPU in SystemVerilog with full instruction support and FPGA-ready architecture. - Check Repository
  - \* **Pipelined Core:** Implemented a 5-stage pipelined RV32I CPU with hazard detection, forwarding, stall control, and branch prediction, achieving full RV32I functional verification. - Check Repository
  - \* SystemVerilog, Vivado design flow, RISC-V architecture, pipeline control logic, and hardware verification.

Jul 2024 – Jan 2025
- **EcoWatt – Smart Inverter Monitoring & Control System**

*ESP32-Based IoT Platform for Solar Inverter Telemetry*

  - \* Developed an ESP32-powered IoT system for real-time solar inverter monitoring using **Modbus RTU polling** and an adaptive compression pipeline achieving **96% data size reduction**.
  - \* Implemented encrypted telemetry uploads to a Flask backend with reliable remote command execution and a **secure FOTA pipeline** using **RSA-2048 signature verification** and **AES-encrypted firmware delivery**.

*Ongoing*

Aug 2025 – Present
- **TransX – Transformer Maintenance Full-Stack Web Platform**

*AI-Powered Thermal Inspection & Maintenance System*

  - \* Developed a full-stack transformer maintenance platform integrating **YOLOv8 thermal anomaly detection**, canvas-based annotation tools, and a complete inspection workflow for end-to-end transformer health assessment.
  - \* Built using a microservice architecture with **React, Spring Boot, Flask, and MySQL**, enabling automated reporting, real-time collaboration, and scalable transformer data management.

*Ongoing*

Jul 2025 – Present
- **Serial Bus Design**

*Custom RTL Bus Interconnect with Arbitration & Split Transactions*

  - \* Developing a custom RTL serial bus featuring a **fixed-priority arbiter** (Master0 > Master1), **range-based address decoder**, and parameterized master/slave interface modules.
  - \* Implemented **split-transaction handling** with full verification using module-level and top-level testbenches (**Verilator** + **Vivado**), and FPGA-ready synthesis flows for both **Vivado** and **Quartus**.

*Ongoing*

Aug 2025 – Present
- **Full-Stack Solution Development with Modular OOP Design**

*Developed a web application as a submodule within a main project.*

  - \* Integrating backend functionalities with frontend components to assembly line operations.
  - \* Spring boot, Java, MongoDB, React, Postman, Rest API

Jan 2024 - May 2024

Repository
- **Project Hydrolink - Champions | SLIoT Challenge 2023**

*A Complete IoT Device Revolutionizing Water Tank Management*

  - \* A complete IoT device revolutionizing water tank management.
  - \* Arduino IDE, ESP Microcontroller, Google Firebase, Flutter, SolidWorks, Altium

2023 - Present

[www.hydrolink.lk](http://www.hydrolink.lk)
- **High-Performance Trading System in C++**

*Flower Exchange Order Matching Engine*

  - \* Developed a high-performance **C++ order matching engine** implementing price–time priority, in-memory order books, and full order validation across multiple instruments.
  - \* Designed the C++ backend architecture including matching logic, execution state handling, and CSV-based batch processing with test coverage.

*Repository*

Aug 2024 – Nov 2024
- **Steer-Safe - Championship | IEEE Circuit Challenge 2024 and 1st Runners-Up | Brainstorm 2024**

*Drowsiness Detection system*

  - \* Developed a lightweight, eyewear-integrated driver safety device using **embedded systems, Communication Protocols**, and low-power firmware for real-time drowsiness and attention monitoring.

*Repository*

Jun 2024 – Oct 2024

- **Gazebo Robot Simulation** May 2024  
Repository  
*Robot Simulation Project using ROS2 Humble and Gazebo*
  - \* Map a room and navigate the robot from one location to another, avoiding obstacles along the way. Additionally, perform object tracking.
  - \* Gazebo, Ros2, Ubuntu, OpenCV
- **Point-to-Point Communication Design project** Aug 2023 - Dec 2023  
Repository  
*We implemented a secure and reliable point-to-point digital wireless communication system using SDR.*
  - \* Our achievements include the successful transmission and reception of diverse data types, such as images, text, and real-time audio.
  - \* Python, GNU radio, MATLAB
- **Industrial Portable Water Quality Measurement Device** Jan 2024 - May 2024  
Repository  
*Developed an industrial portable water quality measuring device using sensor technologies and a Mobile app.*
  - \* Capable of accurately measuring four key parameters: pH, Turbidity, Conductivity, and Temperature.
  - \* Arduino-IDE, ESP-Microcontroller, Google Firebase, Flutter, SolidWorks, Altium
- **UART Communication System Implementation on FPGA using Verilog** May 2024  
Repository  
*Implemented and tested a UART communication system on an FPGA using Verilog.*
  - \* Utilized Quartus Lite for FPGA development and integrated Raspberry Pi for data input.
  - \* Verilog-HDL, Quartus Lite, FPGA, Raspberry-pi, Python
- **Analog Portable Audio Amplifier** Aug 2023 - Dec 2023  
Repository  
*We have designed a Portable Audio Amplifier using only analog components.*
  - \* Our device is capable of amplifying audio input from any audio-generating device through three main sub-circuits: preamplifier, tone controller, and power amplifier. We've implemented the Baxandall passive tone controller.
  - \* Simulink, Proteus, LT-Spice, Altium, Solidworks
- **Machine Learning Projects**   
*Repository*
  - \* DiabetesAI-Webproject
  - \* SMS spam detector
  - \* Stock prediction
  - \* Breast Cancer Wisconsin Diagnostic Predictor
  - \* Cardiovascular Disease Predictor

## AWARDS

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- **1st Runners-Up | DVCon India 2025 – International Design Contest** 2025
  - \* SLMs on Edge – A lightweight FPGA-based systolic array accelerator and bare-metal inference engine designed to run the full Qwen3 pipeline on the VEGA AT1051 RISC-V SoC.
- **Championship | SLIoT Challenge 2023 - All island IoT competition** 2023
  - \* Hydrolink - A Complete IoT Device Revolutionizing Water Tank Management
- **Championship | IEEE Sri Lanka Circuit Challenge 2024** 2024
  - \* Steer Safe by PulseX - A wearable device that utilizes machine learning and Electrooculography (EOG) signals to track a driver's state of awareness in real-time.
- **1st Runners-Up | Brainstorm 2024 - Healthcare innovation competition** 2024
  - \* Steer Safe - A wearable device that utilizes machine learning and Electrooculography (EOG) signals to track a driver's state of awareness in real-time
- **Stage 2 (Top 20) | DVCon India 2024 - International Design Contest** 2024
  - \* GateMasters - Design and implement a hardware accelerator for a Vision Transformer-based malware detection system on a VEGA Processor.
- **Finalist | HackX 2024 - Inter University Startup Challenge** 2024
  - \* Hydrolink - A Complete IoT Device Revolutionizing Water Tank Management.
- **Dean's List**
  - \* Semester 2, 6

## SPECIALIZATIONS AND CERTIFICATIONS

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- **Function Acceleration on FPGA with Vitis**  
*Udemy*
- **Linux Device Drivers**  
*LinkedIn Learning*
- **High-Performance and Mission-Critical Software Development Using C++**  
*London Stock Exchange Group*
- **Introduction to FPGA Design for Embedded Systems**  
*University of Colorado Boulder - Coursera*
- **FPGA Softcore Processors and IP Acquisition**  
*University of Colorado Boulder - Coursera*
- **Hardware Description Languages for FPGA Design**  
*University of Colorado Boulder - Coursera*
- **Machine Learning Specialization**  
*Deeplearning.AI - Coursera*
- **AAT Level 3 Completed**  
*Association of Accounting Technicians of Sri Lanka*
- **Diploma in English**  
*Esoft Metro Campus - Sri Lanka*
- **Diploma in IT**  
*Esoft Metro Campus - Sri Lanka*

## EXTRA-CURRICULAR AND VOLUNTEERING

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- **Judge Board – HackElite 2.0** 2025  
*IEEE Sri Lanka Women in Engineering – University of Moratuwa*
- **Conduct Knowledge Session: Advanced Biomedical Electronics & Computational Technologies** 2025  
*IEEE EMBS Student Branch Chapter – University of Moratuwa*
- **Conduct Knowledge Session: Raspberry Pi Web Services** 2025  
*Pi Mora, SPARK Branch - University of Moratuwa*
- **Head of Marketing** Aug 2025 - Present  
*Electronic Club - University of Moratuwa*
- **Marketing Coordinator** Sep 2024 - Aug 2025  
*Electronic Club - University of Moratuwa*
- **Social Media Sub-Coordinator** Aug 2023 - Sep 2024  
*Electronic Club - University of Moratuwa*
- **Social Media Sub-Coordinator** Aug 2023 - Sep 2024  
*Electronic Club - University of Moratuwa*
- **Department Batch Representative** Jan 2024 - May 2025  
*Department of Electronic and Telecommunication Engineering - University of Moratuwa*
- **Finance Committee member** Mar 2023 - Aug 2023  
*IEEE Society University of Moratuwa - project "Mora Foresight 1.0"*
- **Event Sub-Committee member** July 2023 - Aug 2023  
*EXMO - University of Moratuwa*
- **Finance Committee member** Aug 2022 - Dec 2022  
*AIESEC Society University of Moratuwa - project "Rooted 1.0"*
- **Junior Prefect** Jan 2015 - Dec 2015  
*Dharmaraja Collage - Kandy*
- **President of Collage Hosteler's Society** Jan 2017 - Dec 2017  
*Dharmaraja Collage - Kandy*
- **Volunteering in Sasnaka Sansada** 2021 - 2022  
*Teaching experience with Volunteering in "Ganitha Saviya" Project*

## SPORTS AND ACTIVITIES

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- **Sri Lanka University Games Championship 2023**  
*University Baseball Team - University of Moratuwa*
- **Participated STRIDIAN'23**  
*Mora Hiking Club - University of Moratuwa*

- **Captain of the college under 17 volleyball team**  
*Dharmaraja College - Kandy*
- **Obtained a 'Merit' for Hockey on Annual "Colors Nite".**  
*Dharmaraja College - Kandy*
- **Member of the college Baseball, and Hockey team**  
*Dharmaraja College - Kandy*

## TECHNICAL SKILLS

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- **Languages:** Java, C, C++, VHDL, Verilog, SystemVerilog, Python, SQL, React, JavaScript, Dart, HTML, CSS
- **Developer Tools:** Vivado, Vitis, Quartus, IntelliJ, MATLAB, Git, Altium Designer, SolidWorks, Android Studio, Gazebo, Docker, VS Code, Postman
- **Frameworks:** UVM, Spring Boot, Flutter, Arduino, Scikit-learn, ROS2
- **Cloud/Databases:** Firebase, Mongo DB, Microsoft Azure, MySQL
- **Operating Systems:** Ubuntu, Windows, RedHat , Raspbian
- **Soft Skills:** Problem-Solving, Team Leadership, Project Management, Teamwork, Public Speaking, Finance and Account management, Strategic Decision-Making, Digital Marketing, Teaching, Photography, Videography

## REFERENCES

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- **Ajith A. Pasqual,**  
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