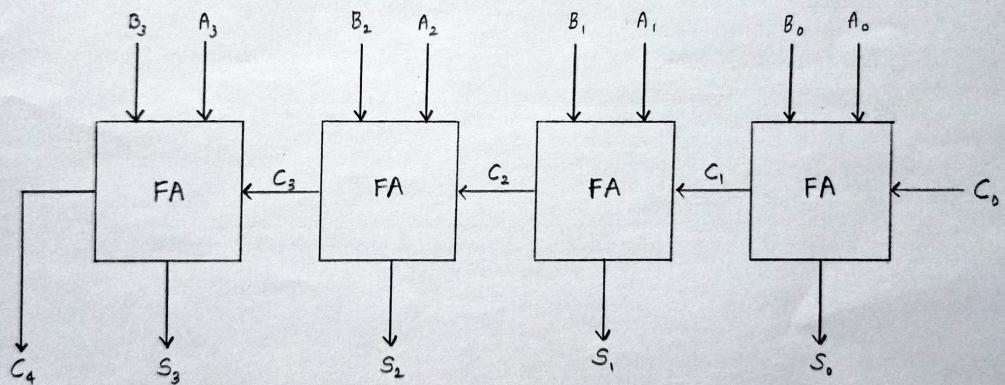
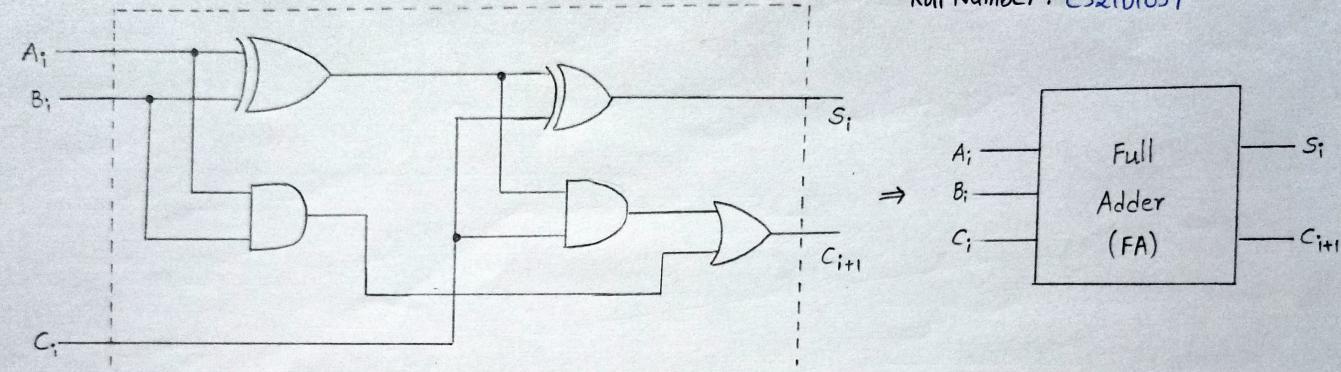


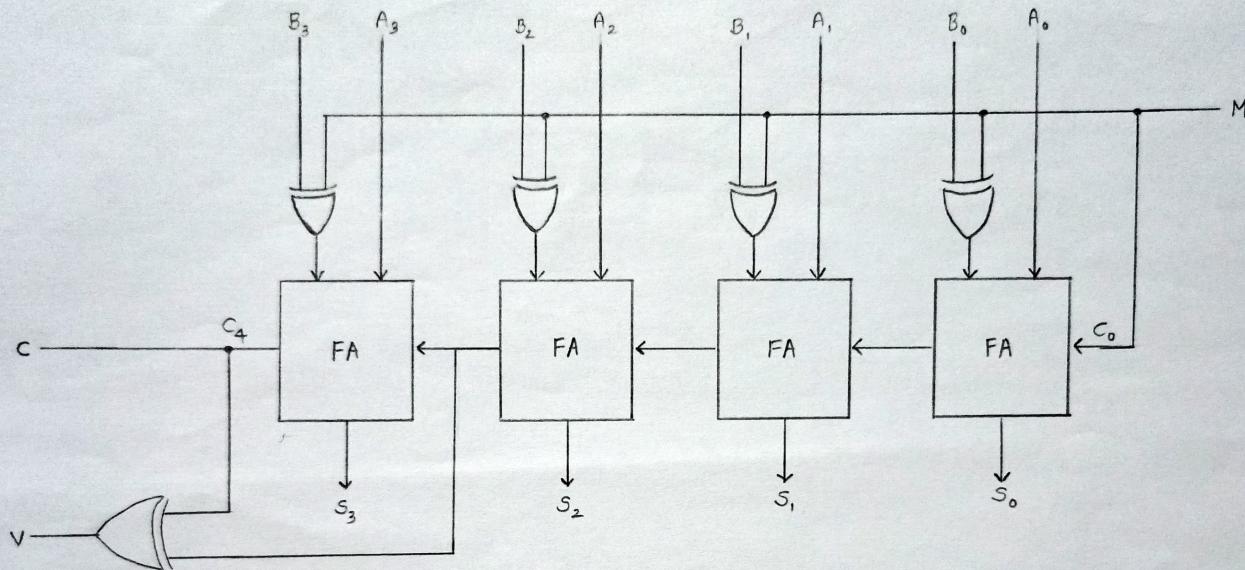
FOUR-BIT ADDER CIRCUIT

Name: M. Prabhas Reddy
Roll Number: CS21B1039



* Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs A and B and the third input carry is C_{in} . The output carry is designated as C_{out} and normal output is designated as S which is SUM.

FOUR-BIT ADDER-SUBTRACTOR



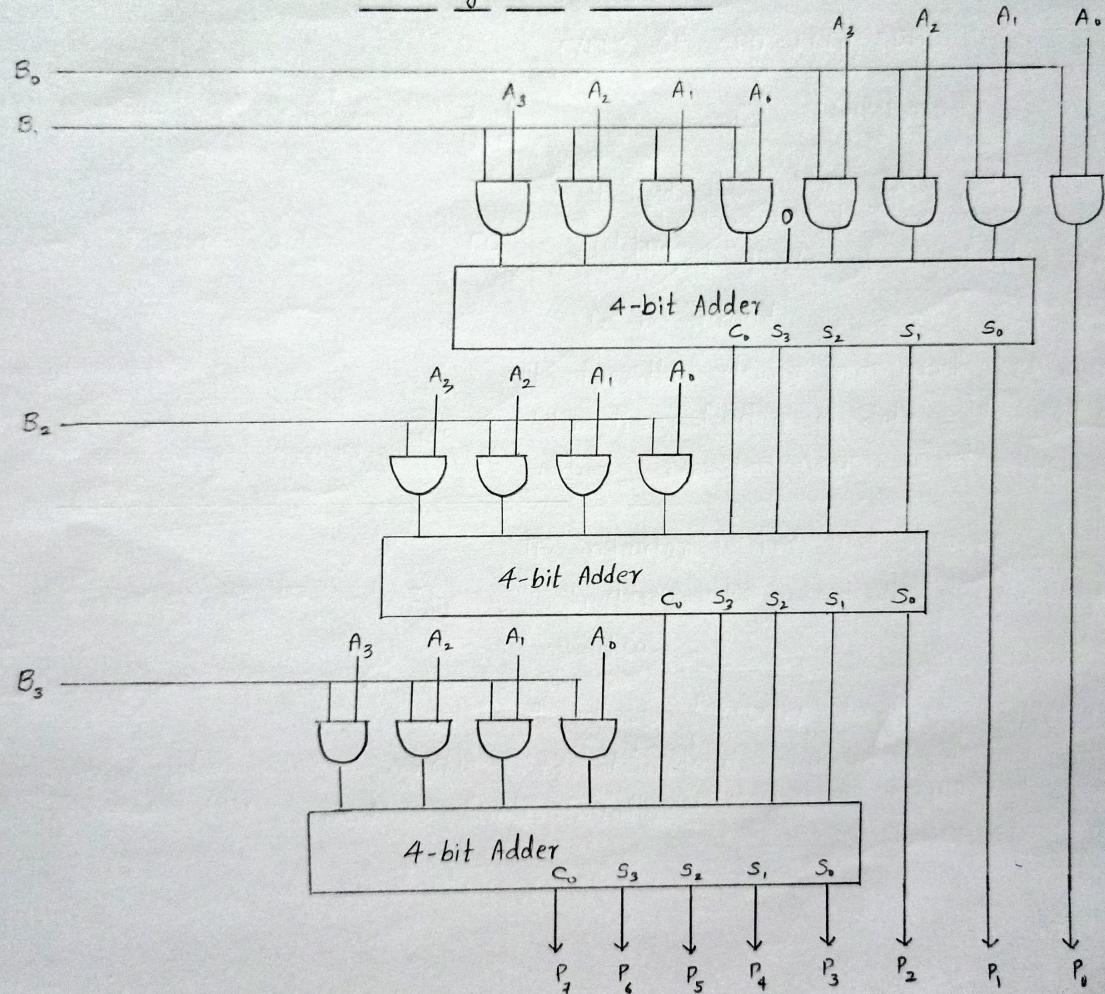
* The subtraction $A - B$ can be done by taking the 2's complement of B and adding it to A . The 2's complement can be obtained by taking the 1's complement and adding 1 to the least significant pair of bits.

* The mode input M controls the operation..

$M=0 \Rightarrow$ Adder circuit

$M=1 \Rightarrow$ Subtractor circuit.

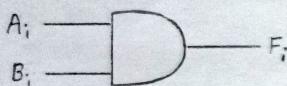
4-Bit By 4-Bit Multiplier



LOGICAL OPERATIONS

1. AND operation:

- AND is used for supporting logical expressions by performing bitwise AND operation.



A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

2. OR operation:

- OR is used for supporting logical expressions by performing bitwise OR operation.



A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT operation:

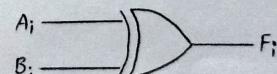
- NOT implements the bitwise NOT operation by reversing the bits in an operand.



A	F
0	1
1	0

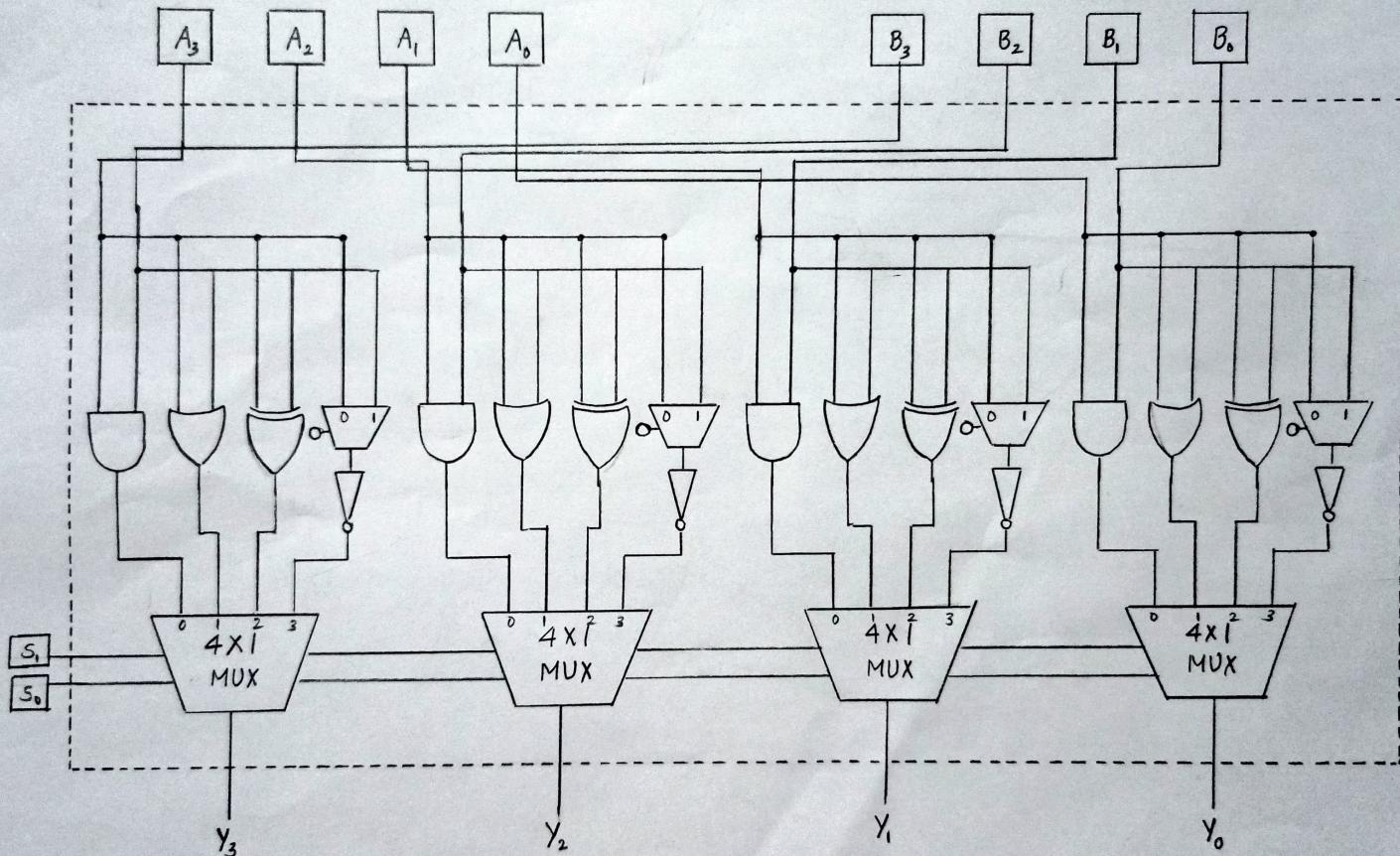
4. XOR operation:

- XOR operation sets the resultant bit to 1, if and only if the bits from the operands are different.



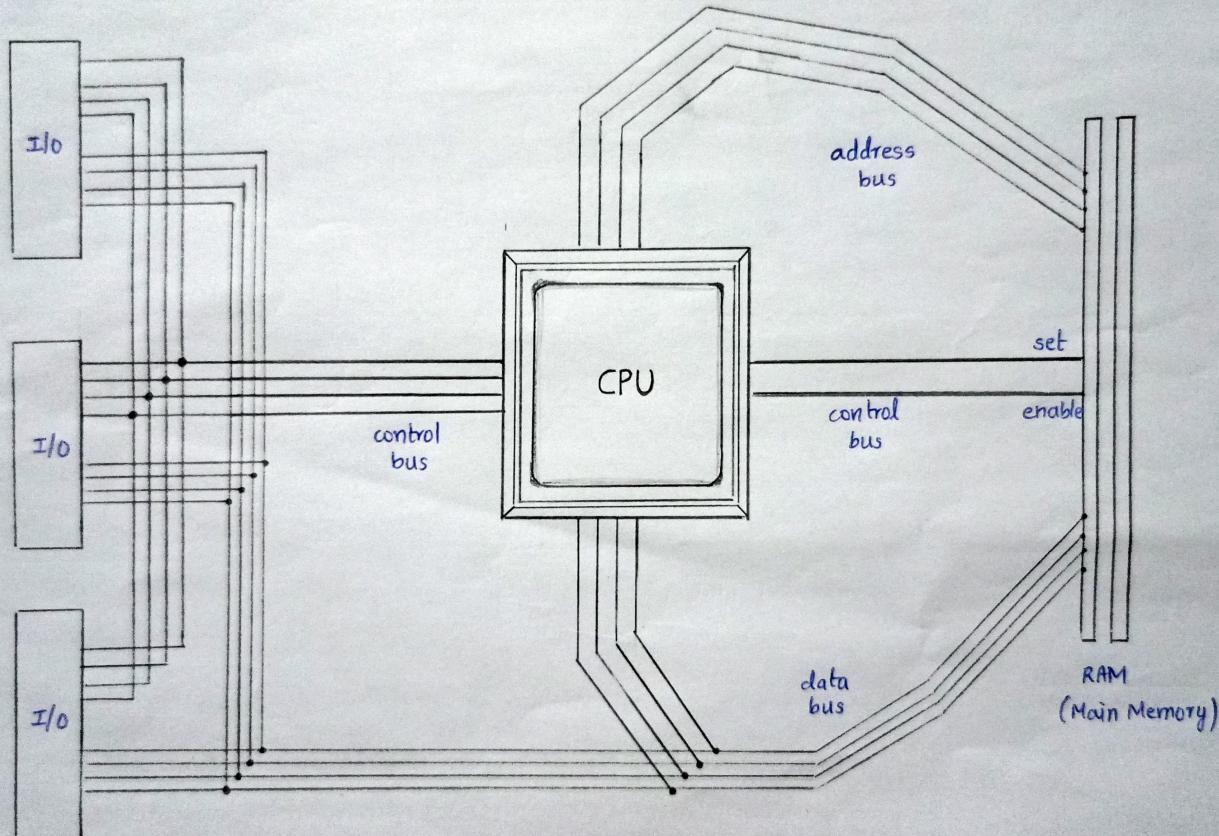
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

LOGICAL UNIT - AND, OR, XOR, NOT



* The 2×1 MUX is used to perform the NOT operation for both inputs - A and B. If select line is 0, input A is NOTed otherwise input B.

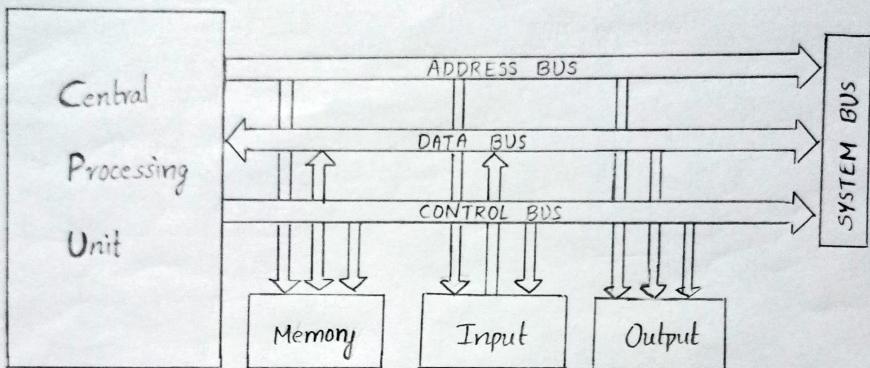
FUNCTIONAL UNITS



NOTE: The no. of lines in the buses are just drawn to illustrate the data flow between functional units.

SYSTEM BUS

(7)



- A bus used to communicate between the major components of a computer is called a System bus. It contains 3 categories of lines:

1. Address Lines:

- Used to carry the address to memory and IO.
- Unidirectional
- Based on the width of an address bus we can determine capacity of main memory.

2. Data Lines:

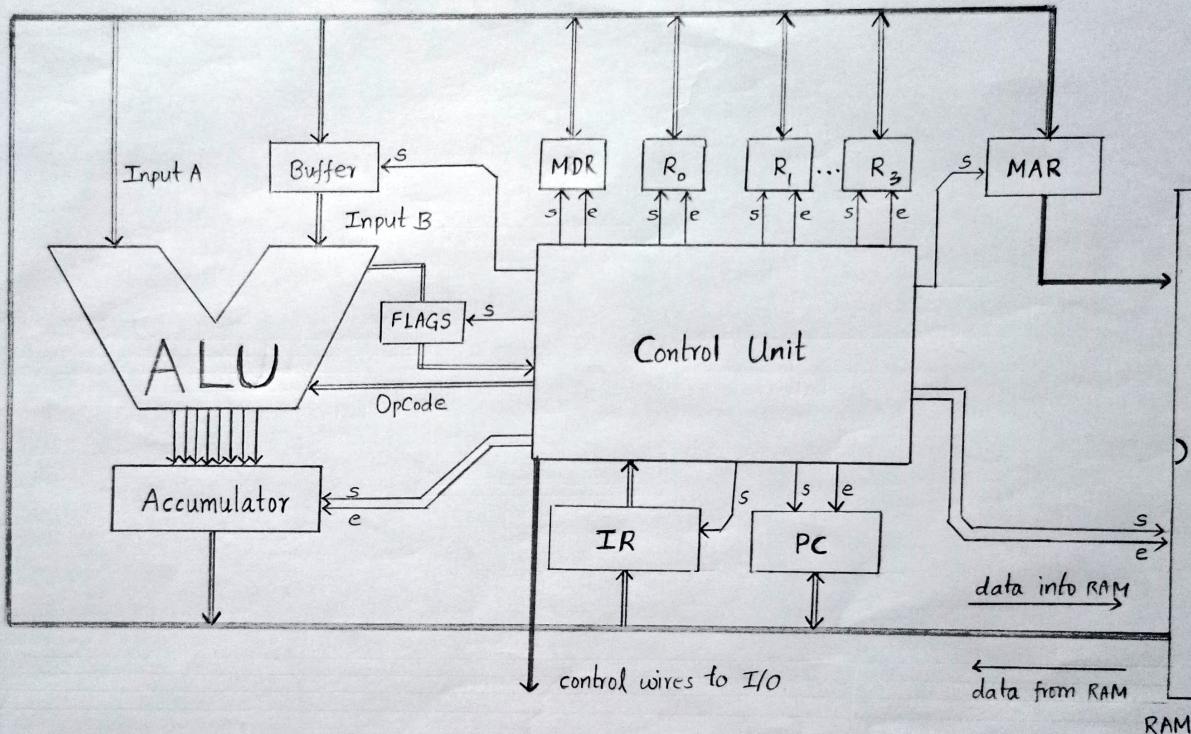
- Used to carry data between CPU, memory and IO.
- Bidirectional
- Based on width of a data bus we can determine word length of CPU.

3. Control Lines:

- Used to carry the control and timing signals.
- Control signals indicate the type of operation.

Central Processing Unit (CPU)

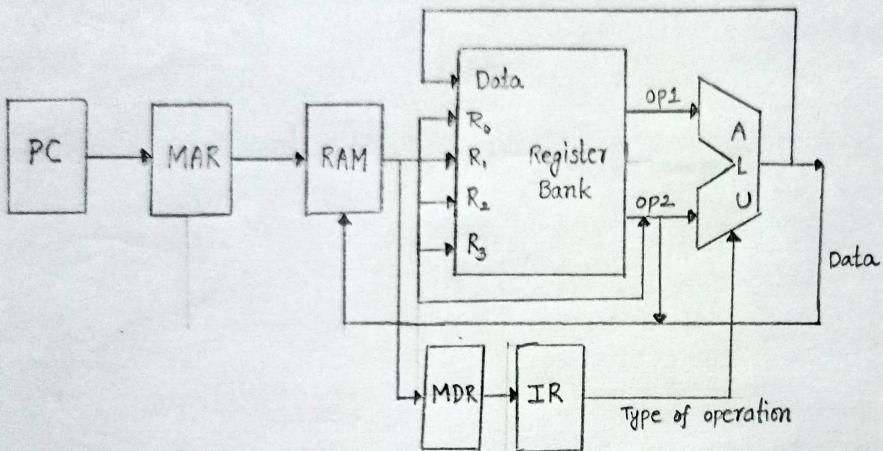
s-set
e-enable



TYPES OF CPU REGISTERS

S.No.	CPU Register	Short Form	Functionality
1.	Program Counter.	PC	It holds the address the next instruction to be fetched. Also called the instruction address register, keeps track of the memory location of next instruction to be executed.
2.	Memory Address Register	MAR	It stores the address from which CPU needs to fetch the instruction or data and also store the address where the data will be stored in memory.
3.	Instruction Register	IR	The instruction fetched from memory is stored in Instruction Register where the decoder decodes the instruction.
4.	Accumulator	AC	It acts as temporary storage location which holds an intermediate value in mathematical or logical calculations.
5.	Memory Data Register	MDR	The operand fetched from the operand address, is stored in a register known as memory data register.

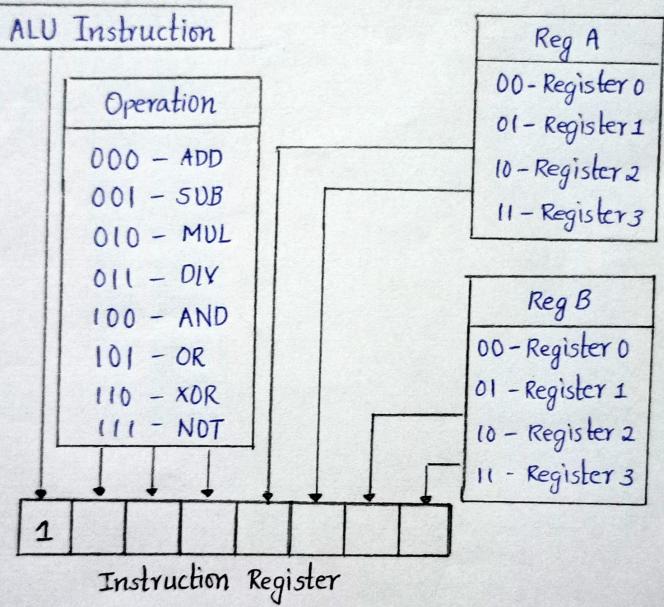
DATA PATH AND CONTROL



PC - Program Counter
 MAR - Memory Address Register
 RAM - Random Access Memory
 IR - Instruction Register
 ALU - Arithmetic & Logic Unit.

Operating steps:

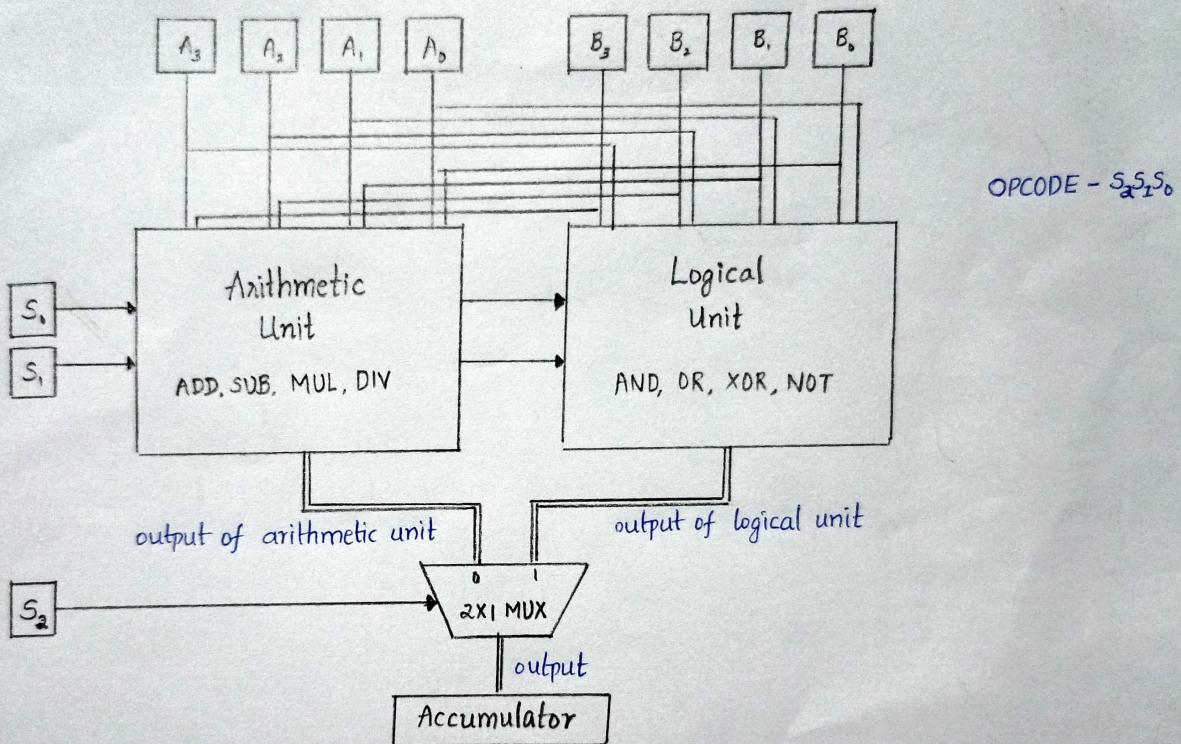
- PC is set to point to the first instruction. The contents of PC are transferred to MAR.
- A read signal is sent to the memory. The instruction is read out and loaded into MDR
- The contents of MDR are transferred to IR. Decode and execute the instruction.
- Get operands for ALU, Perform operation in ALU
- store the result back to general purpose register or to the memory
- During the execution, PC is incremented to the next instruction.



General Purpose Registers

- Register 0 (R_0)
- Register 1 (R_1)
- Register 2 (R_2)
- Register 3 (R_3)

Arithmetic and Logic Unit (ALU)



Input A : 4 bits

Input B : 4 bits

Output : 8 bits