COA: CPU Simulator ISA Design

Team Members:

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Constraints:

Instruction length: 16 bits (2 bytes)

Number of registers in Register File: 8 (address of 3 bits)

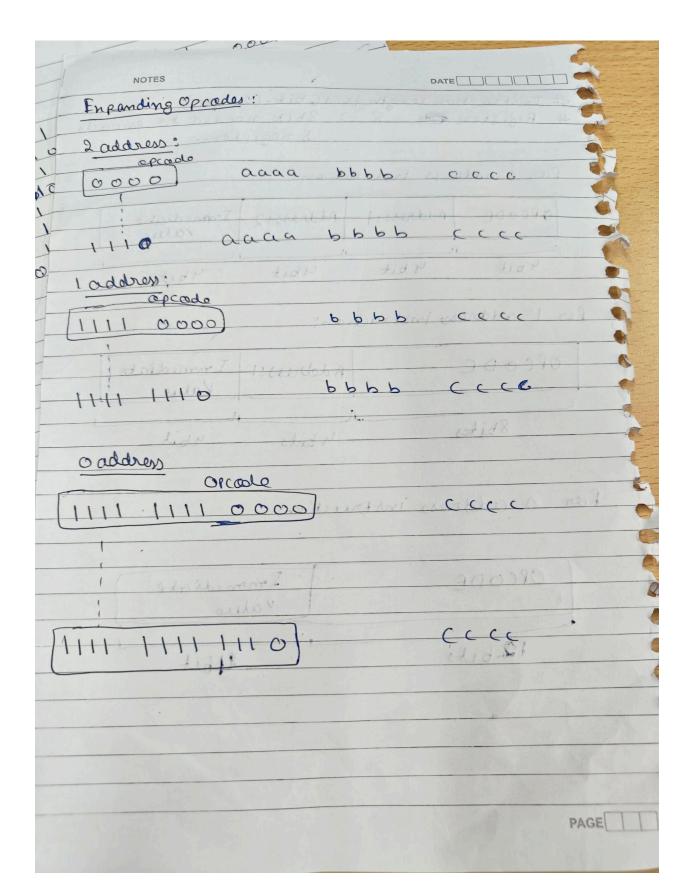
Data: 8 bits

Instruction	Opcode	Description	
BGT	0000	Branch to the specified address if the value in Register_1 is greater than Register_2	
LOAD	0001	Load the value from a memory address or immediate value into Register_1	

STORE	0011	Register_1 * Register_2 -> [Register_1] Or Register_1 * Immediate_ Value -> [Register_1]	
MOVE	0100	Moves value in register_1 If addressing mode : 1. 0 : Value of register_2 in register_1 2. 1 : Immediate value stored in register_1	
ADD	0010	Register_1 + Register_2 -> [Register_1] Or Register_1 + Immediate_ Value -> [Register_1]	

SUB	0101	Register_1 - Register_2 -> [Register_1]	
		Or	
		Register_1 - Immediate_ Value -> [Register_1]	
MUL	0110	Register_1 * Register_2 -> [Register_1] Or	
		Register_1 * Immediate_ Value -> [Register_1]	
DIV	0111	Register_1 / Register_2 -> [Register_1] Or	
		Register_1 / Immediate_ Value -> [Register_1] Gives absolute value (Quotient)	
AND	1000	Bitwise AND between Register_1 and Register_2 -> [Register_1]	
OR	1001	Bitwise OR between Register_1 and Register_2 -> [Register_1	
NOT	1010	Bitwise NOT of Register_1 -> [Register_1]	
JMP	1011	Jump to the address specified by the immediate value or register	
BEQ	1100	Branch to the address if Register_1 == Register_2	
BNE	1101	Branch to the address if Register_1 != Register_2	
BLT	1110	Branch to the address if Register_1 < Register_2	

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R,	0010	ADD	0010
P,	0011	SUB	0101
R3	00100	MUL	0110
Ry	0101	DIV	10111
O Rs	0110	AND	1000
R6	0111	OR	(00)
Rz	0000		1010
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