COA : CPU Simulator ISA Design

Team Members :

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Constraints :

Instruction length : 16 bits (2 bytes)
Number of registers in Register File : 8 (address of 3 bits)
Data : 8 bits

Instruction	Opcode	Description
BGT	0000	Branch to the specified address if the value in Register_1 is greater than Register_2
LOAD	0001	Load the value from a memory address or immediate value into Register_1
STORE	0011	Register_1 * Register_2 -> [Register_1] Or Register_1 * Immediate_ Value -> [Register_1]
MOVE	0100	Moves value in register_1 If addressing mode : 1. 0 : Value of register_2 in register_1 2. 1 : Immediate value stored in register_1
ADD	0010	Register_1 + Register_2 -> [Register_1] Or Register_1 + Immediate_ Value -> [Register_1]

SUB	0101	Register_1 - Register_2 -> [Register_1] Or Register_1 - Immediate_ Value -> [Register_1]
MUL	0110	Register_1 * Register_2 -> [Register_1] Or Register_1 * Immediate_ Value -> [Register_1]
DIV	0111	Register_1 / Register_2 -> [Register_1] Or Register_1 / Immediate_ Value -> [Register_1] Gives absolute value (Quotient)
AND	1000	Bitwise AND between Register_1 and Register_2 -> [Register_1]
OR	1001	Bitwise OR between Register_1 and Register_2 -> [Register_1
NOT	1010	Bitwise NOT of Register_1 -> [Register_1]
JMP	1011	Jump to the address specified by the immediate value or register
BEQ	1100	Branch to the address if Register_1 == Register_2
BNE	1101	Branch to the address if Register_1 != Register_2
BLT	1110	Branch to the address if Register_1 < Register_2

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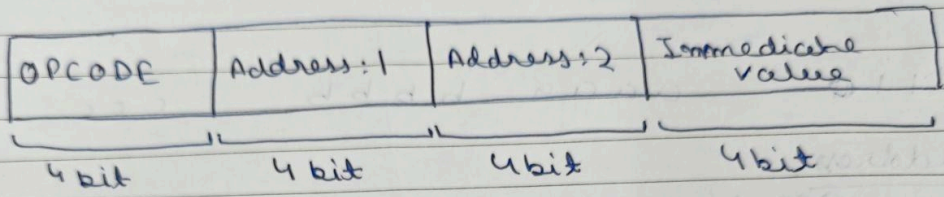
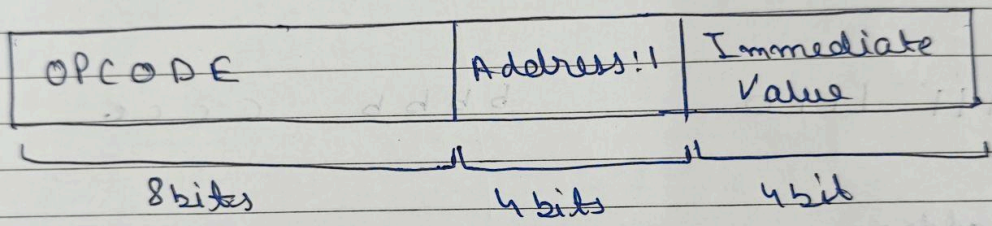
Instruction length is 16 bit. (2 bytes)
Registers = 8 ⇒ 3bits needed to encode 8 registers.

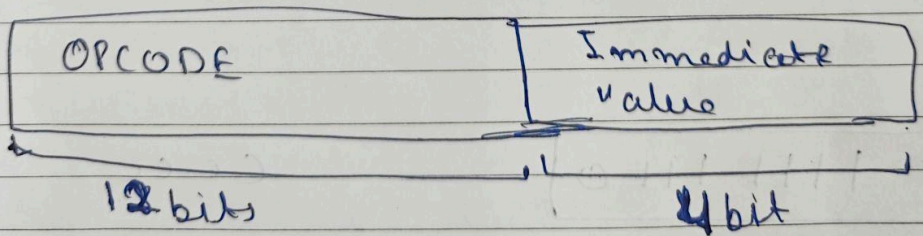
For 2 address instruction:



For 1 address instruction:



For 0-address instruction:



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Expanding Opcodes:

2 address:

opcode

0000 aaaa bbbb cccc

1110 aaaa bbbb cccc

1 address:

opcode

1111 0000 bbbb cccc

1111 1110 bbbb cccc

0 address

opcode

1111 1111 0000 cccc

1111 1111 1110 cccc

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8 registers:

R_0	0001
R_1	0010
R_2	0011
R_3	0100
R_4	0101
R_5	0110
R_6	0111
R_7	0000

Operation	OPCODE
LOAD	0001
STORE	0011
MOV	0100
ADD	0010
SUB	0101
MUL	0110
DIV	0111
AND	1000
OR	1001
NOT	1010
JMP	1011
B EQ	1100
BNE	1101
BLT	1110
BGT	0000