

## Inverters with n-type MOSFET load:-

### Limitations of Resistive load Inverter:-

- ① Resistive load inverter circuit is not suitable for digital system applications because of the large area occupied by the load resistor.
- ② Power dissipation is large because in resistive type load resistor load is a resistor.

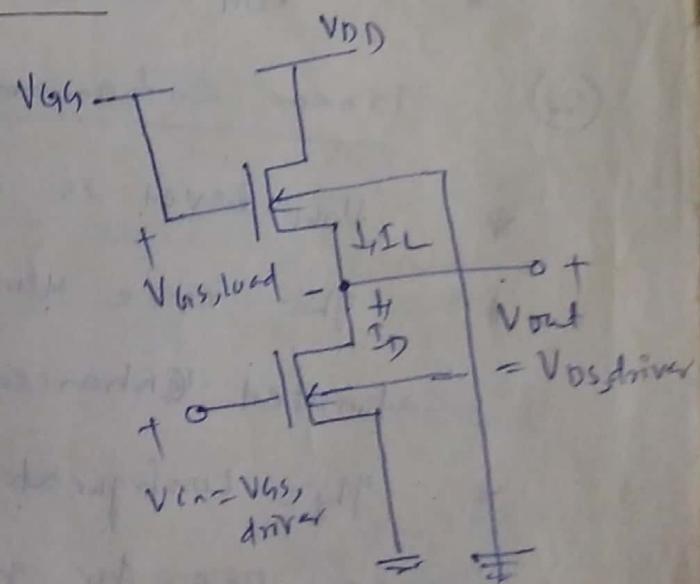
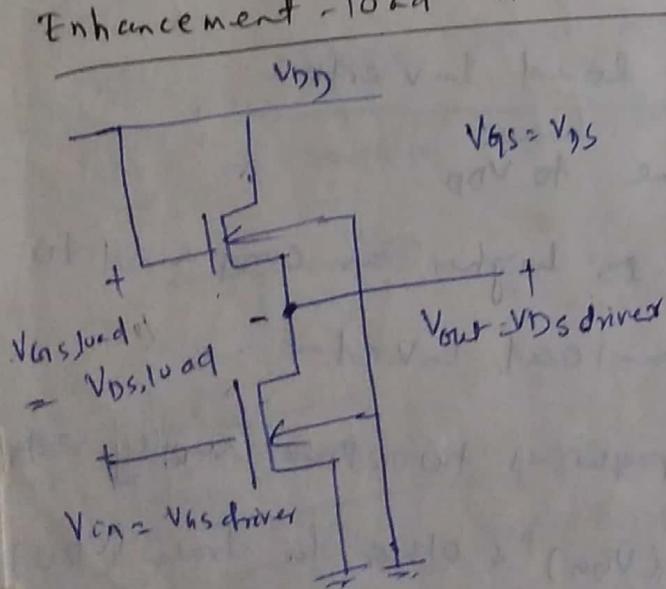
### Advantages of n-type MOSFET Inverter load:-

- ① Load device is an active load instead of load resistor.
- ② Silicon area occupied by the transistor is usually smaller as compare to resistive load.
- ③ Overall performance is better.

→ Inverter with n-type MOSFET load is of 2 types

- ① Enhancement-load n-mos inverter
- ② Depletion-load " "

### Enhancement-load n-mos Inverter:-



(a) Inverter circuit with saturated enhancement type n-mos load

(b) Inverter with linear enhancement-type load

- Depending on the bias voltage applied to the gate, the load transistor can be operated in saturation region or in linear region.
- These two inverters have some advantages & disadvantages according to the design of each part.
- Enhanced-load inverters are of two types

- (1) Saturated enhancement-load inverter
- (2) Linear " "

### (1) Saturated enhancement-load inverter

- \* The saturated enhancement-load inverter load requires a single voltage supply & the both gate & drain is  $V_{DD}$ .
- \* Fabrication process is simple.
- \*  $V_{OH}$  level is limited to  $V_{DD} - V_{Tload}$ .

### (2) Linear enhancement-load inverter

- \*  $V_{OH}$  level is equal to  $V_{DD}$ .
- \* The noise margin is higher as compared to saturated enhancement-load inverter.
- \* This configuration requires two bias supply voltages i.e. one for gate ( $V_{bias}$ ) & other for drain ( $V_{DD}$ ).

### Drawback of enhancement-load inverters

- Both types of inverters suffer from relatively high Stand-by or DC power dissipation because

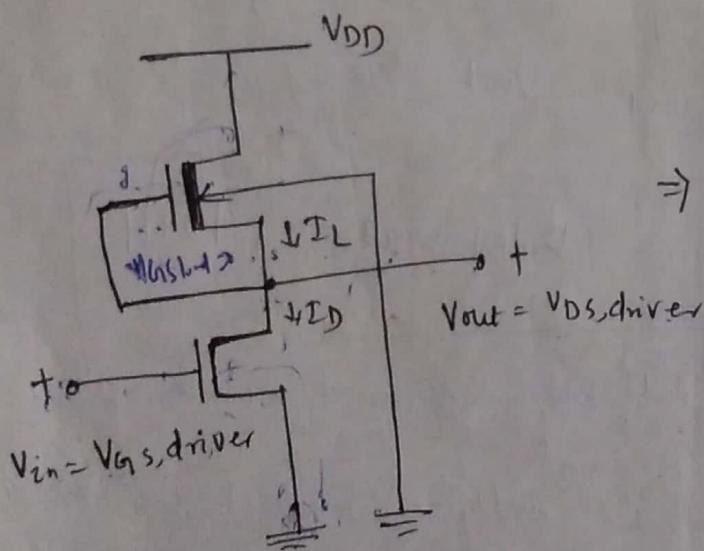
Enhancement-load nmos inverters are not used in any large scale digital applications.

### Depletion-Load nmos Inverter:-

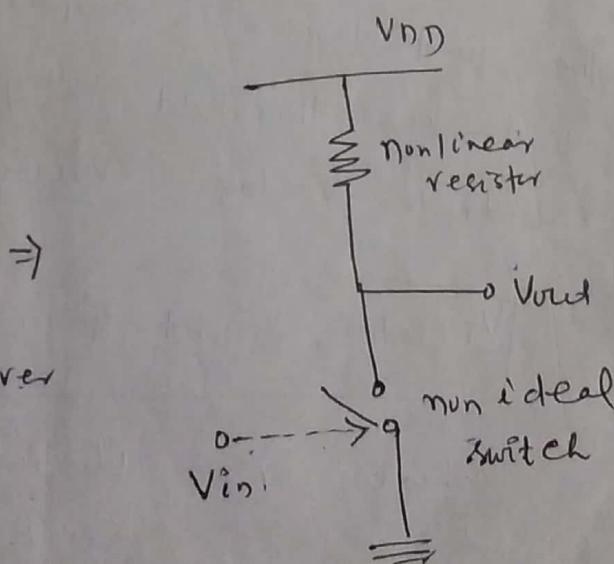
→ several disadvantages of the enhancement-type load inverter can be avoided by using a depletion-type nmos transistor as the load device.

#### Advantages :-

- (i) The fabrication process for producing an inverter with enhancement type nmos driver and depletion type nmos load is slightly more complicated and requires additional processing steps, especially for the channel implant to adjust the threshold voltage of the ~~load~~ load device.
- (ii) Sharp VTC & better Noise Margin
- (iii) Single power supply
- (iv) Smaller overall layout area



(a) Inverter circuit with depletion-type nmos load.



(b) Equivalent circuit consisting of a nonlinear resistor and a nonideal switch controlled by the input

## Working Principle:

- The driver device is an enhancement type nmos transistor, with  $V_{TO,driver} > 0$ , whereas the load is a depletion-type nmos transistor, with  $V_{TO,load} < 0$ .
- The current-voltage eqn to be used for the depletion type load transistor are identical to those of enhanced type device, with the exception of negative threshold voltage.
- The gate & the source nodes of the load transistor are connected; hence  $V_{GS,load} = 0$  always. Since the threshold voltage of the depletion-type load is negative, the condition  $V_{GS,load} > V_{T,load}$  is satisfied and the load device has a conducting channel regardless of the input & o/p voltage levels.
- Both the driver transistor & load transistor are built on the same p-type substrate which is connected to ground. The load device is subject to the substrate-bias effect. So that its threshold voltage is a function of its source-to substrate voltage,  $V_{SB,load} = V_{out} - \underline{V_{SB,driver}} = 0$ .

$$V_{T,load} = V_{TO,load} + r(\sqrt{2\phi_F} + V_{out} - \sqrt{12\phi_F})$$

where  $r$  = substrate bias coefficient or body effect coefficient

$\phi_F$  = potential difference at Fermi level.

## Operating Regions:-

→ the operating mode of the load transistor is determined by the O/P voltage level.

Case-I When the O/P voltage is small i.e. when  $V_{out} < V_{DD} + V_{T,load}$ ,

then the load transistor operates in saturation region.

$$\Rightarrow V_{DS,load} > V_{DS,load} - V_{T,load}$$

so Saturation load current is given by

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[ -V_{T,load}(V_{out}) \right]^2$$

$$\begin{cases} V_{DD} - V_{out} > -V_{TL} & \text{satn} \\ V_{DD} - V_{out} \leq V_{TL} & \text{linear} \end{cases}$$

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[ V_{T,load}(V_{out}) \right]^2$$

Case-II For larger O/P voltage levels i.e.  $V_{out} > V_{DD} + V_T$ , then the depletion-type load transistor operates in the linear region.

The load current is given by

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[ 2 \cdot V_{T,load}(V_{out}) \cdot (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

$V_{in}$	$V_{out}$	Driver-operating region	Load operating region
$V_{OL}$	$V_{OH}$	Cut-off	Linear
$V_{IL}$	$\approx V_{OH}$	Saturation	Linear
$V_{IH}$	Small	Linear	Saturation
$V_{OH}$	$V_{OL}$	Linear	Saturation

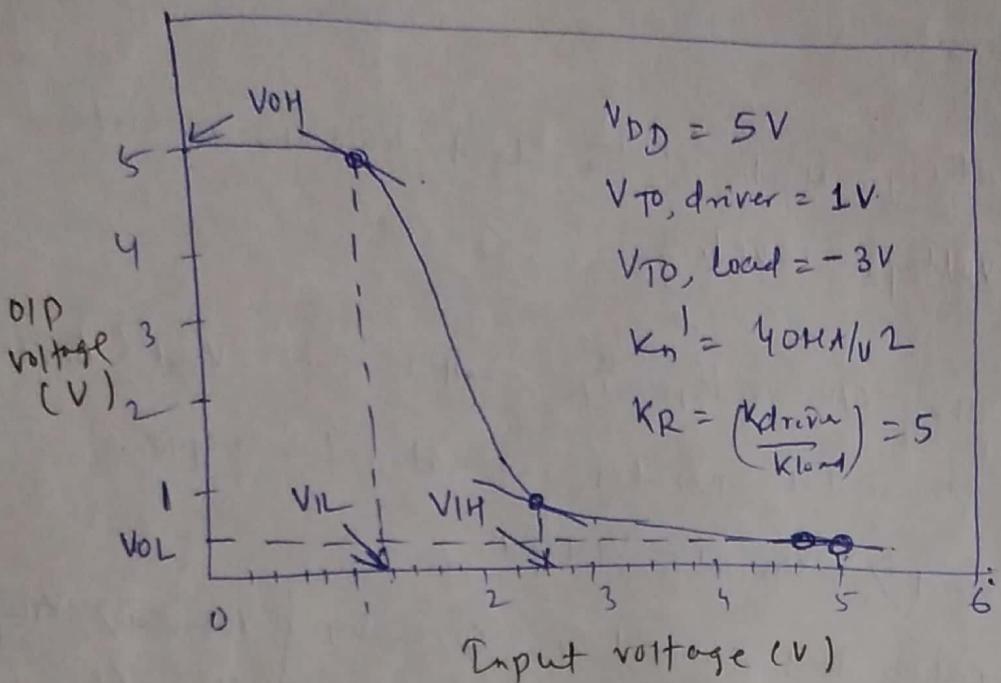


Fig: Typical VTC of a depletion-load inverter circuit

→ The Voltage Transfer characteristic (VTC) of this inverter can be constructed by setting  $I_{D, \text{driver}} = I_{D, \text{load}}$ ,  $V_{GS, \text{driver}} = V_{in}$  and  $V_{DS, \text{driver}} = V_{out}$  and  $V_{out} = f(V_{in})$

Calculation of  $V_{OH}$  :-

- When the input voltage  $V_{in}$  is smaller than the driver threshold voltage  $V_{TO}$ , the driver transistor is turned off and does not conduct any drain current. i.e  $I_{D, \text{driver}} = 0$ .
- The load device, which operates in linear region and also has zero drain current.

We know that  
 $I_{D, \text{load}} = I_{D, \text{driver}}$

Let  $I_{D, \text{load}} = 0$ .

⇒  $(I_{D, \text{load}})$  ~~at~~ Linear =  $(I_{D, \text{driver}})$  cut-off

⇒  $(I_{D, \text{load}}) = 0$

$$I_{D,load} = \frac{k_n,load}{2} \left[ 2 |V_{T,load}(v_{out})| (V_{DD} - v_{out}) - (V_{DD} - v_{out})^2 \right] = 0$$

put  $v_{out} = V_{OH}$

$$\Rightarrow \frac{k_n,load}{2} \left[ 2 |V_{T,load}(V_{OH})| (V_{DD} - V_{OH}) - (V_{DD} - V_{OH})^2 \right] = 0$$

$$\Rightarrow (V_{DD} - V_{OH}) \left[ \frac{k_n,load}{2} [2 |V_{T,load}(V_{OH})| - (V_{DD} - V_{OH})] \right] = 0$$

$k_n,load \neq 0$   
 $V_{DD} - V_{OH} = 0$

$$V_{DD} = V_{OH}$$

$$\text{or } \boxed{V_{OH} = V_{DD}}$$

Calculation of  $V_{OL}$ :

→ To calculate the o/p low voltage  $V_{OL}$ , we assume that the input voltage  $v_{in}$  of the inverter is equal to

$$V_{OH} = V_{DD}$$

→ In this case, the driver transistor operates in the linear region while depletion-type load is in saturation.

As we know that

$$I_{D,driver} = I_{D,load}$$

$$\Rightarrow (I_{D,driver})_{\text{linear}} = (I_{D,load})_{\text{saturation}}$$

$$\Rightarrow \frac{k_n,driver}{2} \left[ 2 (v_{in} - V_{TO}) v_{out} - v_{out}^2 \right] = \frac{k_n,load}{2} [-V_{T,load}(v_{out})]$$

$$\text{but } \boxed{v_{in} = V_{OH}, \quad v_{out} = V_{OL}}$$

$$\Rightarrow \frac{k_n,driver}{2} \left[ 2 (V_{OH} - V_{TO}) V_{OL} - V_{OL}^2 \right] = \frac{k_n,load}{2} [-V_{T,load}(V_{OL})]$$

$$\Rightarrow 2(V_{OH} - V_{TO})V_{OL} - V_{OL}^2 = \frac{K_n|load}{K_n,driver} |V_{T,load}(V_{OL})|^2$$

$$\Rightarrow V_{OL}^2 - 2(V_{OH} - V_{TO})V_{OL} + \frac{K_n|load}{K_n,driver} |V_{T,load}(V_{OL})|^2 = 0$$

The above eqn is now in quadratic eqn

$$a = 1, b = -2(V_{OH} - V_{TO}), c = \frac{K_n|load}{K_n,driver} |V_{T,load}(V_{OL})|^2$$

$$V_{OL} = \frac{-(-2) \pm \sqrt{4(V_{OH} - V_{TO})^2 - 4 \cdot 1 \cdot \frac{K_n|load}{K_n,driver} |V_{T,load}(V_{OL})|^2}}{2 \times 1}$$

$$= \frac{2(V_{OH} - V_{TO}) \pm 2\sqrt{(V_{OH} - V_{TO})^2 - \frac{K_n|load}{K_n,driver} |V_{T,load}(V_{OL})|^2}}{2}$$

$$= V_{OH} - V_{TO} \pm \sqrt{(V_{OH} - V_{TO})^2 - \frac{K_n|load}{K_n,driver} |V_{T,load}(V_{OL})|^2}$$

$$V_{OL} = (V_{OH} - V_{TO}) - \sqrt{(V_{OH} - V_{TO})^2 - \frac{K_n|load}{K_n,driver} |V_{T,load}(V_{OL})|^2}$$

(From  $\pm$ , we will take  $-ve$  sign, because  $V_{OL}$  is the Low O/P voltage).

## Calculation of V<sub>IL</sub>

→ Slope of the VTC is equal to (-1) i.e.  $\frac{dV_{out}}{dV_{in}} = -1$ , when the I/P

$$\text{voltage } V_{in} = V_{IL}$$

→ In this case, the driver transistor operates in saturation while the load transistor operates in the linear region.

We know that

$$I_{D, \text{load}} = I_{D, \text{driver}}$$

$$\Rightarrow (I_{D, \text{load}})_{\text{linear}} = (I_{D, \text{driver}})_{\text{saturation}}$$

$$\text{or } (I_{D, \text{driver}})_{\text{saturation}} = (I_{D, \text{load}})_{\text{linear}}$$

$$\frac{K_{\text{driver}}}{2} (V_{in} - V_{TO})^2 = \frac{K_{\text{load}}}{2} \left[ 2 |V_{T, \text{load}}(V_{out})| (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

Differentiating w.r.t  $V_{in}$  -

$$\Rightarrow K_{\text{driver}} @ (V_{in} - V_{TO}) = \frac{K_{\text{load}}}{2} \left[ 2 |V_{T, \text{load}}(V_{out})| \left( -\frac{dV_{out}}{dV_{in}} \right) \right.$$

$$+ 2(V_{DD} - V_{out}) \frac{d|V_{T, \text{load}}(V_{out})|}{dV_{in}} \frac{dV_{out}}{dV_{in}}$$

$$- 2(V_{DD} - V_{out}) \left( -\frac{dV_{out}}{dV_{in}} \right) \left] \right.$$

$$= \frac{K_{\text{load}}}{2} \left[ 2 |V_{T, \text{load}}(V_{out})| \left( -\frac{dV_{out}}{dV_{in}} \right) + 2(V_{DD} - V_{out}) \left( -\frac{dV_{T, \text{load}}}{dV_{in}} \right) - 2(V_{DD} - V_{out}) \left( -\frac{dV_{out}}{dV_{in}} \right) \right]$$

$$\text{Now put } \frac{dV_{T, \text{load}}}{dV_{in}} = 0, \frac{dV_{out}}{dV_{in}} = -1$$

$$\Rightarrow K_{\text{driver}} (V_{in} - V_{TO}) = \frac{K_{\text{load}}}{2} \left[ 2 |V_{T, \text{load}}(V_{out})| - 2(V_{DD} - V_{out}) \right]$$

$$K_{\text{driver}} (V_{in} - V_{TO}) = \frac{K_{\text{load}}}{2} \left[ |VT_{\text{load}}(V_{out})| - (V_{DD} - V_{out}) \right]$$

$$V_{in} - V_{TO} = \frac{K_{\text{load}}}{K_{\text{driver}}} \left[ |VT_{\text{load}}(V_{out})| + V_{out} - V_{DD} \right]$$

$$V_{in} = V_{TO} + \left( \frac{K_{\text{load}}}{K_{\text{driver}}} \right) \left[ V_{out} - V_{DD} + |VT_{\text{load}}(V_{out})| \right]$$

Put  $V_{in} = V_{IL}$

$$V_{IL} = V_{TO} + \frac{K_{\text{load}}}{K_{\text{driver}}} \left[ V_{out} - V_{DD} + |VT_{\text{load}}(V_{out})| \right]$$

Calculation of  $V_{IH}$ :

→  $V_{IH}$  is the larger of the two voltage points on the VTC at which the slope is equal to (-1).

→ Driver transistor is in operation in the linear region and load transistor is in saturation.

We know that  $I_{D, \text{driver}} = I_{D, \text{load}}$

⇒  $(I_{D, \text{driver}})_{\text{linear}} = (I_{D, \text{load}})_{\text{saturation}}$

$$\Rightarrow \frac{K_{\text{driver}}}{2} \left[ 2(V_{in} - V_{TO})V_{out} - V_{out}^2 \right] = \frac{K_{\text{load}}}{2} \left[ -|VT_{\text{load}}(V_{out})|^2 \right]$$

Differentiating w.r.t  $V_{in}$

$$\Rightarrow K_{\text{driver}} \left[ 2(V_{in} - V_{TO}) \frac{dV_{out}}{V_{in}} + 2V_{out} \cdot \frac{d(V_{in} - V_{TO})}{dV_{in}} - 2V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$= K_{\text{load}} \left[ 2 \cdot (-|VT_{\text{load}}(V_{out})|^2) \cdot \frac{d|VT_{\text{load}}(V_{out})|}{dV_{out}} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$\text{Pdt} \quad \frac{dV_{out}}{dV_{in}} = -1$$

$$\Rightarrow K_{\text{driver}} [-2(V_{in} - V_{TO}) + 2V_{out} + 2V_{out}] \\ = -2K_{\text{load}} \left[ -V_{T\text{load}}(V_{out}) \frac{dV_{T\text{load}}}{dV_{out}} \right]$$

$$\Rightarrow K_{\text{driver}} [- (V_{in} - V_{TO}) + 2V_{out}] = -2K_{\text{load}} \left[ \left\{ \begin{array}{l} V_{T\text{load}}(V_{out}) \\ \frac{dV_{T\text{load}}}{dV_{out}} \end{array} \right\} \right]$$

$$\Rightarrow - [(V_{in} - V_{TO})] + 2V_{out} = - \frac{K_{\text{load}}}{K_{\text{driver}}} \left[ \left\{ \begin{array}{l} V_{T\text{load}}(V_{out}) \\ \frac{dV_{T\text{load}}}{dV_{out}} \end{array} \right\} \right]$$

$$\Rightarrow -V_{in} + V_{TO} + 2V_{out} = - \frac{K_{\text{load}}}{K_{\text{driver}}} \left[ \left\{ \begin{array}{l} V_{T\text{load}}(V_{out}) \\ \frac{dV_{T\text{load}}}{dV_{out}} \end{array} \right\} \right]$$

$$\Rightarrow V_{in} - V_{TO} - 2V_{out} = \frac{K_{\text{load}}}{K_{\text{driver}}} \left[ \left\{ \begin{array}{l} V_{T\text{load}}(V_{out}) \\ \frac{dV_{T\text{load}}}{dV_{out}} \end{array} \right\} \right]$$

$$\Rightarrow V_{in} = V_{TO} + 2V_{out} + \frac{K_{\text{load}}}{K_{\text{driver}}} \left[ \left\{ \begin{array}{l} V_{T\text{load}}(V_{out}) \\ \frac{dV_{T\text{load}}}{dV_{out}} \end{array} \right\} \right]$$

Pdt  $V_i$

Pdt  $V_{in} = V_{IH}$

$$V_{IH} = V_{TO} + 2V_{out} + \frac{K_{\text{load}}}{K_{\text{driver}}} \left[ \left\{ \begin{array}{l} V_{T\text{load}}(V_{out}) \\ \left( \frac{dV_{T\text{load}}}{dV_{out}} \right) \end{array} \right\} \right]$$

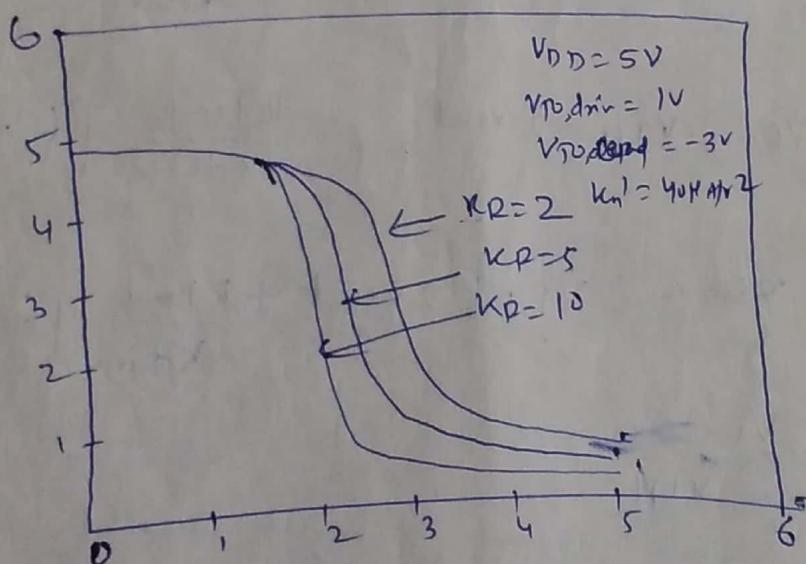
$$\text{But} \quad \frac{dV_{T\text{load}}}{dV_{out}} = \frac{\gamma}{2\sqrt{(\gamma^2 - 1)V_{out}}} \quad \boxed{\gamma}$$

$\Rightarrow$  The critical voltage points, the general shape of the inverter VTC & the noise margins are determined

by the threshold voltage of the driver & load devices and  
driver-to-load ratio ( $k_{\text{driver}}/k_{\text{load}}$ )

- $k_{\text{driver}} = k_{\text{load}}$ , the driver-to-load ratio is  
determined by the (W/L) ratios of the driver-to-load  
transistor i.e. by the device geometries.
- the total area occupied by a depletion-load inverter  
circuit with an acceptable cut performance is expected to be  
much smaller than the area occupied by a comparable  
resistive-load or enhancement-load inverter.

### Design of Depletion-load Inverters:-



- The design parameter in an inverter circuit are
- (i) Power supply voltage  $V_{DD}$
  - (ii) Threshold voltages of driver & load transistor
  - (iii) W/L ratio of the driver & load transistor

- The power supply voltage  $V_{DD}$  of the inverter circuit and  
determines the level of high output voltage  $V_{OH}$ . The  
remaining three critical voltages on the VTC, the output

Low voltage VOL is usually the most significant constraint.

→ Designing the inverter to achieve a certain VOL value will automatically set the  $V_{IL}$  &  $V_{IH}$ .

$$\therefore K_R = \frac{k_{\text{driver}}}{k_{\text{load}}} = \frac{|V_T|_{\text{load(VOL)}}|^2}{2(V_{OH} - V_{TO})V_{OL} - V_{OL}^2}$$

$$K_R = \frac{k_n | \text{driver (W/L)}_{\text{drive}}}{k_n | \text{load (W/L)}_{\text{load}}}$$

✓ since the channel doping densities & channel electron mobilities of the enhancement-type driver transistor & the depletion-type load transistor are not equal, i.e. ~~different~~  $k_n | \text{driver} \neq k_n | \text{load}$  in general case. But in this inverter both driver & load are made up of same substrate e.g. p-substrate. so  $k_n | \text{driver} \approx k_n | \text{load}$ .

$$K_R = \frac{(W/L)_{\text{driver}}}{(W/L)_{\text{load}}}$$

→ the design procedure determines the ratio of driver & load transconductance but not specific ( $W/L$ ) ratio of each transistor.

→ the actual sizes of load transistor are usually determined by

(i) current driver capability

(ii) steady state power dissipation

(iii) the transistor switching speed.

## CMOS Inverter:-

- It consists of an enhancement-type n-mos driver transistor and a load device an enhancement-type p-mos transistor.
- In this configuration, input signal is always applied to the gate of the driver transistor and the operation of the inverter is controlled primarily by switching the driver.
- This configuration is called complementary MOS (CMOS). The circuit topology is complementary push-pull in the sense that for high input, the nmos transistor drives the O/P node while pmos acts as the load and for low input the pmos transistor drives the O/P node while the nmos transistor acts as load.

The CMOS inverter has two important advantages over the other Inverter config

- ① The steady state power dissipation of CMOS inverter circuit is negligible.
- ② The voltage transfer characteristics (VTC) exhibits a full O/P voltage swing between OV & VDD. This results high noise margin. Also, the VTC transition is usually very sharp and hence, the CMOS Inverter resembles an ideal inverter characteristics.

### Limitations

1. Since Nmos & Pmos transistors must be fabricated on the same chip side-by-side the CMOS process is more complex than the standard Nmos-only process.
2. Formation of parasitic bipolar transistors are due to close proximity of Nmos & Pmos transistors causes CMOS latch condition. Additional guard rings must be built around the Nmos

& PMOS transistors to prevent undesirable effect.

### Circuit Diagram:

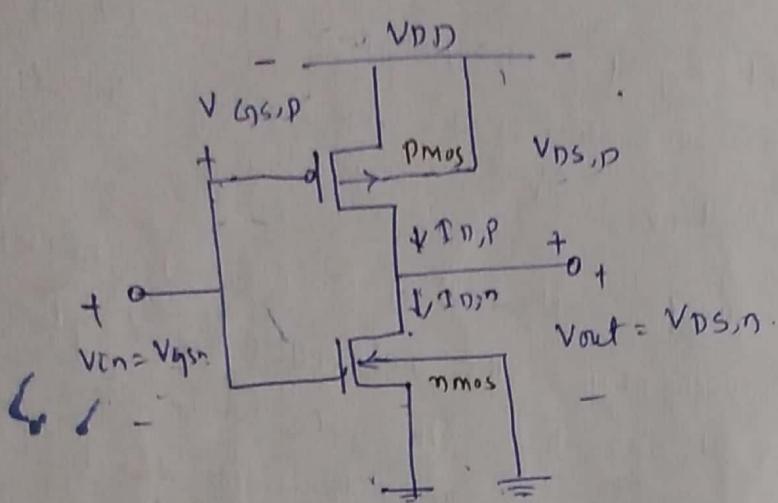
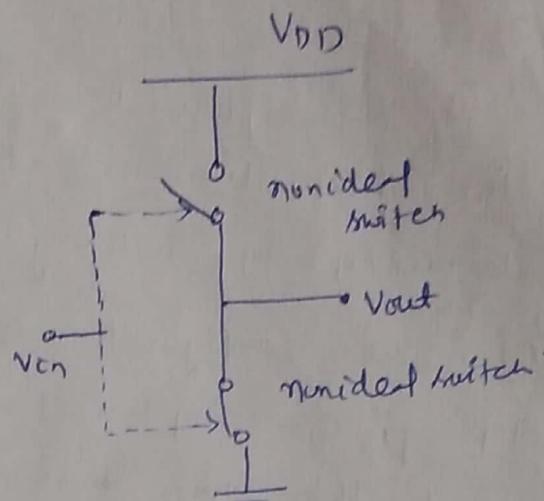
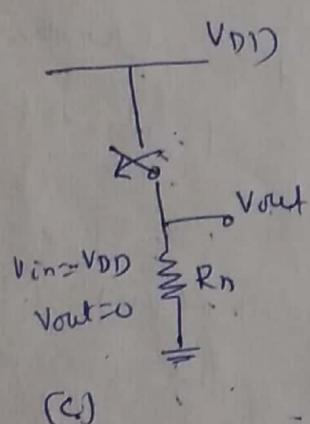


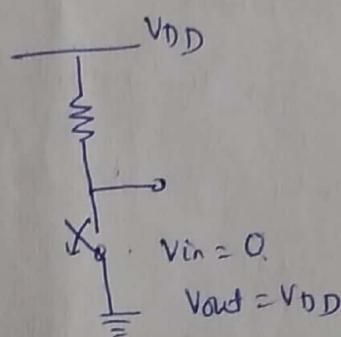
Fig (a) CMOS Inverter circuit



(b) simplified equivalent circuit



(c)



(d)

(switch model of CMOS Inverter)

→ The operation is readily understood with the aid of simple switch Model of the MOS transistor. The transistor nothing but a switch with an infinite OFF resistance for  $|V_{GS}| > V_T$  and a finite ON resistance for  $|V_{GS}| \leq V_T$ .

→ When  $V_{in}$  is high and equal to  $V_{DD}$ , the NMOS transistor is ON and the PMOS transistor is OFF. So a direct path exists between  $V_{out}$  & ground node, resulting in steady-state value of 0V.

- When the input  $V_{in}$  is low (0V), NMOS transistor OFF & PMOS transistor ON. So a path exists between  $V_{DD}$  &  $V_{out}$ , resulting a high  $V_{DD}$  voltage. Thus, the gate functions as an inverter.
- NMOS transistor is ON for high input & OFF for low input, thereby operating under positive logic, while PMOS transistor is OFF for high input & ON for low input with negative logic operation.

### Ckt Operation:

- ① In the CMOS inverter ckt, the input voltage is connected to gate terminals of both the NMOS & PMOS transistors. Thus, both transistors are driven directly by the input signal  $V_{in}$ . The substrate of the NMOS transistor is connected to the ground, while substrate of the PMOS transistor is connected to the power supply voltage  $V_{DD}$ , in order to reverse-bias the source & drain junction. Since  $V_{SD} = 0$  for both NMOS & PMOS there is no substrate bias effect.

### Case-I

When the input voltage is smaller than the NMOS threshold voltage i.e. when  $V_{in} < V_{Tn,n}$ , the NMOS transistor is cut-off. At the same time, the PMOS transistor is ON, operating in the linear region. Since the drain currents for both transistors are approximately equal to zero i.e.

$$I_{D,n} = I_{D,p} = 0$$

the drain-to-source voltage of PMOS transistor is equal to zero.

the O/P voltage  $V_{OH}$  is equal to the power supply voltage.

$$V_{out} = V_{OH} = V_{DD}$$

### Case-II

When input voltage exceeds  $(V_{DD} + V_{TO,P})$ , the PMOS transistor is turned off and NMOS transistor is operating in the linear region, but its drain-to-source voltage is equal to zero.

The O/P voltage of the CKT is

$$V_{out} = V_{OL} = 0$$

### Case-III

Now we have to see the operating modes of NMOS & PMOS transistors as functions of input & O/P voltages.

→ The NMOS transistor operates in saturation if  $V_{in} > V_{TO,n}$

$$\text{and } V_{DS,n} > V_{GS,n} - V_{TO,n} \Leftrightarrow V_{out} > V_{in} - V_{TO,n}$$

→ The PMOS transistor operates in saturation if  $V_{in} < V_{DD} + V_{TO,p}$

$$\text{and } V_{DS,p} \leq V_{GS,p} - V_{TO,p} \Leftrightarrow V_{out} \leq V_{in} - V_{TO,p}$$

Relation B/w voltages for three regions of operation of a CMOS inverter

	Cut-off	Linear	Saturation
P-device (PMOS)	$V_{GSP} > V_{TP}$ $V_{in} > V_{TP} + V_{DD}$	$V_{GSP} < V_{TP}$ $V_{in} < V_{TP} + V_{DD}$	$V_{GS} < V_{TP}$ $V_{in} < V_{TP} + V_{DD}$
		$V_{DSP} > V_{GSP} - V_{TP}$ $V_{out} > V_{in} - V_{TP}$	$V_{DSP} \leq V_{GSP} - V_{TP}$ $V_{out} \leq V_{in} - V_{TP}$
N-device (NMOS)	$V_{GSn} < V_{TN}$ $V_{in} < V_{TN}$	$V_{GSn} > V_{TN}$ $V_{in} > V_{TN}$	$V_{DSn} \geq V_{GS} - V_{TN}$ $V_{out} \geq V_{in} - V_{TN}$
		$V_{DSn} \leq V_{GS} - V_{TN}$ $V_{out} \leq V_{in} - V_{TN}$	

### Region-A

This region is defined by  $0 \leq V_{in} \leq V_{th}$  in which inverter is cut-off ( $I_{DSn} = 0$ ), and the p-device is in linear.

$$I_{DSn} = -I_{DSP}$$

Since  $I_{DSn} = 0$ ,  $I_{DSP} = 0$

$$\text{Also } V_{DS,P} = V_{out} - V_{DD}$$

The drain-to-source current for p-device is also zero.

Zero.

$$V_{out} - V_{DD} = V_{DS,P}$$

$$V_{out} - V_{DD} = 0$$

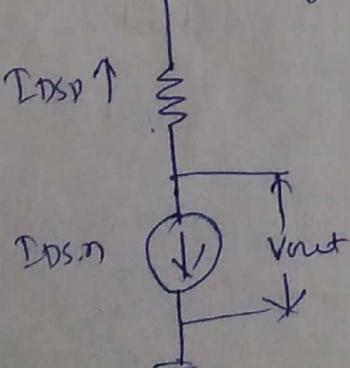
$$\boxed{V_{out} = V_{DD}}$$

$$\boxed{V_{out} = V_{OH} = V_{DD}}$$

### Region-B

This region is characterized by  $V_{th} \leq V_{in} \leq V_{DD}/2$  in which pmos is in its linear region ( $V_{DS} \neq 0$ ) while transistors in saturation. The equivalent circuit for the inverter in this region can be represented by a resistor for pmos & a current for the nmos transistor.

Region B

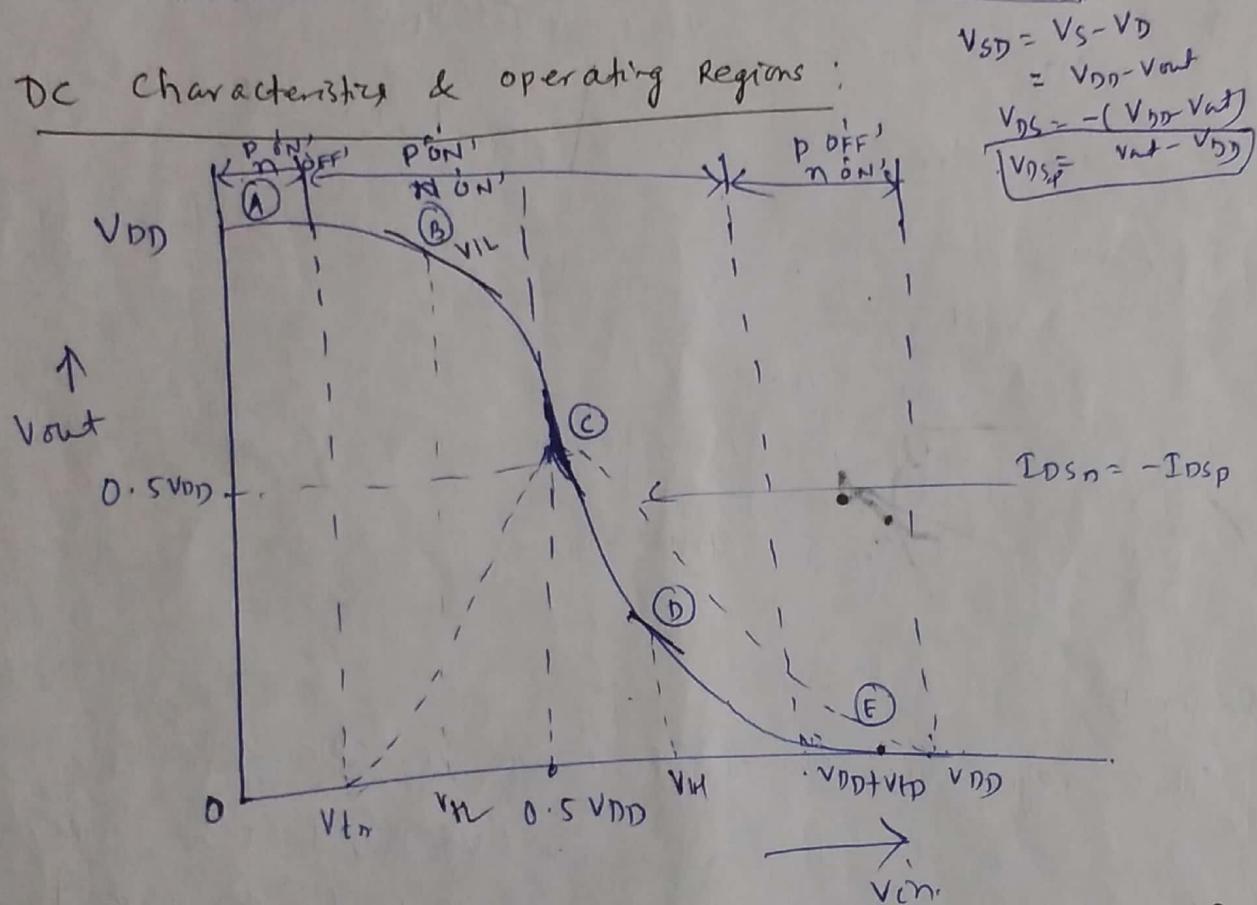


Assumptions:-

$$V_{SG} = V_S - V_G \\ = V_{DD} - V_{in} \\ V_{GS,P} = -(V_{DD} - V_{in}) = V_{in} - V_{DD}$$

$V_{GS,n} = V_{in}$	$I_{DS,n} = -I_{DS,p}$
$V_{DS,n} = V_{out}$	
$V_{GS,P} = -(V_{DD} - V_{in}) = V_{in} - V_{DD}$	
$V_{DS,P} = -(V_{DD} - V_{out}) = V_{out} - V_{DD}$	

DC Characteristics & operating Regions:



Behavior of n & p transistors in the five regions of CMOS Inverter

Region	$V_{in}$	$V_{out}$	NMOS	PMOS
A	$< V_{tn}$	$V_{OH}$	Cut-off	Linear
B	$\phi V_{IL}$	$\text{high} \approx V_{OH}$	Saturation	Saturation
C	$V_{th}$	$V_{IH}$	Saturation	Saturation
D	$V_{IH}$	$\text{low} \approx V_{OL}$	Linear	Cut-off
E	$> V_{DD} + V_{TP}$	$V_{OL}$	Linear	

The saturation current for the nmos,  $I_{DSn}$  is obtained by setting  $V_{GSn} = V_{in}$

$$I_{DSn} = \frac{k_n}{2} (V_{in} - V_{tn})^2$$

The drain current for the pmos can be obtained by substituting  $V_{GSp} = V_{in} - V_{DD}$

$$V_{Dsp} = V_{out} - V_{DD}$$

$$I_{Dsp} = -k_p \left[ 2(V_{in} - V_{DD} - V_{tp}) (V_{out} - V_{DD}) - (V_{out} - V_{DD})^2 \right]$$

$$I_{Dsp} = -I_{DSn}$$

$$\frac{k_n}{2} (V_{in} - V_{tn})^2 = -\frac{k_p}{2} \left[ 2 (V_{in} - V_{DD} - V_{tp}) (V_{out} - V_{DD}) - (V_{out} - V_{DD})^2 \right]$$

$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - \frac{k_n}{k_p} (V_{in} - V_{tp})^2} - 2 (V_{in} - \frac{V_{DD}}{2} - V_{tp}) V_{DD}$$

### Region C:

In this region, both nmos & pmos are in saturation.

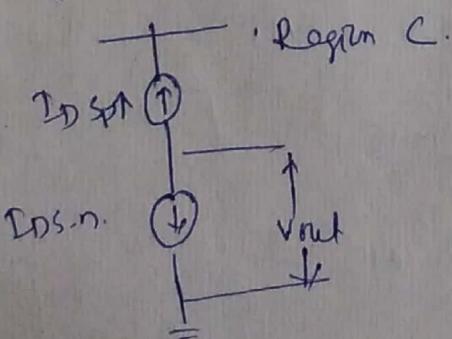


Fig. equivalent circuit for region C of a CMOS inverter

$$D_{DSp} = -\frac{k_p}{2} (V_{in} - V_{DD} - V_{tp})^2$$

$$D_{DSn} = \frac{k_n}{2} (V_{in} - V_{tn})^2$$

Since  $D_{DSn} = -D_{DSp}$

$$\frac{k_n}{2} (V_{in} - V_{tn})^2 = \frac{k_p}{2} (V_{in} - V_{DD} - V_{tp})^2$$

put  $k_n = k_p$ ,  $V_{tn} = -V_{tp}$

$$(V_{in} - V_{tn})^2 = (V_{in} - V_{DD} - V_{tp})^2$$

$$(V_{in} - V_{tn})^2 = (V_{in} - V_{DD} + V_{tn})^2$$

$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn} \sqrt{K_p/k_p}}{1 + \frac{V_{tn}}{V_{DD} + V_{tp}}}$$

$$V_{in} = \frac{V_{DD}}{2}$$

The possible value of  $V_{out}$  in this region can be deduced as follows :

n mos :  $V_{in} - V_{out} < V_{tn}$

$$V_{out} > V_{in} - V_{tn}$$

p mos :  $V_{in} - V_{out} > V_{tp}$

$$V_{out} < V_{in} - V_{tp}$$

Combining the two inequalities results in

$$V_{in} - V_{tn} < V_{out} < V_{in} - V_{tp}$$

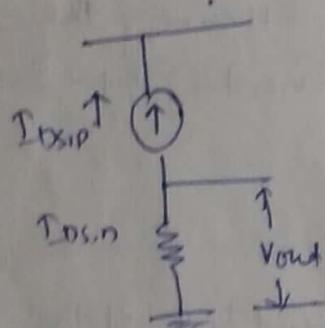
This indicates  $V_{in} = \frac{V_{DD}}{2}$ .

→ In reality, as  $V_{DS}$  increase,  $I_{DS}$  also increases slightly. This region C has a finite slope. In region C, we have two current sources in series, which is an "unstable" condition.

This a small R/P voltage has a large effect at the O/P. This makes the O/P transition very steep. This region defines the gain of the CMOS inverter.

### Region-D

→ This region is described by  $V_{DD}/2 < V_{in} \leq V_{DD} + V_{tp}$ . Here, PMOS is in saturation, while the NMOS is operating in its linear region.



The saturation current for PMOS is obtained as

$$I_{DS,p} = -\frac{K_p}{2} [(V_{in} - V_{DD} - V_{tp})^2]$$

$$I_{DS,n} = \frac{K_n}{2} [2(V_{in} - V_{tn})V_{out} - V_{out}^2]$$

$$I_{DS,p} = -I_{DS,n}$$

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{K_p}{K_n} (V_{in} - V_{DD} - V_{tp})^2}$$

### Region-E:- ( $V_{in} > V_{DD} + V_{tp,p}$ )

This region is defined by the input condition  $V_{in} > V_{DD} + V_{tp,p}$ , the PMOS transistor is cut off ( $I_{DS,p}=0$ ) & NMOS is in linear region.

Here  $V_{GSp} = V_{in} - V_{DD}$  which is more than  $V_{tp}$ .

$$I_{DS,n} = 0, I_{DS,p} = 0, V_{DS,n} = 0$$

The o/p in this region is

$$V_{out} = 0, \text{ i.e. } [V_{OL} = 0]$$

- The nmos & pmos transistors can be seen as nearly ideal switches ie controlled by the input voltage that connect the o/p node to the power supply voltage or to the ground potential depending on the input voltage level.

- The drain current  $I_{D,n}$  of the nmos transistor is a function of the voltages  $V_{GS,n}$  &  $V_{DS,n}$ . Hence - the nmos drain current is also a function of the inverter input & o/p voltages  $V_{in}$  &  $V_{out}$ .

$$I_{D,n} = f(V_{in}, V_{out})$$

- Similarly, the drain current  $I_{D,p}$  of the pmos transistor is also a function of the inverter input & o/p voltages  $V_{in}$  &  $V_{out}$

$$I_{D,p} = f(V_{in}, V_{out})$$

- CMOS Inverter operating in steady state, the drain current of the nmos transistor is always equal to the drain current of the pmos transistor.

$$I_{D,n} = I_{D,p}$$

- Calculation of  $V_{IL}$ : (When  $V_{in}$  is increased beyond  $V_{IO,n}$ )  
→ The slope of VTC is equal to  $(-1)$  i.e.  $\frac{dV_{out}}{dV_{in}} = -1$  when the input

voltage is  $V_{in} = V_{IL}$ . In this case, the nmos transistor operates in saturation while the pmos transistor operates in linear region.

By applying KCL at the O/P node

$$I_{D,n} = I_{D,p}$$

$$\Rightarrow (I_{D,p})_{\text{linear}} = (I_{D,n})_{\text{saturation}}$$

$$\Rightarrow (I_{D,n})_{\text{saturation}} = (I_{D,p})_{\text{linear}}$$

$$\Rightarrow \frac{k_n}{2} (V_{in} - V_{TO,n})^2 = \frac{k_p}{2} [2(V_{out} - V_{DD})]$$

$$\Rightarrow \frac{k_n}{2} (V_{GS,n} - V_{TO,n})^2 = \frac{k_p}{2} [2(V_{GSP} - V_{TO,p})V_{DS,p} - V_{DS,p}^2]$$

$$\Rightarrow \frac{k_n}{2} (V_{in} - V_{TO,n})^2 = \frac{k_p}{2} [2(V_{in} - V_{DD} - V_{TO,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]$$

Differentiating with respect to  $V_{GS,n}$

$$\frac{k_n}{2} \cdot 2 (V_{in} - V_{TO,n}) = \frac{k_p}{2} \left[ 2 \left\{ (V_{in} - V_{DD} - V_{TO,p}) \cdot \frac{dV_{out}}{dV_{in}} + 1 \cdot (V_{out} - V_{DD}) \right\} - 2 (V_{out} - V_{DD}) \cdot \frac{dV_{out}}{dV_{in}} \right]$$

Now we will put  $\frac{dV_{out}}{dV_{in}} = -1$ ,  $V_{in} = V_{IL}$

$$\Rightarrow k_n (V_{in} - V_{TO,n}) = k_p \left[ (V_{in} - V_{DD} - V_{TO,p})(-1) + (V_{out} - V_{DD}) + (V_{out} - V_{DD}) \right]$$

$$\Rightarrow k_n (V_{in} - V_{TO,n}) = k_p \left[ -V_{in} + V_{DD} + V_{TO,p} + V_{out} - V_{DD} + V_{out} - V_{DD} \right]$$

$$\Rightarrow k_n (V_{in} - V_{TO,n}) = k_p \left[ -V_{in} + V_{DD} + V_{TO,p} + 2V_{out} - 2V_{DD} \right]$$

$$\Rightarrow k_n (V_{in} - V_{TO,n}) = k_p \left[ -V_{in} + V_{DD} + V_{TO,p} + 2V_{out} \right]$$

$$\Rightarrow k_n (V_{in} - V_{TO,n}) = k_p \left[ V_{TO,p} - 2V_{out} - V_{in} + V_{TO,p} - V_{DD} \right]$$

$$\Rightarrow k_n (V_{in} - V_{TO,n}) = k_p \left[ 2V_{out} - V_{in} + V_{TO,p} - V_{DD} \right]$$

$$\Rightarrow (V_{in} - V_{TO,n}) = \frac{k_p}{k_n} \left[ 2V_{out} - V_{in} + V_{TO,p} - V_{DD} \right]$$

$$\Rightarrow \frac{k_n}{k_p} (V_{in} - V_{TO,n}) = \left[ 2V_{out} - V_{in} + V_{TO,p} - V_{DD} \right]$$

$$\Rightarrow \frac{k_n}{k_p} V_{in} - \frac{k_n}{k_p} V_{TO,n} + V_{in} = 2V_{out} + V_{TO,p} - V_{DD}$$

$$\Rightarrow V_{in} \left( \frac{k_n}{k_p} + 1 \right) = 2V_{out} + V_{TO,p} - V_{DD} + \frac{k_n}{k_p} V_{TO,n}$$

$$\Rightarrow V_{IL} (K_R + 1) = 2V_{out} + V_{TO,p} - V_{DD} + K_R V_{TO,n}$$

$$\Rightarrow V_{IL} = \frac{2V_{out} + V_{TO,p} - V_{DD} + K_R V_{TO,n}}{1 + K_R}$$

$$K_R = \frac{k_n}{k_p}$$

$$V_{in} = V_{IL}$$

Calculation of  $V_{IH}$   $(V_{out} \text{ falls below } (V_{in} - V_{TO,n}))$

→ when the input voltage is equal to  $V_{IH}$ , the nmos transistor operates in the linear region and the pmos transistor operates in saturation.

By applying KCL at O/p node

$$\Rightarrow (I_{D,n}) = I_{D,p}$$

$$\Rightarrow (I_{D,n})_{\text{linear}} = (I_{D,p})_{\text{saturation}}$$

$$\Rightarrow \frac{K_n}{2} \left[ 2(v_{GS,n} - v_{TO,n}) \cdot v_{DS,n} - v_{DS,n}^2 \right] = \frac{k_p}{2} (v_{GS,p} - v_{TO,p})^2$$

put  $v_{GS,n} = v_{in}$

$$v_{DS,n} = v_{out}$$

$$v_{GS,p} = v_{in} - V_{DD}$$

$$\Rightarrow \frac{K_n}{2} \left[ 2(v_{in} - v_{TO,n}) v_{out} - v_{out}^2 \right] = \frac{k_p}{2} (v_{in} - V_{DD} - v_{TO,p})^2$$

Now differentiating w.r.t  $v_{in}$

$$\Rightarrow \frac{K_n}{2} \left[ 2 \left\{ (v_{in} - v_{TO,n}) \frac{dv_{out}}{dv_{in}} + 1 \cdot v_{out} \right\} - 2 v_{out} \cdot \frac{dv_{out}}{dv_{in}} \right]$$

$$= \frac{k_p}{2} \left[ 2 (v_{in} - V_{DD} - v_{TO,p}) \right]$$

Now put  $\frac{dv_{out}}{dv_{in}} = -1$

$$\Rightarrow K_n \left[ ((v_{in} - v_{TO,n})(-1) + v_{out}) - 2 v_{out} (-1) \right]$$

$$= k_p [v_{in} - V_{DD} - v_{TO,p}]$$

$$\Rightarrow K_n \left[ -v_{in} + v_{TO,n} + v_{out} + v_{out} \right] = k_p [v_{in} - V_{DD} - v_{TO,p}]$$

$$\Rightarrow K_n \left[ -v_{in} + v_{TO,n} + 2 v_{out} \right] = k_p [v_{in} - V_{DD} - v_{TO,p}]$$

$$\Rightarrow \frac{K_n}{k_p} \left[ -v_{in} + v_{TO,n} + 2 v_{out} \right] = [v_{in} - V_{DD} - v_{TO,p}]$$

put  $v_{in} = V_{IH}$  &  $\frac{K_n}{k_p} = KR$

$$\Rightarrow KR \left[ -V_{IH} + v_{TO,n} + 2 v_{out} \right] = [V_{IH} - V_{DD} - v_{TO,p}]$$

$$\Rightarrow KR [V_{T0,n} + 2V_{out}] = V_{IH} - V_{DD} - V_{TO,P} + KR V_{IH}$$

$$\Rightarrow KR [V_{T0,n} + 2V_{out}] = KR V_{IH} [1 + KR] - V_{DD} - V_{TO,P}$$

$$\Rightarrow V_{IH} [1 + KR] = KR [V_{T0,n} + 2V_{out}] + V_{DD} + V_{TO,P}$$

$$\Rightarrow V_{IH} = \frac{V_{DD} + V_{TO,P} + KR (2V_{out} + V_{T0,n})}{1 + KR}$$

Calculation of  $V_{th}$  ( $V_{in} = V_{th}$ ) (regime C)  $V_{out} \approx V_{in} - V_{TO,P}$   
 $V_{out} = V_{in} - V_{T0,n}$

- The inverter threshold voltage is defined as  $V_{th} = V_{in} - V_{out}$ . Since the CMOS Inverter exhibits large noise margin & very sharp VTC transition,
- For  $V_{in} = V_{out}$ , both transistors are expected to be in saturation mode.

$$(I_{D,n})_{\text{saturation}} = (I_{D,P})_{\text{saturation}}$$

$$\Rightarrow \frac{Kn}{2} (V_{Gsn} - V_{T0,n})^2 = \frac{Kp}{2} (V_{Gsp} - V_{TO,P})^2$$

$$\text{put } V_{Gsn} = V_{in}$$

$$V_{Gsp} = V_{in} - V_{DD}$$

$$\Rightarrow \frac{Kn}{2} (V_{in} - V_{T0,n})^2 = \frac{Kp}{2} (V_{in} - V_{DD} - V_{TO,P})^2$$

$$\Rightarrow \sqrt{\frac{Kn}{2}} (V_{in} - V_{T0,n})^2 = Kp (V_{in} - V_{DD} - V_{TO,P})^2$$

Taking the square root on both sides,

$$\sqrt{K_n} (V_{in} - V_{TO,n}) = \pm \sqrt{K_p} (V_{in} - V_{DD} - V_{TO,p})$$

$$\Rightarrow \sqrt{K_n} (V_{in} - V_{TO,n}) = - \sqrt{K_p} (V_{in} - V_{DD} - V_{TO,p})$$

$$\Rightarrow (V_{in} - V_{TO,n}) = - \sqrt{\frac{K_p}{K_n}} (V_{in} - V_{DD} - V_{TO,p})$$

$$\Rightarrow V_{in} - V_{TO,n} = - \sqrt{\frac{K_p}{K_n}} V_{in} + \sqrt{\frac{K_p}{K_n}} (V_{DD} + V_{TO,p})$$

$$\Rightarrow V_{in} + \sqrt{\frac{K_p}{K_n}} V_{in} = \sqrt{\frac{K_p}{K_n}} (V_{DD} + V_{TO,p}) + V_{TO,n}$$

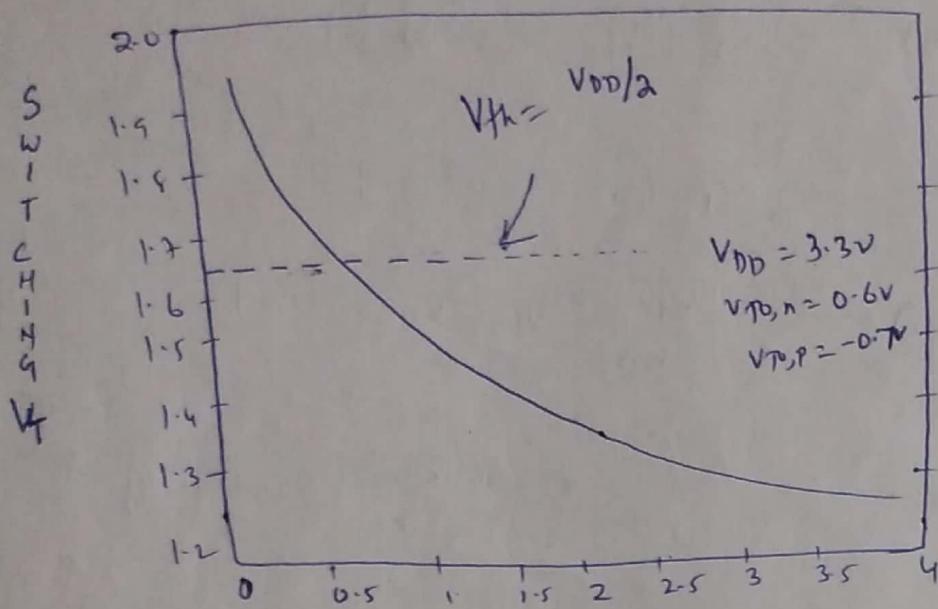
$$\Rightarrow V_{in} \left( 1 + \sqrt{\frac{K_p}{K_n}} \right) = V_{TO,n} + \sqrt{\frac{K_p}{K_n}} (V_{DD} + V_{TO,p})$$

$$\Rightarrow V_{in} = \frac{V_{TO,n} + \sqrt{\frac{K_p}{K_n}} (V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{K_p}{K_n}}}$$

$$\frac{K_n}{K_p} = K_R \quad ; \quad \frac{1}{K_R} = \frac{K_p}{K_n}$$

$$\Rightarrow V_{in} = \frac{V_{TO,n} + \sqrt{\frac{1}{K_R}} (V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{1}{K_R}}}$$

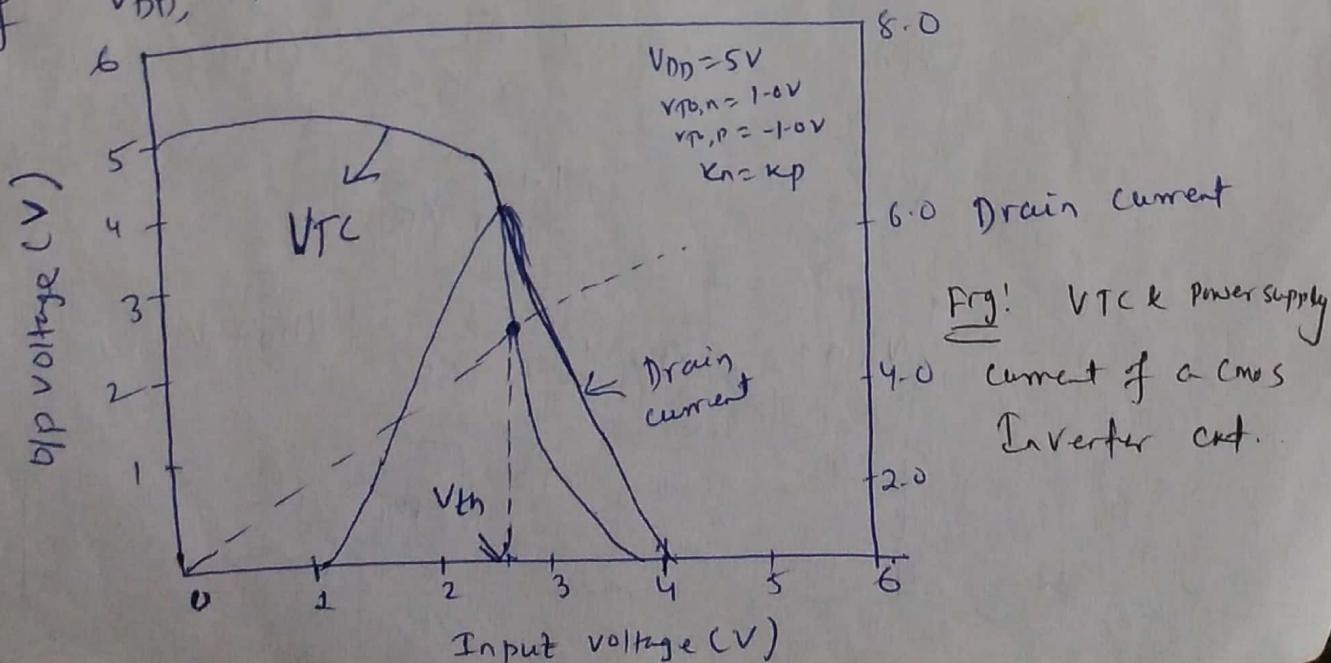
$$\Rightarrow V_{th} = \frac{V_{TO,n} + \sqrt{\frac{1}{K_R}} (V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{1}{K_R}}}$$



$$\text{Transconductance ratio } K_R = \frac{K_n}{K_p}$$

Fig: Variation of the inversion threshold voltage as a function of  $K_R$ .

- Inverter threshold voltage is defined as  $V_{th} = V_{in} = V_{out}$ . When the i/p voltage is equal to  $V_{th}$ , o/p voltage can actually attain any value between  $(V_{th} - V_{T0,n})$  &  $(V_{th} - V_{T0,p})$ .
- The inverter switching threshold voltage  $V_{th}$  as a function of transconductance ratio  $K_R$  and for fixed values of  $V_{DD}$ ,  $V_{T0,n}$ , &  $V_{T0,p}$ .



①  
 → CMOS Inverter does not draw any significant current from the power source, except for small leakage & subthreshold currents, when the input voltage is either smaller than  $V_{TO,n}$  or larger than  $(V_{DD} + V_{TO,p})$ .

- The NMOS & PMOS transistors conduct a nonzero current during low-to-high & high-to-low transitions i.e. Region B, C, & D.
- Current being drawn from the power supply source during transition reaches its peak value when  $V_{in} = V_{th}$  i.e. Max<sup>m</sup> current is drawn when both transistors are operating in Saturating Node.

### Design of CMOS Inverter:-

- The CMOS inverter swings between 0 to  $V_{DD}$  and the noise margins are relatively wide.
- The problem of designing a CMOS inverter can be reduced to setting the inverter threshold to a desired voltage value.
- The value of  $K_R$  can be found out by using power supply voltage, the NMOS & PMOS transistor threshold voltages & desired inverter threshold voltage  $V_{th}$ .

We know that

$$V_{th} = \frac{V_{TO,n} + \sqrt{K_R(V_{DD} + V_{TO,p})}}{1 + \sqrt{K_R}}$$

$$\begin{aligned} V_{th}(1 + \sqrt{K_R}) &= V_{TO,n} + \sqrt{K_R(V_{DD} + V_{TO,p})} \\ &= V_{TO,n} + \sqrt{K_R} V_{DD} + \sqrt{K_R} V_{TO,p} \end{aligned}$$

$$V_{th} + V_{TO} \sqrt{\frac{1}{KR}} = V_{TO,n} + \sqrt{\frac{1}{KR}} V_{DD} + \sqrt{\frac{1}{KR}} V_{TO,p}$$

$$\begin{aligned} V_{th} - V_{TO,n} &= \sqrt{\frac{1}{KR}} V_{DD} + \sqrt{\frac{1}{KR}} V_{TO,p} - V_{th} \sqrt{\frac{1}{KR}} \\ &= \sqrt{\frac{1}{KR}} (V_{DD} + V_{TO,p} - V_{th}) \end{aligned}$$

$$\sqrt{\frac{1}{KR}} = \frac{V_{th} - V_{TO,n}}{V_{DD} + V_{TO,p} - V_{th}}$$

Squaring both sides, then we will get

$$\frac{1}{KR} = \left( \frac{V_{th} - V_{TO,n}}{V_{DD} + V_{TO,p} - V_{th}} \right)^2$$

$$KR = \frac{V_{th}^2}{\left( \frac{V_{DD} + V_{TO,p} - V_{th}}{V_{th} - V_{TO,n}} \right)^2}$$

$$KR = \frac{k_n}{k_p} = \left( \frac{V_{DD} + V_{TO,p} - V_{th}}{V_{th} - V_{TO,n}} \right)^2 \quad \text{--- (1)}$$

For an ideal inverter switching threshold voltage is defined as

$$V_{th,ideal} = \frac{V_{DD}}{2}$$

Now putting the value of  $V_{th,ideal}$  in eqn(1)

$$\left[ \left( \frac{k_n}{k_p} \right)_{ideal} = \left( \frac{0.5V_{DD} + V_{TO,p}}{0.5V_{DD} - V_{TO,n}} \right)^2 \right] \quad \text{--- (2)}$$

→ The operations of the nmos & the pmos transistors of the CMOS inverter are fully complementary, we can achieve completely symmetric input-output characteristics by setting the threshold voltages as  $V_{TO} = V_{TO,n} = |V_{TO,p}|$ . So eqn(2) can reduced to

$$V_{TO,n} = -V_{TO,p}$$

$$\left(\frac{K_n}{K_p}\right)_{\text{symmetric}} = \left(\frac{0.5 V_{DD} + V_{TO,p}}{0.5 V_{DD} + V_{TO,p}}\right)^2 = 1^2 = 1$$

$$\boxed{\left(\frac{K_n}{K_p}\right)_{\text{symmetric}} = 1}$$

$$\therefore \frac{K_n}{K_p} = \frac{k_n \operatorname{con}(\frac{w}{l})_n}{k_p \operatorname{con}(\frac{w}{l})_p} = \frac{k_n (\frac{w}{l})_n}{k_p (\frac{w}{l})_p}$$

$$1 = \frac{k_n (\frac{w}{l})_n}{k_p (\frac{w}{l})_p}$$

$$k_n (\frac{w}{l})_n = k_p (\frac{w}{l})_p$$

$$\frac{k_n (\frac{w}{l})_n}{(\frac{w}{l})_p} = \frac{k_p}{k_n} \approx \frac{230 \text{ cm}^2/\text{V.s}}{580 \text{ cm}^2/\text{V.s}} = \frac{1}{2.5}$$

$$\frac{(\frac{w}{l})_n}{(\frac{w}{l})_p} = \frac{1}{2.5}$$

$$\boxed{K_n = 2.5 K_p}$$

Hence

$$\boxed{(\frac{w}{l})_p \approx 2.5 (\frac{w}{l})_n}$$

→  $K_n$ ,  $k$   $K_p$  values will vary with surface doping concentration of the substrate & the tub.

## Symmetric CMOS Inverter:-

For a symmetric CMOS inverter with  $V_{TO,n} = |V_{TO,p}|$  &  $K_R = K_P$

$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{TO,n})$$

$$V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{TO,n})$$

→ sum of  $V_{IL}$  &  $V_{IH}$  is always equal to  $V_{DD}$  in a symmetric inverter.

$$V_{IL} + V_{IH} = V_{DD}$$

$$\begin{aligned} N_{ML} &= V_{IL} - V_{OH} \\ &= V_{IL} - 0 \end{aligned}$$

$$N_{ML} = V_{IL}$$

$$\begin{aligned} N_{MH} &= V_{OH} - V_{IH} \\ &= V_{DD} - V_{IH} \end{aligned}$$

$$N_{MH} = V_{DD} - V_{IH}$$

$$N_{MH} = V_{IL} + V_{IH} - V_{IH} = V_{IL}$$

So

$$N_{MH} = N_{ML} = V_{IL}$$

- N.B: → CMOS inverter does not conduct a significant amount of current during a switching event i.e. when the output voltage changes from a low to high state or from a high to low state.
- Overall power consumption is less in CMOS inverter as compared to other inverter ckt.

## Asymmetric CMOS Inverter

①

$$K_R \neq 1$$

$$K_n \neq K_P$$

$$k_{nL} \operatorname{cos}(\omega/L)_n \neq k_{pL} \operatorname{cos}(\omega/L)_P$$

$$V_{OH} = V_{DD}, \quad V_{OL} = 0$$

②

$$V_{IL} = \frac{2V_{out} + V_{t_{p,n}} - V_{DD} + K_R V_{t_{n,p}}}{1 + K_R}$$

$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{t_{p,n}})$$

$$V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{t_{p,n}})$$

$$V_{IH} = \frac{V_{DD} + V_{t_{p,n}} + K_R (2V_{out} + V_{t_{p,n}})}{1 + K_R}$$

④

$$V_{t_{p,n}} \neq V_{t_{p,p}}$$

$$V_{t_{p,n}} = |V_{t_{p,p}}|$$

⑤

$$V_{th} = \frac{V_{t_{p,n}} + \sqrt{K_R} (V_{DD} + V_{t_{p,p}})}{1 + \sqrt{K_R}}$$

$$V_{th} = \frac{V_{DD}}{2}$$

⑥

$$N_{ML} = V_{IL} - V_{OL}$$

$$N_{ML} = V_{IL} - V_{OL}$$

$$N_{MH} = V_{OH} - V_{IH}$$

$$N_{MH} = N_{ML} = V_{IL}$$

⑦

$V_{th}$  is a function of  $K_R$  & fixed values  
of  $V_{DD}$ ,  $V_{t_{p,n}}$  &  $V_{t_{p,p}}$

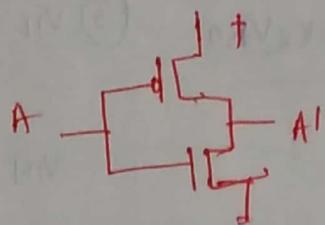
⑧  $V_{th}$  is a function of  
only supply voltage  
 $V_{DD}$

Q. 2011  
EE8

Design a CMOS inverter so that noise margin Low ( $N_{ML}$ )  
= Noise Margin High ( $N_{MH}$ ) =  $V_{IL}$ .

Q. 2012

Consider the device built from two CMOS transistors shown  
in the figure. Briefly describe its function & performance  
& how it works.



Ans

$V_{in} < V_{to,n} \rightarrow$  NMOS off, PMOS on  $\Rightarrow V_{out} = V_{DD} \rightarrow$  logic 1

$V_{in} > V_{DD} + V_{tp,p} \rightarrow$  NMOS on, PMOS off  $\Rightarrow V_{out} = 0 \rightarrow$  logic 0

Q. 2013

A logic gate has  $V_{OH} = 5V$ ,  $V_{OL} = 0.2V$ ,  $V_{IH} = 0.5V$  &  $V_{IL} = 0.8V$ . Calculate the Noise Margins.

Soln!

$$V_{OH} = 5V, V_{OL} = 0.2V, V_{IH} = 0.5V, V_{IL} = 0.8V$$

$$N_{ML} = V_{IL} - V_{OL} = 0.8V - 0.2V = 0.6V$$

$$N_{MH} = V_{OH} - V_{IH} = 5 - 0.5V = 4.5V$$

Q. 2013  
2019

What is the minimum power supply voltage required for a CMOS inverter so that it can operate properly?

Xm

$$V_{DD}^{min} = V_{to,n} + |V_{tp,p}|$$

Consider a CMOS inverter circuit with the following parameters:

$$V_{DD} = 3.3V, V_{t0,n} = 0.6V, V_{t0,p} = -0.7V, K_n = 200 \mu A/V^2$$

$$K_p = 80 \mu A/V^2$$

Calculate the Noise Margins of the CMOS.

$$K_n = 200 \mu A/V^2$$

$$K_p = 80 \mu A/V^2$$

$$\frac{K_n}{K_p} = 2.5 \Rightarrow K_R \neq 1 \quad (\text{Asymmetric CMOS Inverter})$$

$$V_{OL} = 0$$

$$V_{OH} = V_{DD} = 3.3V$$

$$V_{IL} = \frac{2V_{out} + V_{t0,p} - V_{DD} + K_R V_{t0,n}}{1 + K_R}$$

$$= \frac{2V_{out} - 0.7 - 3.3 + 2.5 \times 0.6}{1 + 2.5}$$

$$= 0.57V_{out} - 0.71$$

for  $V_{IL}$  calculation NMOS is in saturation & PMOS is in linear.

$$\frac{K_n}{K_p} [V_{in} - V_{t0,n}]^2 = \frac{K_p}{2} [2(V_{gs,p} - V_{t0,p})V_{ds,p} - V_{ds,p}^2]$$

$$2.5 [V_{in} - V_{t0,n}]^2 = 2 [(V_{in} - V_{DD} - V_{t0,p})(V_{nf} - V_{DD}) - (V_{nf} - V_{DD})^2]$$

$$2.5 [(V_{IL} - V_{t0,n})^2] = 2 [(V_{IL} - V_{DD} - V_{t0,p})(V_{nf} - V_{DD}) - (V_{nf} - V_{DD})^2]$$

$$2.5 [(0.57V_{nf} - 0.71 - 0.6)^2] = 2 [(0.57V_{nf} - 0.71 - 3.3 + 0.7)(V_{nf} - 3.3) - (V_{nf} - 3.3)^2]$$

$$V_{out} = 3.14 \text{ V}$$

$$V_{IL} = 0.57 V_{out} - 0.71$$

$$= 0.57 \times 3.14 - 0.71 = 1.08 \text{ V}$$

$V_{IH}$

$$V_{IH} = \frac{V_{DD} + V_{to,p} + KR(2V_{out} + V_{to,n})}{1+KR}$$

$$= \frac{3.3 - 0.7 + 2.5(2V_{out} + 0.6)}{1+2.5}$$

$$= 1.43 V_{out} + 1.17$$

for  $V_{IH}$  calculation nmos linear & pmos saturation

$$\frac{k_n}{2} [2(V_{in} - V_{to,n})V_{DS,n} - V_{DS,n}^2] = \frac{k_p}{2} [V_{GS,p} - V_{to,p}]^2$$

$$2.5 [2(V_{IH} - V_{to,n})V_{out} - V_{out}^2] = (V_{in} - V_{DD} - V_{to,p})^2$$

$$2.5 [2(V_{IH} - V_{to,n})V_{out} - V_{out}^2] = (V_{IH} - V_{DD} - V_{to,p})^2$$

$$2.5 [2(1.43 V_{out} + 1.17 - 0.6)V_{out} - V_{out}^2] = (1.43 V_{out} + 1.17 - 3.3 + 0.7)^2$$

$$\boxed{V_{out} = 0.27 \text{ V}}$$

$$V_{IH} = 1.43 V_{out} + 1.17$$

$$= 1.43 \times 0.27 + 1.17 = 1.55 \text{ V}$$

$$NML = V_{IL} - V_{OL} = 1.08 \text{ V}$$

$$NMH = V_{OH} - V_{IH}$$

$$= 3.3 - 1.55$$

$$\boxed{NMH = 1.75 \text{ V}}$$

Calculate the Noise Margin of a CMOS Inverter with

$$V_{DD} = 5V, V_{t_{n,p}} = 1V, V_{t_{p,n}} = -1V, K_n = K_p = 2 \text{ nA/V}^2$$

Ans!

$$V_{DD} = 5V, V_{t_{n,p}} = 1V, V_{t_{p,n}} = -1V,$$

$$K_n = K_p = 2 \text{ nA/V}^2 \quad (\text{so it is symmetric CMOS Inverter})$$

$$\boxed{V_{OH} = V_{DD} = 5V}$$

$$\boxed{V_{OL} = 0}$$

$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{t_{p,n}})$$

$$= \frac{1}{8} (2 \times 5 + 2 \times 1) = \frac{17}{8} = 2.125V$$

$$V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{t_{n,p}})$$

$$= \frac{1}{8} (5 \times 5 - 2 \times 1) = \frac{23}{8} = 2.875V$$

$$N_{mL} = 2.125V$$

$$N_{mH} = V_{OH} - V_{IH} = 5 - 2.875V$$

$$= 2.125V$$

$$\boxed{N_{mL} = N_{mH} = 2.125V}$$

for a symmetric CMOS Inverter with  $V_{t_{n,p}} = V_{t_{p,n}}$  &  $K_n = K_p = 1$ .

Q210 Write the expression for  $V_{IL}$  &  $V_{IH}$  in terms of  $V_{DD}$  &  $V_{t_0}$ .

Soln:

$$V_{t_{n,p}} = 1V_{t_{p,n}}, K_n = K_p = 1$$

$$\boxed{V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{t_{p,n}})}$$

$$\boxed{V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{t_{n,p}})}$$

Q Discuss the operation of CMOS inverter by drawing its  
& derive the expression for its switching threshold voltage  
& show that for a symmetric inverter ( $L_p = L_n$ )  $V_t = 2.5V$

Sol:

Q 2001

In a CMOS inverter the upper MOSFET is

- (a) A passive load
- (b) An active load
- (c) depth of the channel
- (d) none of the above

Q 2002

for a CMOS inverter when  $V_{DD} = V_{TH}$

- (a) the NMOS transistor will be in cut-off while PMOS transistor will be in saturation
  - (b) the NMOS transistor will be in linear region while PMOS transistor will be in saturation
  - (c) the NMOS transistor will be in saturation while the PMOS transistor will be in linear region
  - (d) both the NMOS & PMOS transistors will be in saturation
- Q The high O/P of a CMOS digital circuit is usually
- (a)  $V_{DD}/2$
  - (b)  $V_{GS}$
  - (c)  $V_{DS}$
  - (d)  $V_{DD}$

Q. 2006 In a CMOS inverter if the MOSFET are having  $|V_t| = 1V$ , find  
 $V_{IL}$ ,  $V_{IH}$  & Noise Margins if  $V_{DD} = 10V$

$$V_{TH} = 1V, V_{DD} = 10V$$

$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{TH,n})$$

$$= \frac{1}{8} (3 \times 10 + 2 \times 1) = 4V$$

$$V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{TH,n})$$

$$= \frac{1}{8} (5 \times 10 - 2 \times 1) = \frac{48}{8} = 6V$$

$$N_{ML} = V_{IL} - V_{OL}^{\infty} = 4V$$

$$N_{MH} = V_{OH} - V_{IH} = 10 - 6V = 4V$$

$$\boxed{N_{ML} = N_{MH} = 4V}$$

Q1.5.b

Consider a CMOS inverter with the following parameters:

nMOS  $V_{TH,n} = 0.6V$   $K_{n,ON} = 60 \text{ mA/V}^2$   $(W/L)_n = 8$

pMOS  $V_{TH,p} = -0.7V$   $K_{p,ON} = 25 \text{ mA/V}^2$   $(W/L)_p = 12$

Calculate the noise margin & switching threshold voltage ( $V_{TH}$ ) of this ckt. The power supply voltage is  $V_{DD} = 3.3V$

Soln!

$$K_n = K_{n,ON} (W/L)_n = 60 \times 8 \text{ mA/V}^2$$

$$= 480 \text{ mA/V}^2$$

$$K_p = K_{p,ON} (W/L)_p = 25 \text{ mA/V}^2 \times 12$$

$$= 300 \text{ mA/V}^2$$

$$\frac{K_n}{K_p} = \frac{480}{300} = \frac{8}{5} = 1.6$$

$\frac{K_n}{K_p} \neq 1$  (So it is Asymmetric CMOS Inverter)