

CS 577: Project Report

| | |
|---------------------------------|---|
| <i>Project Number :</i> | 17 |
| Group Number: | 19 |
| <i>Name of the top modules:</i> | Crypto_sign |
| <i>Link for GitHub Repo:</i> | https://github.com/PrachiS24/optimized_project17.git |

| Group Members | Roll Numbers |
|--------------------|--------------|
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| Sakshi Sharma | 194101042 |

Date: 15.05.2020

INTRODUCTION

The project aimed at understanding high level synthesis(HLS), and the steps involved in the process. It also comprises of learning the use of the software suite Vivado, for the same. This report consists of explanations and results of the several steps involved in performing optimization on the code provided, with the help of the Vivado software.

HLS is an automated design process that compiles a high level description of a design into a RTL implementation keeping in mind the specific constraints. HLS input is an untimed data flow and is specified in languages like C, C++ etc. The output of the HLS may include RTL implementation, Analysis feedback etc.. HLS is used to identify and extract parallelism and optimize the code according to various optimization goals. Major benefit of HLS is that it allows designing at a high level of abstraction.

Vivado is a software tool for synthesis and analysis of hardware designs. We can perform HLS using this software tool. Vivado high level synthesis can compile C programs directly into RTL with the need for doing it manually.

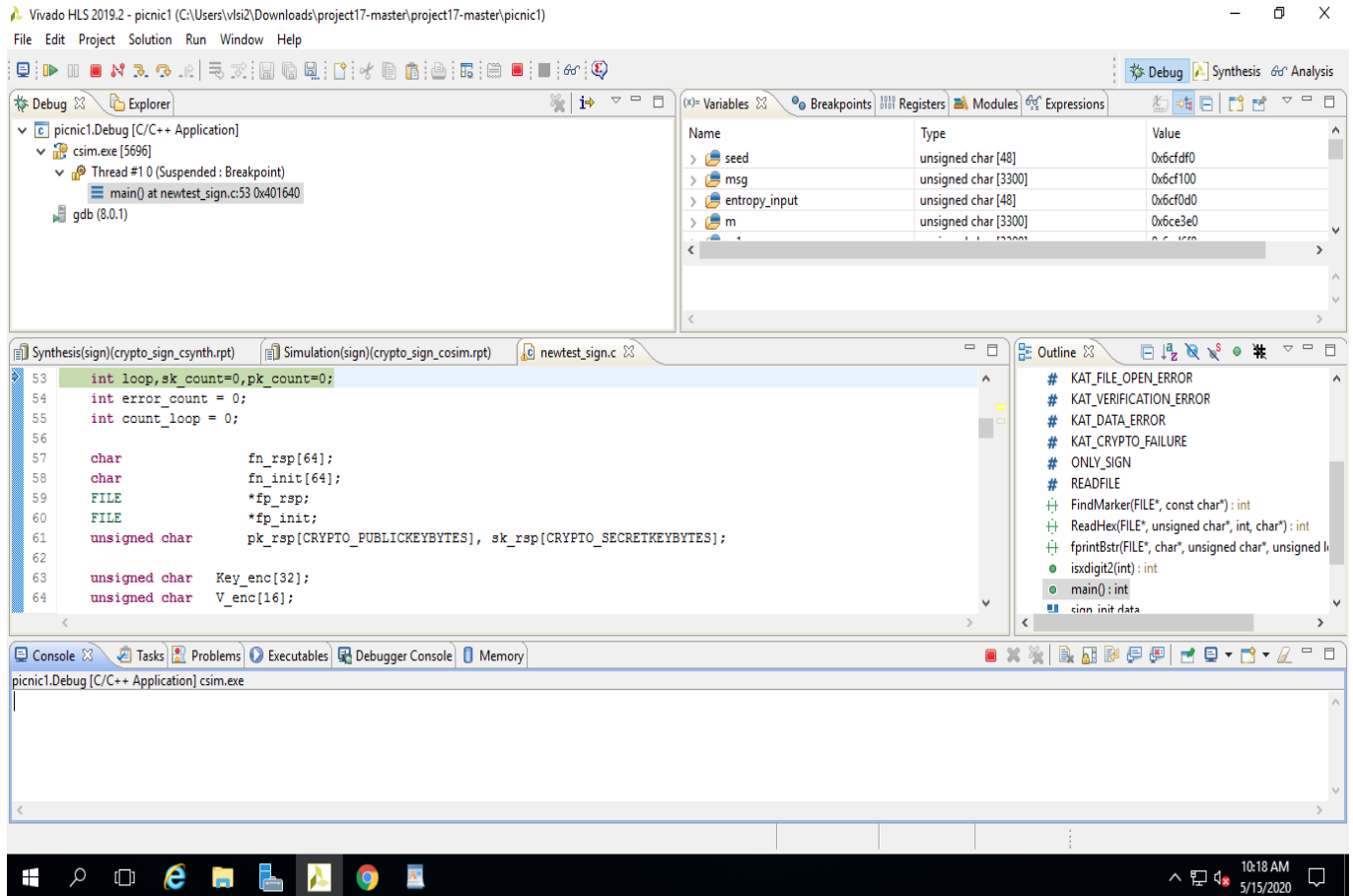
The major steps in the project includes importing the code (“picnic” , in our case) from github to the Vivado IDE and perform simulation ,synthesis and RTL simulation on the code. Initially, area utilization for the project was greater than 100% (103%). We have applied resource and area optimization techniques using various directives in VIVADO. Area and latency utilization were significantly reduced after using various directives.

We get reports after each of these operations using which we perform optimizations in order to make our code more efficient and faster. The report consists of these reports and the results of these operations in a tabular form. We identify the areas where we can perform optimizations for getting more efficient results. These optimizations and its details are also enlisted in phase two of the results.

PHASE-1

- Running the algorithm

1.1 Simulation screenshot



1.2 Synthesis screenshot

Vivado HLS 2019.2 - picnic1 (C:\Users\vlsi2\Downloads\project17-master\project17-master\picnic1)

File Edit Project Solution Window Help

Explorer

- aes.c
- api.c
- hash.c
- KeccakHash.c
- KeccakP-1600-reference.c
- KeccakSpongeWidth1600.c
- lowmc_constants.c
- picnic_impl.c
- picnic_types.c
- picnic.c
- picnic2_impl.c
- rng.c
- tree.c
- Test Bench
- sign
 - constraints
 - directives.tcl
 - script.tcl
 - csim
 - build
 - report
 - impl
 - sim
 - autowrap
 - report
 - crypto_sign_cosim
 - verilog
 - tv
 - verilog
 - wrapc
 - wrapc_pc
 - syn

Synthesis(sign)(crypto_sign_csynth.rpt)

Simulation(sign)(crypto_sign_cosim.rpt)

Debug Synthesis Analysis

Outline Directive

Directive View is not available.

Date: Thu May 14 05:01:21 2020
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: picnic1
Solution: sign
Product family: artix7
Target device: xc7a200t-fbg676-2

Performance Estimates

Timing

Summary

| Clock | Target | Estimated | Uncertainty |
|--------|----------|-----------|-------------|
| ap_clk | 10.00 ns | 8.750 ns | 1.25 ns |

Latency

Summary

| Latency (cycles) | Latency (absolute) | Interval (cycles) |
|------------------|--------------------|-------------------|
|------------------|--------------------|-------------------|

Console

Errors Warnings DRCs

Vivado HLS Console

```
INFO: [RMS 210-278] Implementing memory 'picnic_sign_sig_OOgC_ram (RAM)' using block RAMs.  
INFO: [RTMG 210-278] Implementing memory 'picnic_sign_sig_ONgs_ram (RAM)' using block RAMs.  
INFO: [RTMG 210-278] Implementing memory 'picnic_sign_sig_OOgC_ram (RAM)' using block RAMs.  
INFO: [RTMG 210-278] Implementing memory 'picnic_sign_sig_OPgM_ram (RAM)' using distributed RAMs.  
INFO: [RTMG 210-278] Implementing memory 'picnic_sign_temp_ram (RAM)' using distributed RAMs.  
INFO: [RTMG 210-278] Implementing memory 'crypto_sign_secreRg6_ram (RAM)' using distributed RAMs.  
INFO: [HLS 200-111] Finished generating all RTL models Time (s): cpu = 01:18:48 ; elapsed = 01:23:02 . Memory (MB): peak = 930.730 ; gair  
INFO: [VHDL 208-304] Generating VHDL RTL for crypto_sign.  
INFO: [VLOG 209-307] Generating Verilog RTL for crypto_sign.  
INFO: [HLS 200-112] Total elapsed time: 4982.4 seconds; peak allocated memory: 692.743 MB.  
Finished C synthesis.
```

Windows taskbar: 10:15 AM 5/15/2020

1.3 C/RTL co-simulation screenshot

Vivado HLS 2019.2 - picnic1 (C:\Users\vlsi2\Downloads\project17-master\project17-master\picnic1)

File Edit Project Solution Window Help

Debug Synthesis Analysis

Explorer

- Includes
 - Source
 - aes.c
 - api.c
 - hash.c
 - KeccakHash.c
 - KeccakP-1600-reference.c
 - KeccakSpongeWidth1600.c
 - lowmc_constants.c
 - picnic_impl.c
 - picnic_types.c
 - picnic.c
 - picnic2_impl.c
 - rng.c
 - tree.c
- Test Bench
 - sign
 - constraints
 - directives.tcl
 - script.tcl
 - csim
 - build
 - report
 - impl
 - sim
 - autowrap
 - report
 - crypto_sign_cosim
 - verilog
 - tv
 - verilog
 - wrapc

Synthesis(sign)(crypto_sign_csynth.rpt) Simulation(sign)(crypto_sign_cosim.rpt)

Cosimulation Report for 'crypto_sign'

Result

| RTL | Status | Latency | | | Interval | | |
|---------|--------|-----------|-----------|-----------|----------|-----|-----|
| | | min | avg | max | min | avg | max |
| VHDL | NA | NA | NA | NA | NA | NA | NA |
| Verilog | Pass | 147314213 | 147314213 | 147314213 | NA | NA | NA |

Export the report(.html) using the [Export Wizard](#)

Directive View is not available.

Console

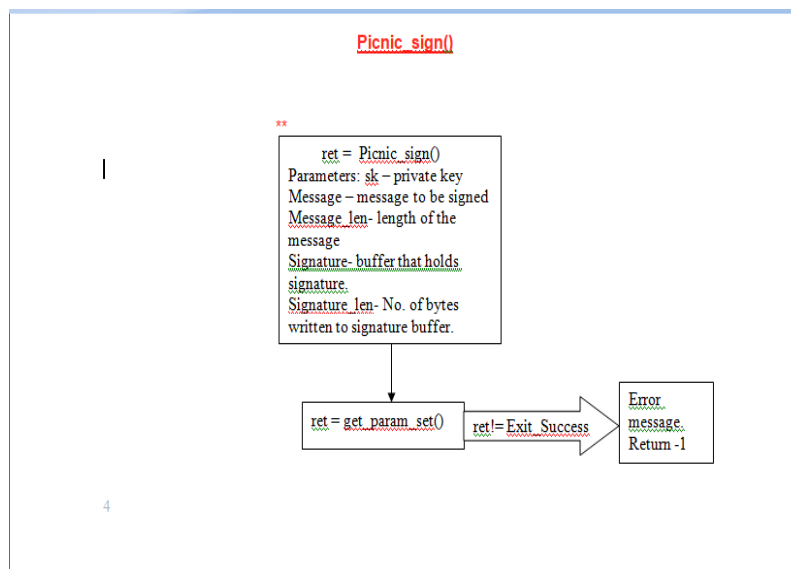
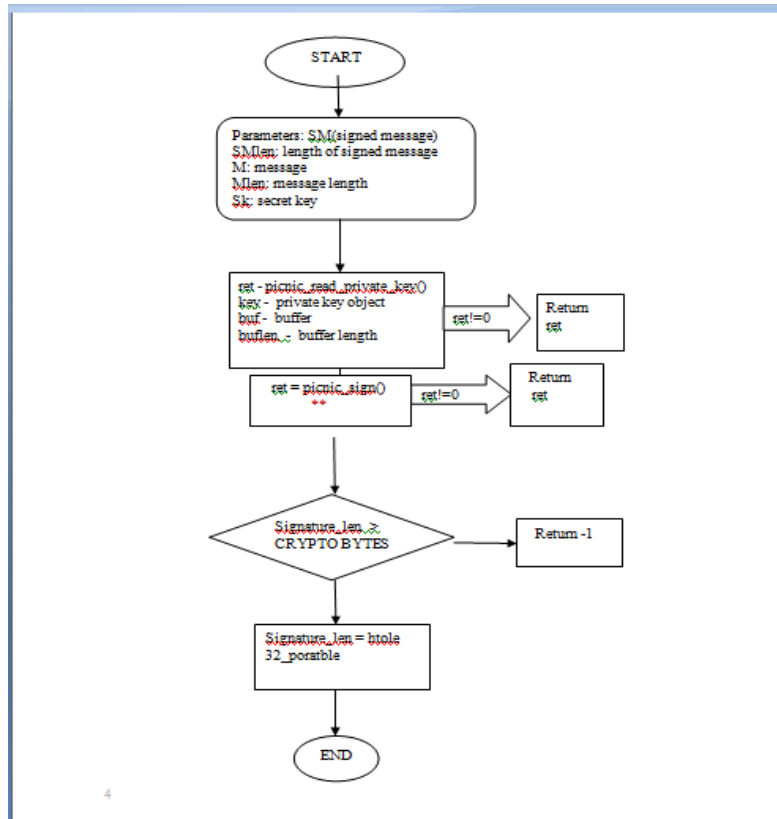
Vivado HLS Console

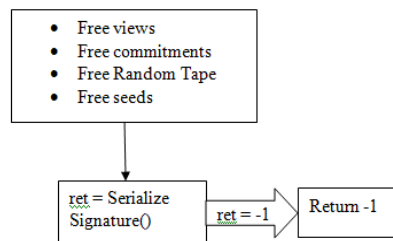
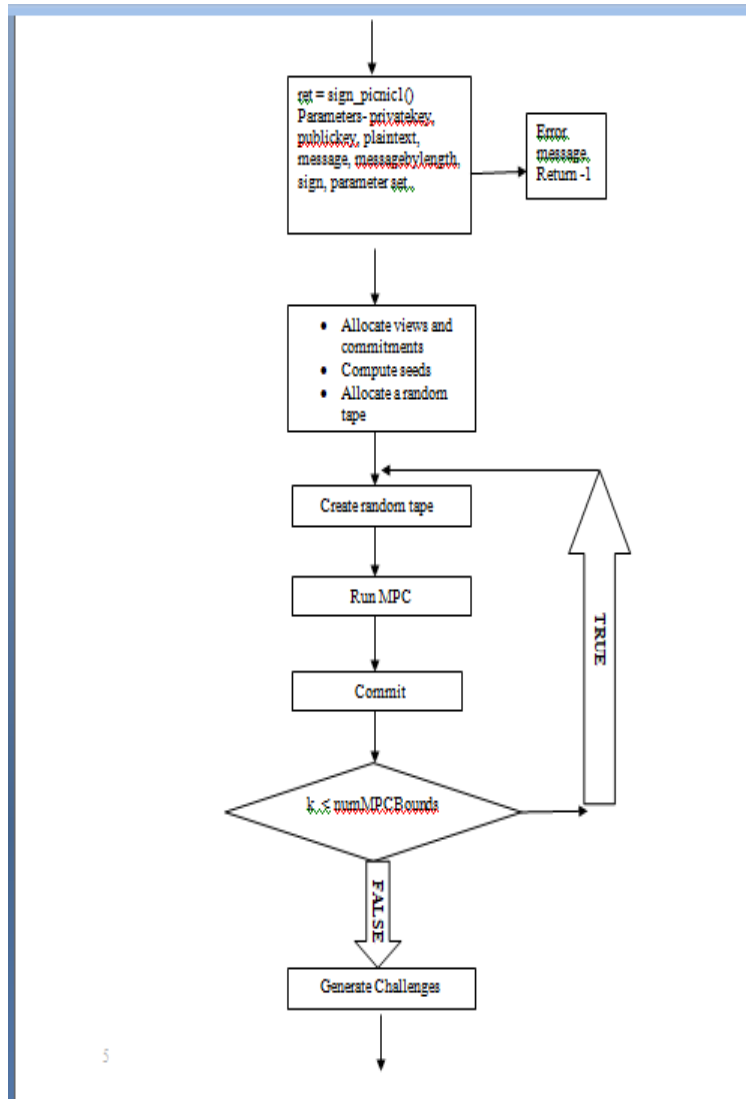
```
run: Time (s): cpu = 00:00:02 ; elapsed = 27:11:53 . Memory (MB): peak = 242.188 ; gain = 4.082
## quit
INFO: [Common 17-206] Exiting xsim at Fri May 15 08:28:21 2020...
INFO: [COSIM 212-316] Starting C post checking ...
Known Answer Tests PASSED.

INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-211] II is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as
Finished C/RTL cosimulation.
```

10:08 AM 5/15/2020

- Flowchart (Give the flowchart of the function used. Describe basic understanding of the algorithm)





The `crypto_sign` function is the top function. It basically adds a signature to the beginning of the message `m` by making use of the secret key `sk`. The `picnic_write_private_key` serialisers the private key. It returns the number of bytes written. The `picnic_sign` function is the signature function. Given the key-pair, it signs a message with it

`picnic_sign` calls a number of functions to achieve this. Some major functions among them are `get_param_set`, `sign_picnic1` which actually does most of the tasks such as allocating views and commitments, computing seeds, allocation random tape. `createRandomTape`, `runMPC`, `commit`, these functions are a part of a loop.

For each iteration compute random tapes, simulate the MPC protocol to compute the LowMC which consists of a number of XOR and matrix multiplication operations, and finally we store the shares in the views. And then we form commitments.

Next we compute challenges with the function `H3`, which is a hash function. It hashes the output shares, commitments, public key and the message. Lastly `SerializeSignature()` serialises the signature into a byte array, encoding the signature. Signature length must be at most `CRYPTOBYTES`. If greater than that, the function returns -1. Else signature length is set by calling the function `htole32_portable`.

- **Result**

| FPGA Part | Name of Top Module | FF | LUT | BRAM | DSP | Latency | II |
|-----------------|--------------------|------------|-------------|----------|--------|----------|----|
| xc78200tfbg76-2 | crypto_sign | 46135(17%) | 104855(77%) | 468(64%) | 5(~0%) | 95602574 | |

3.1 Explain the result

Initially, the area utilization of the project was 103% for LUTs. We used directives for area utilization which resulted in reducing area utilization of LUTs from 103% to 77%. Also, FF area utilization decreased from 18% to 17% when resource optimization was applied along with latency optimization. Initially, latency was 147314213 which was reduced to 95602574 using latency optimization techniques.

3.2 Problems and its solution

Major concern of the project was area utilization. It was greater than 100%. That is, the circuit was unable to fit in the chip. LUTs were demanding a huge portion of the chip (more than available). To remove this, problem, we used various directives and techniques for area utilization. The main directive that reduced area utilization significantly was ‘INLINE’ directive. Using INLINE with functions that were being called multiple times, the area utilization of LUTs and FFs reduced significantly to 77% and 17% respectively. Also, after using function INLINE, synthesizing and RTL co-simulation processes became much faster which initially took hours to complete.

After area utilization, the latency increased to 129961224. To reduce this, latency optimizations were done using different directives such as PIPELINE, LOOP UNROLL and ARRAY_PARTITION. Small loops were unrolled to reduce the loop overheads. The nested loops which were frequently used were pipelined. So the final latency became 95602574.

PHASE-2

The target FPGA board is **Artix-7 board**

| Benchmark | Type (Area /Latency) | Resource Utilization | | | | Latency | | Major Optimizations |
|--------------------|----------------------------|-------------------------|-----|-----|----------|------------------------------|-----------------|--|
| | | LUT | FF | DSP | B RAM | No of Clock cycle/latency | Clock period | |
| Baseline | B | 102% | 18% | ~0% | 57% | 147314213 | 8.750 | |
| Optimization1 1 | Area | 65% | 11% | ~0% | 60% | 129961224 | 8.750 | Used Inline directives with most frequently called function like HashUpdate, HashFinal etc. |
| Optimization 2 | Latency | 77% | 17% | ~0% | 64% | 95602574 | 8.750 | AREA+LATENCY Used pipeline and loop unroll directives. |

| | | | | | | | | |
|--|--|--|--|--|--|--|--|--|
| | | | | | | | | |
|--|--|--|--|--|--|--|--|--|

Explanation-

Optimization 1- Area Optimization-

- Initially, area utilization was greater than 100%. That is, the circuit was unable to fit in the chip.
- LUTs were demanding a huge portion of the chip (more than available).
- We have used 'INLINE' directive for function inlining.
- . Using INLINE with functions that were being called multiple times, the area utilization of LUTs and FFs reduced significantly to 60% and 11% respectively
- Also, after using function INLINE, synthesizing and RTL co-simulation processes became much faster which initially took hours to complete.

Optimization 2- Area+Latency Optimization-

- After the area optimization, latency optimization has to be done which was initially very high.
- Pipeline directive was used in inner most loop in nested loops to remove the sequential execution responsible for high latency.
- Small loop were unrolled to remove the loop overhead of condition checking, incrementing etc.
- Finally array_partition was also used as RAM has limited ports to read and write the data.