



Experiment No.6
Implement Carry Look Ahead Adder.
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Roll Number: 49
Date of Performance:
Date of Submission:

**Aim:** . To implement carry look ahead adder.

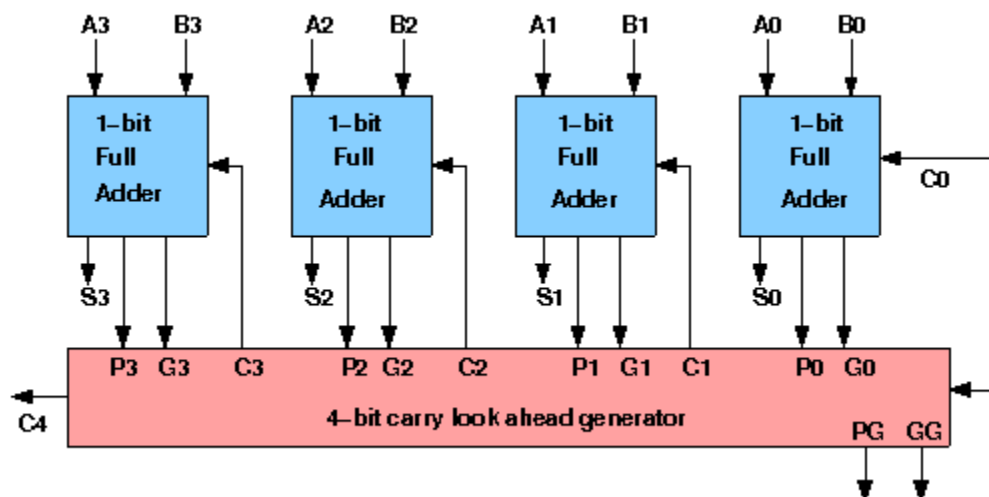
**Objective:**

It computes the carries parallelly thus greatly speeding up the computation.

1. To understanding behaviour of carry lookahead adder from module designed by the student as part of the experiment
2. To understand the concept of reducing computation time with respect of ripple carry adder by using carry generate and propagate functions.
3. The adder will add two 4 bit numbers

**Theory:**

To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be Carry Propagator and Carry Generator. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry. The block diagram of a 4-bit Carry Lookahead Adder is shown here below -





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The number of gate levels for the carry propagation can be found from the circuit of full adder. The signal from input carry  $C_{in}$  to output carry  $C_{out}$  requires an AND gate and an OR gate, which constitutes two gate levels. So if there are four full adders in the parallel adder, the output carry  $C_5$  would have  $2 \times 4 = 8$  gate levels from  $C_1$  to  $C_5$ . For an  $n$ -bit parallel adder, there are  $2n$  gate levels to propagate through.

### Design Issues :

The corresponding boolean expressions are given here to construct a carry lookahead adder. In the carry-lookahead circuit we need to generate the two signals carry propagator( $P$ ) and carry generator( $G$ ),

$$P_i = A_i \oplus B_i$$

$$G_i = A_i \cdot B_i$$

The output sum and carry can be expressed as

$$Sum_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + (P_i \cdot C_i)$$

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each  $C_i$  its value from the previous equations:

$$C_1 = G_0 + P_0 \cdot C_0$$

$$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$$

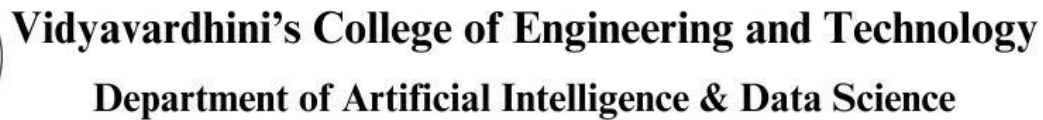
$$C_3 = G_2 + P_2 \cdot C_2 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

$$C_4 = G_3 + P_3 \cdot C_3 = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

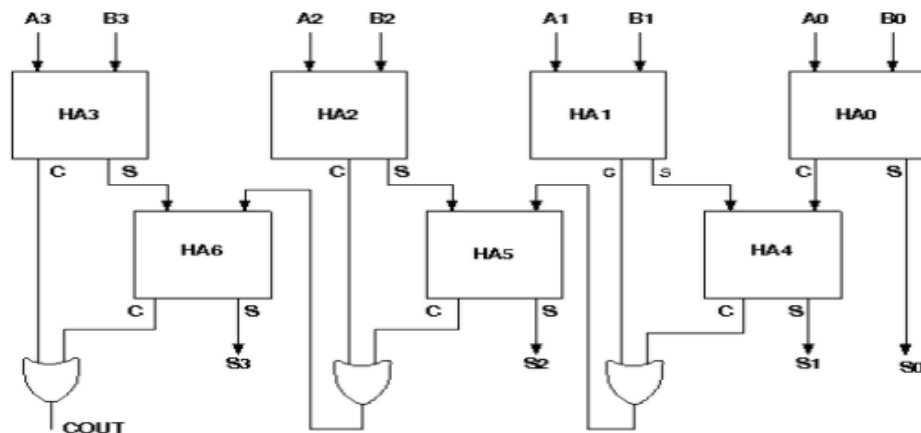
### Procedure:

Procedure to perform the experiment: Design of Carry Look ahead Adders

- 1) Start the simulator as directed. This simulator supports 5-valued logic.
- 2) To design the circuit we need 7 half adder, 3 OR gate, 1 V+(to give 1 as input), 3 Digital display(2 for seeing input and 1 for seeing output sum), 1 Bit display(to see the carry output), wires.
- 3) The pin configurations of a component are shown whenever the mouse is hovered on any canned component of the palette or press the 'show pinconfig' button. Pin numbering starts from 1 and from the bottom left corner (indicating with the circle) and increases anticlockwise.
- 4) For half adder input is in pin-5,8 output sum is in pin-4 and carry is pin-1
- 5) Click on the half adder component(in the Adder drawer in the pallet) and then click on the position of the editor window where you want to add the component(no drag and drop, simple click will serve the purpose), likewise add 6 more full adders(from the Adder drawer in the pallet), 3 OR gates(from Logic Gates drawer in the pallet), 1 V+, 3 digital display and 1 bit Displays(from Display and Input drawer of the pallet, if it is not seen scroll down in the drawer)



- ### Circuit diagram of Carry Look Ahead Adder:



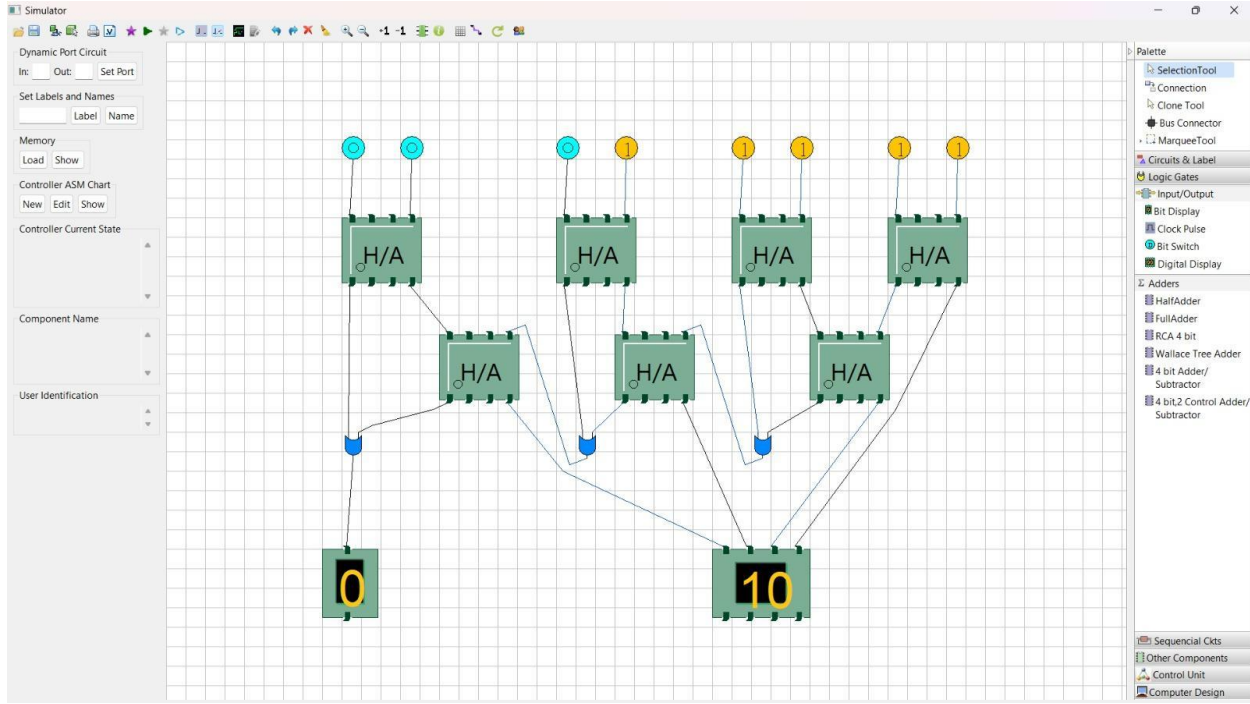
1. 7 half-adders: 4 to create the look adder circuit, and 3 to evaluate  $S_i$  and  $P_i \cdot C_i$
2. 3 OR gates to generate the next level carry  $C_{i+1}$
3. wires to connect
4. LED display to obtain the output

## CSL302: Digital Logic &amp; Computer Organization Architecture Lab



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**Conclusion:** Carry look-ahead adder is a fast and efficient design of multi-bit adder that uses the concepts of carry generate and carry propagate to reduce the carry propagation delay. It computes the carry signals in advance, based on the input bits, without waiting for the previous stage. It uses a complex hardware circuit that consists of partial full adders and carry look-ahead logic. It can be cascaded to form larger adders by using additional circuitry.



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