READ\_ME

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Initialization :

1. Initialize the slx design with matlab code . Which passes input test cases and sample time .
2. The test1.m is used for FOLDED\_basic, folded pipelined , unrolling\_1 , unrolling \_pipelined
3. The test2.m is used for folded\_parallel\_pipelined and unrolling\_pipelined\_parallel
4. The sample time can be varied to match the output slack .

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Running and Implementing :

1. The design is made to run to check if there are any errors .
2. The implantation is generated based on required target fpga board .

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Analyzing the results :

1. The frequency and resource utilization can be analyzed in synplify – pro .