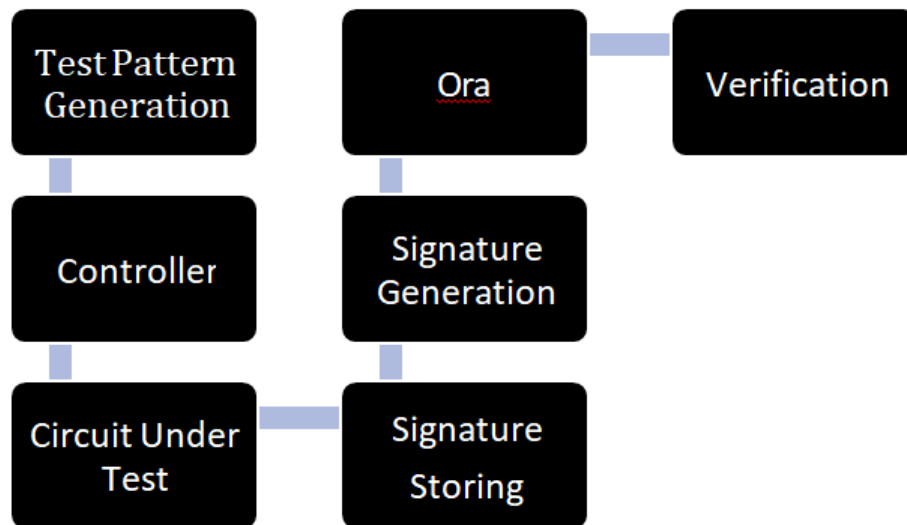
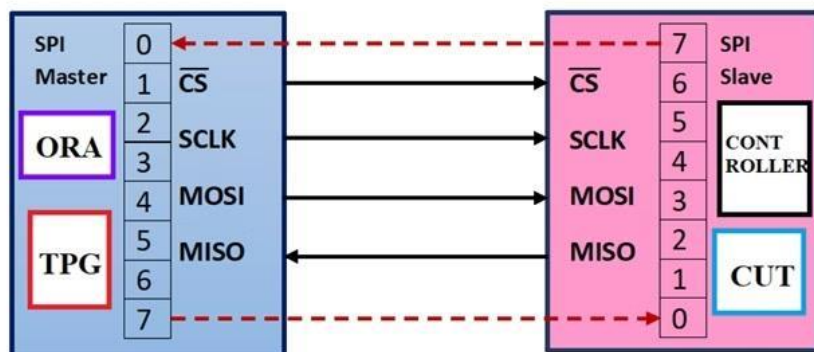


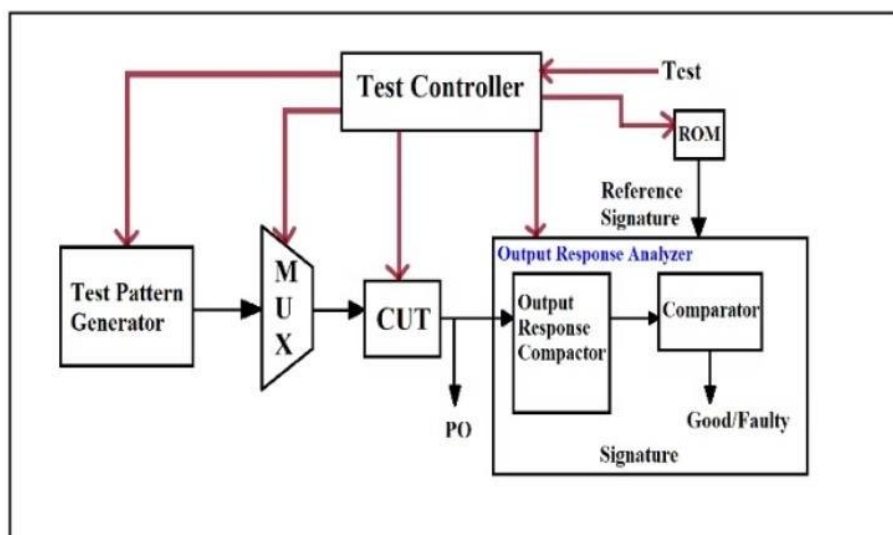
Algorithm Flowchart:



SPI with BIST:

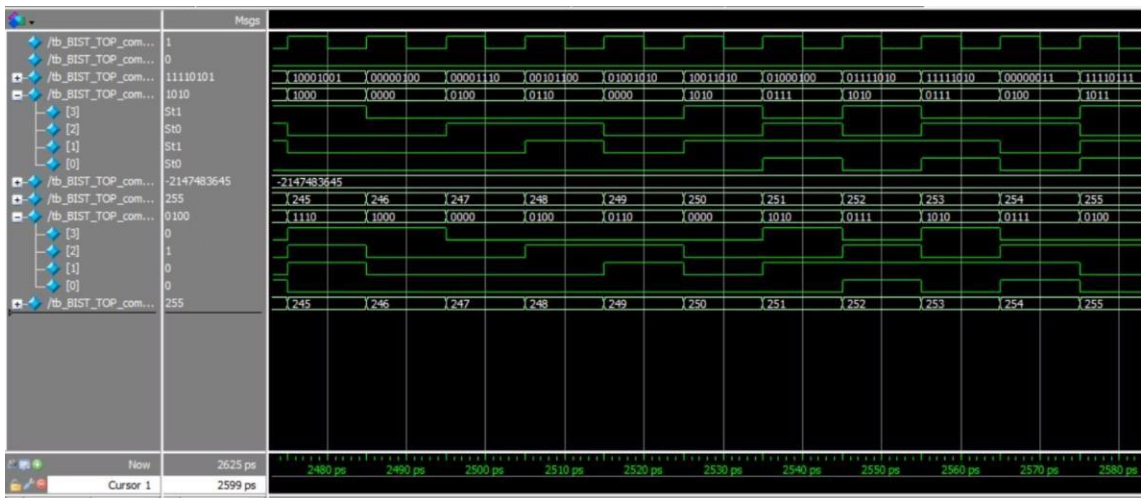


Circuit Diagram:



Results and Output:

Simulation Result:



Testbench Result:

```
Transcript
File Edit View Bookmarks Window Help
Transcript
# IrProgress: [#####] 84% CompleteTest 214: Match! Expected = 1111, Actual = 1111
# IrProgress: [#####] 84% CompleteTest 215: Match! Expected = 0110, Actual = 0110
# IrProgress: [#####] 85% CompleteTest 216: Match! Expected = 1101, Actual = 1101
# IrProgress: [#####] 85% CompleteTest 217: Match! Expected = 0000, Actual = 0000
# IrProgress: [#####] 85% CompleteTest 218: Match! Expected = 1011, Actual = 1011
# IrProgress: [#####] 86% CompleteTest 219: Match! Expected = 1010, Actual = 1010
# IrProgress: [#####] 86% CompleteTest 220: Match! Expected = 0001, Actual = 0001
# IrProgress: [#####] 87% CompleteTest 221: Match! Expected = 1100, Actual = 1100
# IrProgress: [#####] 87% CompleteTest 222: Match! Expected = 1101, Actual = 1101
# IrProgress: [#####] 87% CompleteTest 223: Match! Expected = 1010, Actual = 1010
# IrProgress: [#####] 88% CompleteTest 224: Match! Expected = 0101, Actual = 0101
# IrProgress: [#####] 88% CompleteTest 225: Match! Expected = 0101, Actual = 0101
# IrProgress: [#####] 89% CompleteTest 226: Match! Expected = 1010, Actual = 1010
# IrProgress: [#####] 89% CompleteTest 227: Match! Expected = 1000, Actual = 1000
# IrProgress: [#####] 89% CompleteTest 228: Match! Expected = 0011, Actual = 0011
# IrProgress: [#####] 90% CompleteTest 229: Match! Expected = 0011, Actual = 0011
# IrProgress: [#####] 90% CompleteTest 230: Match! Expected = 0110, Actual = 0110
# IrProgress: [#####] 90% CompleteTest 231: Match! Expected = 1100, Actual = 1100
# IrProgress: [#####] 91% CompleteTest 232: Match! Expected = 0011, Actual = 0011
# IrProgress: [#####] 91% CompleteTest 233: Match! Expected = 1100, Actual = 1100
# IrProgress: [#####] 92% CompleteTest 234: Match! Expected = 0101, Actual = 0101
# IrProgress: [#####] 92% CompleteTest 235: Match! Expected = 0011, Actual = 0011
# IrProgress: [#####] 92% CompleteTest 236: Match! Expected = 0001, Actual = 0001
# IrProgress: [#####] 93% CompleteTest 237: Match! Expected = 1100, Actual = 1100
# IrProgress: [#####] 93% CompleteTest 238: Match! Expected = 1100, Actual = 1100
# IrProgress: [#####] 94% CompleteTest 239: Match! Expected = 0001, Actual = 0001
# IrProgress: [#####] 94% CompleteTest 240: Match! Expected = 1101, Actual = 1101
# IrProgress: [#####] 94% CompleteTest 241: Match! Expected = 1100, Actual = 1100
# IrProgress: [#####] 95% CompleteTest 242: Match! Expected = 0010, Actual = 0010
# IrProgress: [#####] 95% CompleteTest 243: Match! Expected = 0001, Actual = 0001
# IrProgress: [#####] 96% CompleteTest 244: Match! Expected = 1110, Actual = 1110
# IrProgress: [#####] 96% CompleteTest 245: Match! Expected = 1000, Actual = 1000
# IrProgress: [#####] 96% CompleteTest 246: Match! Expected = 0000, Actual = 0000
# IrProgress: [#####] 97% CompleteTest 247: Match! Expected = 0100, Actual = 0100
# IrProgress: [#####] 97% CompleteTest 248: Match! Expected = 0110, Actual = 0110
# IrProgress: [#####] 98% CompleteTest 249: Match! Expected = 0000, Actual = 0000
# IrProgress: [#####] 98% CompleteTest 250: Match! Expected = 1010, Actual = 1010
# IrProgress: [#####] 98% CompleteTest 251: Match! Expected = 0111, Actual = 0111
# IrProgress: [#####] 99% CompleteTest 252: Match! Expected = 1010, Actual = 1010
# IrProgress: [#####] 99% CompleteTest 253: Match! Expected = 0111, Actual = 0111
# IrProgress: [#####] 100% CompleteTest 254: Match! Expected = 0100, Actual = 0100
** Note: $finish : C:/Users/D DANUS/OneDrive/Documents/verilog/18.1 - Copy/tb_BIST_TOP_compare.v(79)
# Time: 2625 ps Iteration: 0 Instance: /tb_BIST_TOP_compare
# 1
# Break in Module tb_BIST_TOP_compare at C:/Users/D DANUS/OneDrive/Documents/verilog/18.1 - Copy/tb_BIST_TOP_compare.v line 79
```