MIC69303RT

Radiation Tolerant Single Supply V_{IN}, Low V_{IN}, Low V_{OUT}, 3A LDO

Features

- Input Voltage Range V_{IN}: +1.65V to +5.5V
- Maximum Dropout (V_{IN} – V_{OUT}) of 500 mV over Temperature
- Adjustable Output Voltage Down to 0.5V
- Soft Start Operation
- Low Ground Current at Shutdown
- Stable at all Temperatures with 20 µF Ceramic Output Capacitor
- Excellent Line and Load Regulation
- Logic Controlled Shutdown
- Thermal Shutdown and Current-Limit Protection
- Error Flag Output
- Military Temperature Range: -55°C to 125°C
- Radiation Tolerant Data:
  - Total Dose: 50 krad (biased and unbiased)
  - Heavy Ion Single Event Effects (SEE): Latch-up Immunity > 78 MeV × cm^2/mg (+125°C)
- 8-Lead SOIC Plastic Package Exposed Pad – 0.078g
- 10-Lead Flat Pack Ceramic Package Exposed Pad – 0.37g
- All Devices are RoHS Compliant

Space Quality Grade

The hermetic MIC69303RT is manufactured in compliance with the following MIL Class Q or Class V requirements: screening testing, qualification testing and TCI/QCI specifications. The plastic MIC69303RT is compliant with AEC-Q100 automotive requirements with specific additional tests necessary for space applications. Screening and qualification flows are described in Aerospace and Defense AEQA0242/DS60001546 specifications available on the Microchip website.

General Description

The MIC69303RT is a high reliability, Radiation Tolerant, high current, low voltage, adjustable output regulator, which supports output currents of 3A built to sustain the most demanding requirements of the Aerospace environment. Operating in temperatures ranging from -55°C to 125°C as required in Aerospace applications, the MIC69303RT is proposed in both ceramic and plastic packages.

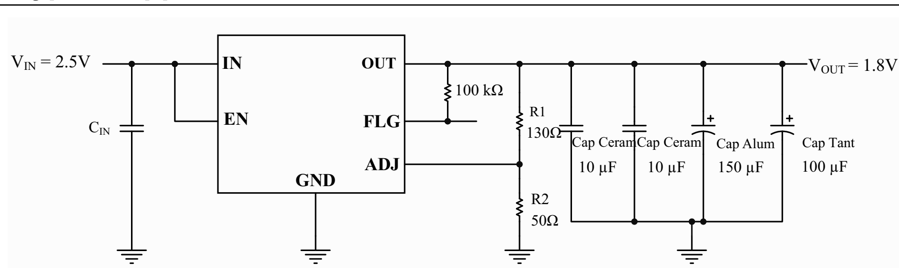
Operating from a single low voltage supply of 1.65V to 5.5V, can supply output voltages as low as 0.5V at high currents, offering high precision and ultra-low dropout voltages of 500 mV under worst-case conditions, making it ideal as the core power supply for FPGA, PLD, DSP, Microcontrollers and low DC-to-DC voltage conversion.

The low noise of the output makes it ideal for applications in sensitive RF circuits, post-regulation of switching power supplies and industrial power applications.

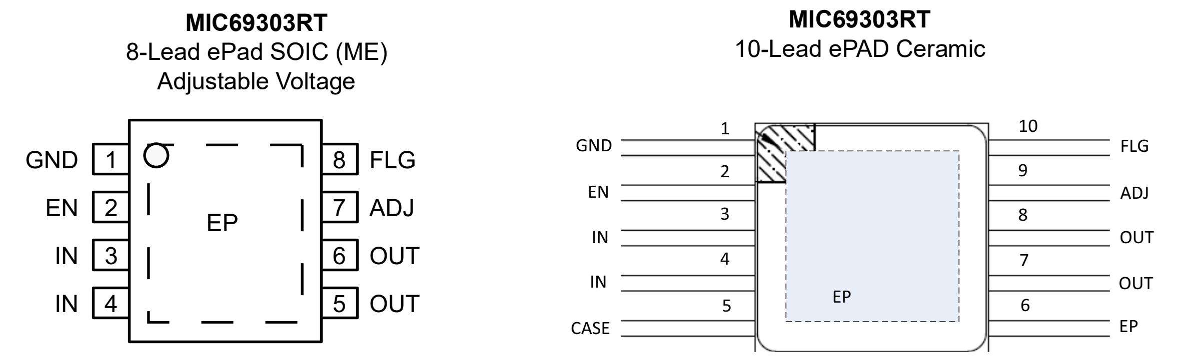
Featuring µCap design, the MIC69303RT is optimized for stability with low-value, low-ESR ceramic output capacitors.

To ensure that the MIC69303RT operates in its nominal range while exposed to radiation, on top of the 10 µF ceramic capacitors, a 150 µF chemical capacitor, and a 100 µF tantalum capacitor shall be connected to the output as close as possible to the device.

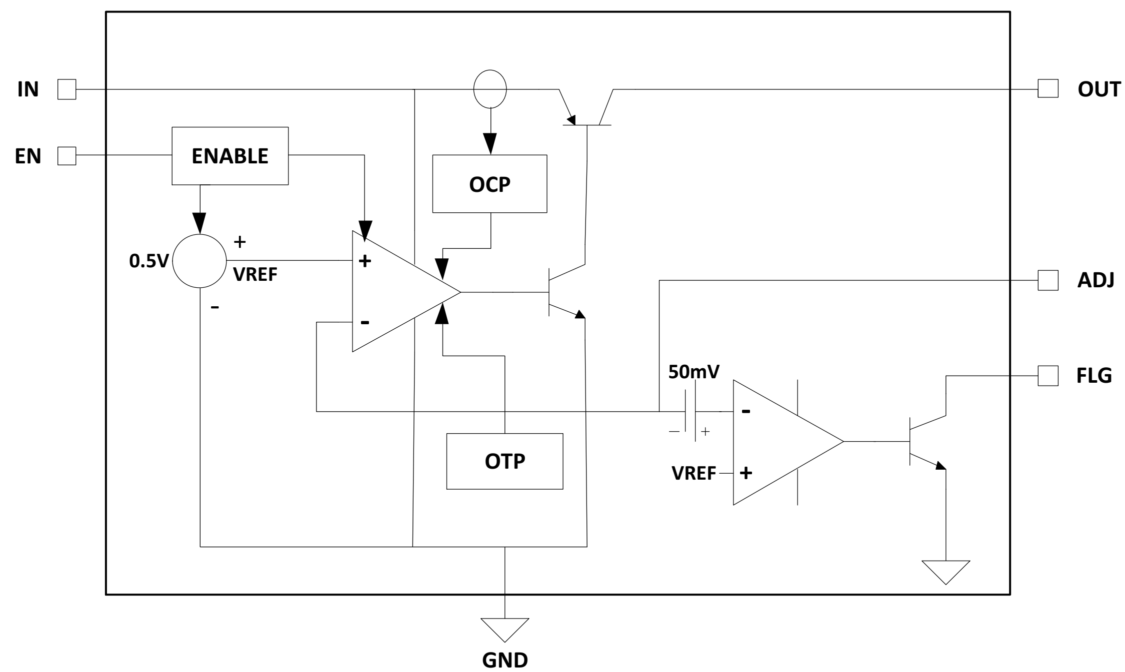
MIC69303RT Typical Application Circuit



Pin Configurations



MIC69303RT Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Input Voltage (V_{IN} to GND) .... -0.3V to +6V
Logic Input Voltage (V_{EN} to GND).......... -0.3V to (V_{IN} + 0.3V)
Fault Flag (V_{FLG} to GND).......... -0.3V to +6V
Maximum Junction Temperature (T_J) .... +165°C
Storage Temperature (T_S).......... -55°C to +165°C
Lead Temperature (T_{LEAD}).......... 260°C
ESD Rating (HBM) .... 2 kV
ESD Rating (CDM in Corner Pins).......... >750V
ESD Rating (CDM on All Other Pins).......... >500V

Operating Ratings ††

Supply Voltage (V_{IN}) .... +1.65V to +5.5V
Enable Input Voltage (V_{EN}) .... 0V to V_{IN}
Junction Temperature (T_J).......... -55°C ≤ T_J ≤ +165°C
Power Dissipation .... Internally Limited

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Exceeding the absolute maximum rating may damage the device.
2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.
3: The device is not guaranteed to function outside operating range.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = V_{OUT} + 1V; –55°C < T_A < +125°C; I_{OUT} = 10 mA; C_{OUT} = 20 µF X7R Ceramic, unless noted (**Note 1**).

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Input Supply						
Input Voltage Range	V_{IN}	1.65	—	5.5	V	—
Ground Pin Current	I_{GND}	—	1.2	5	mA	I_{OUT} = 10 mA
		—	12	30	mA	I_{OUT} = 1.5 A
		—	32	75	mA	I_{OUT} = 3 A
Ground Pin Current in Shutdown	—	—	1	10	µA	V_{EN} = 0V; V_{IN} = 2.0V; V_{OUT} = 0V
Output Voltage						
Load Regulation	—	—	±0.3	—	%	I_{OUT} = 10 mA to 3A
Line Regulation	—	—	0.2	0.3	%/V	V_{IN} = (V_{OUT} + 1.0V) to 5.5V (**Note 3**)

Note 1: Exceeding the absolute maximum rating may damage the device.
2: The device is not guaranteed to function outside its operating rating.
3: The maximum allowable power dissipation of any TA (ambient temperature) is ($P_{D(max)}$ = $T_{J(max)}$ – T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will result in excessive die temperature and the regulator will go into thermal shutdown.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$; –55°C < T_A < +125°C; I_{OUT} = 10 mA; C_{OUT} = 20 µF X7R Ceramic, unless noted (**Note 1**).

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Reference (Adjustable)						
Feedback Reference Voltage (ADJ Pin)	—	0.485	0.5	0.515	V	±3.0%
Feedback Bias Current	—	—	0.25	1.0	µA	V_{ADJ} = 0.5V
Current Limit						
Current Limit	I_{LIM}	3.0	5.2	8	A	V_{OUT} = 0V
Power Dropout Voltage						
Dropout Voltage	$V_{IN} – V_{OUT}$	—	200	300	mV	I_{OUT} = 1.5A
		—	275	500	mV	I_{OUT} = 3A
Enable Input						
Enable Input Threshold	—	0.9		—	V	Regulator Enabled
		—	—	0.1		Regulator Shut Down
Enable Pin Bias Current	—	—	—	1	µA	V_{EN} ≤ 0.2V (Regulator Shutdown)
		—	7	10		V_{EN} ≥ 0.8V (Regulator Enabled)
Turn-On Time	t_{ON}	—	—	150	µs	90% of typical V_{OUT}; $V_{EN} = V_{IN}$
Fault Output						
Fault Threshold Voltage	—	80	90	95	%	% of V_{OUT} below nominal output (V_{OUT} Falling)
Fault Hysteresis	—	—	2.0	—	%	—
Fault Output Low Voltage	—	—		300	mV	I_{FLG} = 5 mA (sinking), V_{EN} = 1.65V
Fault Leakage Current	—	—		1	µA	V_{FLG} = 5.0V; V_{EN} = 1.65V
Thermal Protection						
Overtemperature Shutdown	—	—	165	—	°C	T_J rising
Overtemperature Shutdown Hysteresis	—	—	10	—	°C	—

Note 1: Exceeding the absolute maximum rating may damage the device.

2: The device is not guaranteed to function outside its operating rating.

3: The maximum allowable power dissipation of any TA (ambient temperature) is $(P_{D(max)} = T_{J(max)} – T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature and the regulator will go into thermal shutdown.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–55	—	+165	°C	
Storage Temperature Range	T_S	–55	—	+165	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	—
Package Thermal Resistance						
Thermal Resistance, ePad SOIC 8-Ld	θ_{JC}	—	2.17	—	°C/W	**Note 1**
Thermal Resistance, Ceramic 10-Ld	θ_{JC}	—	1.8	—	°C/W	**Note 1**

Note 1: Simulated in vacuum conditions.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

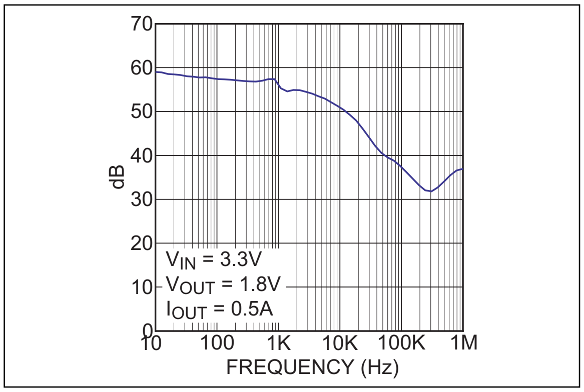


FIGURE 2-1: *Power Supply Rejection Ratio.*

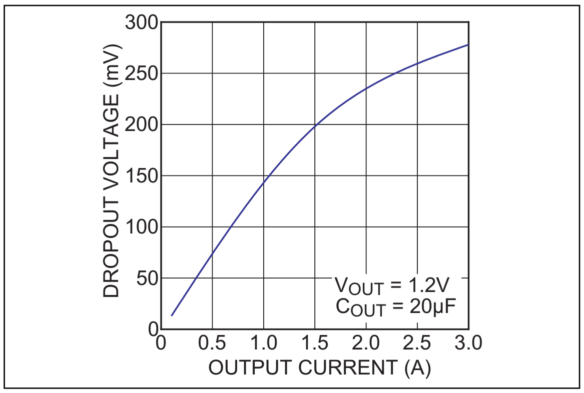


FIGURE 2-2: *Dropout Voltage vs. Output Current.*

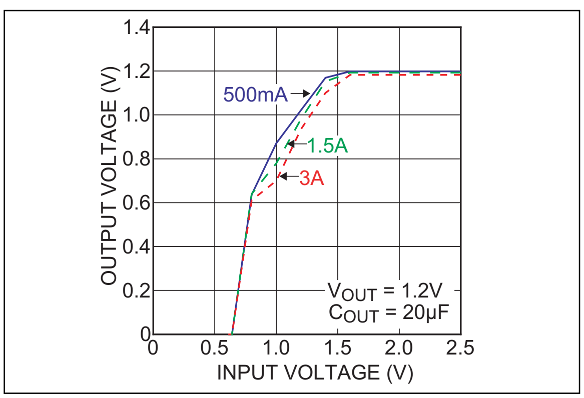


FIGURE 2-3: *Dropout Voltage vs. Input Voltage.*

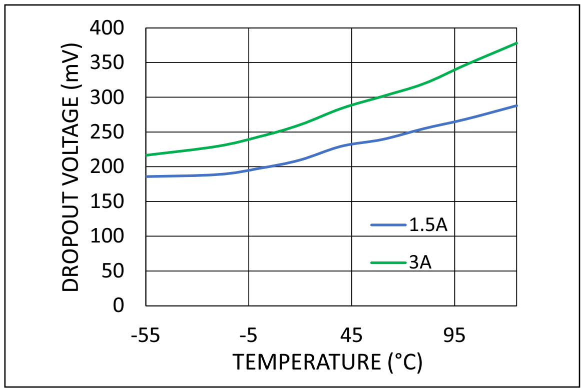


FIGURE 2-4: *Dropout Voltage vs. Temperature.*

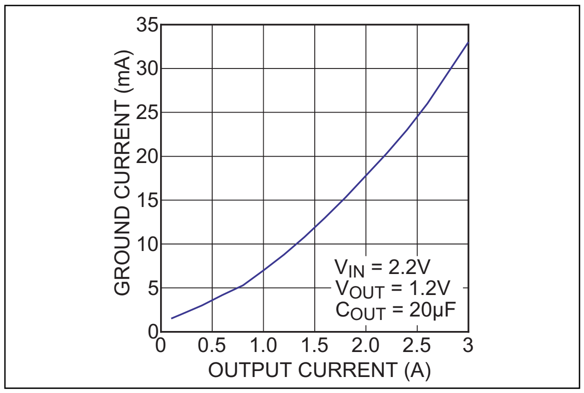


FIGURE 2-5: *Ground Current vs. Output Current.*

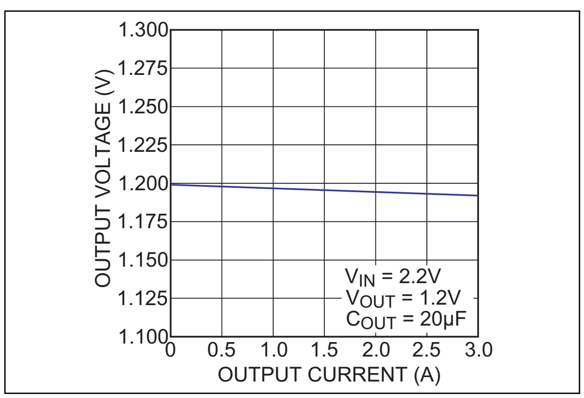


FIGURE 2-6: *Load Regulation.*

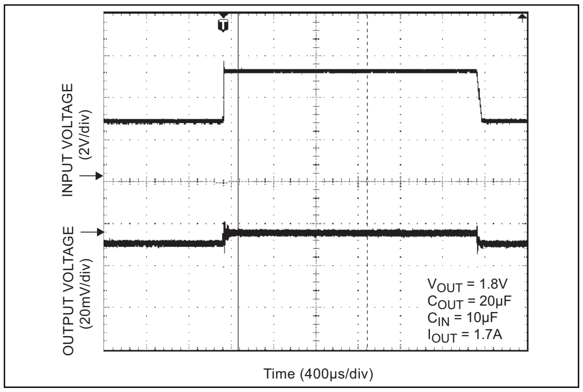


FIGURE 2-7: *Line Transient.*

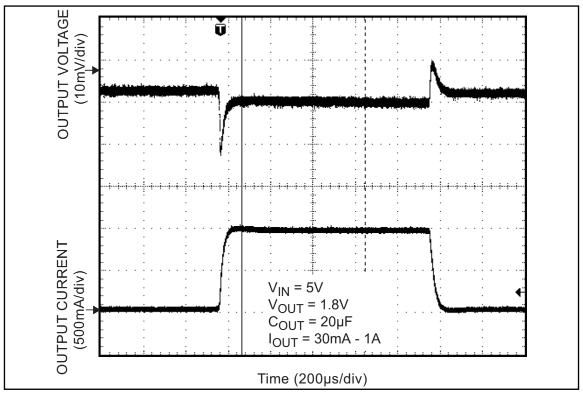


FIGURE 2-8: *Load Transient.*

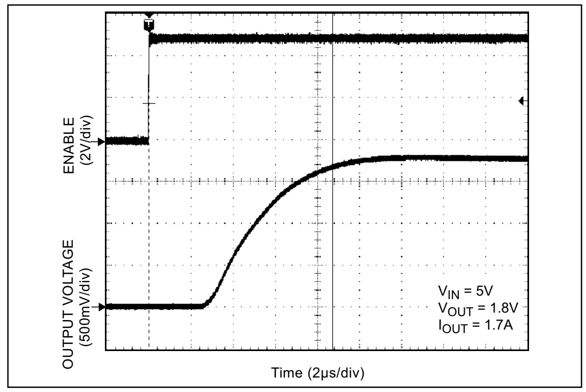


FIGURE 2-9: *Enable Turn-On.*

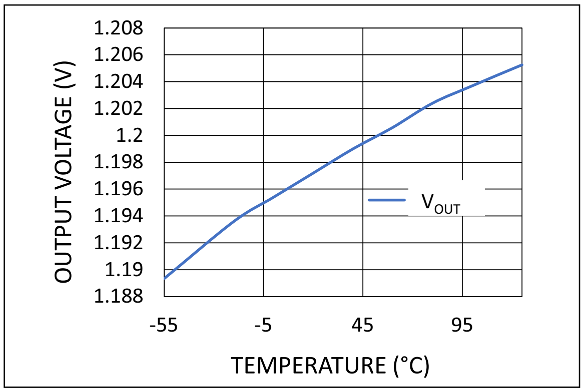


FIGURE 2-10: *Enable Threshold vs. Temperature.*

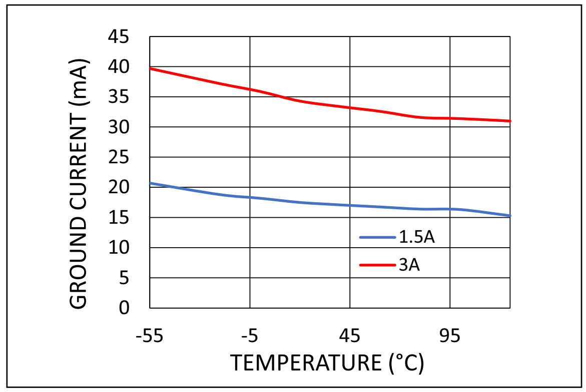


FIGURE 2-12: *Ground Current vs Temperature.*

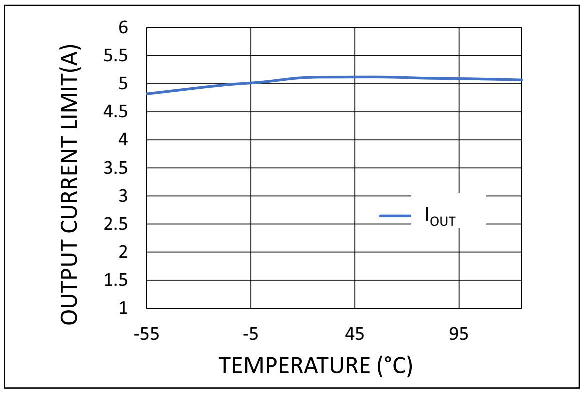


FIGURE 2-11: *Current Limit vs. Temperature.*

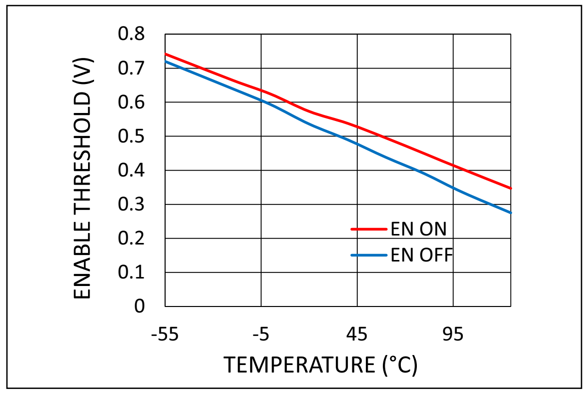


FIGURE 2-13: *Enable Threshold vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number ePad 8L-SOIC	Pin Number 10L-Ceramic	Pin Name	Description
1	1	GND	Ground
2	2	EN	Enable (Input): CMOS compatible input. Logic high = enable, logic low = shutdown. Do not leave pin floating.
3, 4	3, 4	IN	Input voltage that supplies current to the output power device.
5, 6		OUT	Regulator Output.
	5		Connected to case
	6		Connected to EP
	7, 8	OUT	Regulator Output.
7	9	ADJ	Adjustable regulator feedback input. Connect to resistor voltage divider.
8	10	FLG	Error Flag (Output): Open collector output. Active-low indicates an output fault condition.
EP	EP	EP	Exposed pad. Connect to GND.

4.0 FUNCTIONAL DESCRIPTION

The MIC69303RT is an ultra-high performance low dropout linear regulator designed for high current applications requiring a fast-transient response. It utilizes a single input supply and has a very low dropout voltage perfect for low-voltage DC-to-DC conversion. The MIC69303RT requires a minimum number of external components.

The MIC69303RT regulator is fully protected from damage due to fault conditions offering constant current limiting and thermal shutdown.

The MIC69303RT operates from an input voltage of 1.65V to 5.5V. It is designed to drive digital circuits requiring low voltage at high currents (i.e., FPGA, PLDs, DSP, microcontroller, etc.). This regulator is available in adjustable output voltages. The regulator can support output voltages from 5V maximum down to 0.5V.

The µCap design of the MIC69303RT is optimized for stability with two low-value, low-ESR 10 µF ceramic output capacitors to behave correctly under radiation environment in space applications in addition of the 2×10 µF ceramic capacitors, a 150 µF chemical capacitor, and a 100 µF tantalum capacitor shall be connected to the output as close as possible to the device.

Features of the MIC69303RT includes thermal shutdown, current limit protection, Fault Flag and Logic enable functions.

4.1 Input Supply Voltage

V_{IN} provides a high current to the collector of the pass transistor. The minimum input voltage is 1.65V, allowing conversion from low voltage supplies.

4.2 Output Capacitor

The MIC69303RT require a minimum of output capacitance to maintain stability. However, proper capacitor selection is important to ensure desired transient response. The MIC69303RT are specifically designed to be stable with low-ESR ceramic chip capacitors. A 20 µF ceramic chip capacitor should satisfy most applications. Output capacitance can be increased without bound. See the Typical Performance Curves for examples of load transient response.

X7R dielectric ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by only 15% over their operating temperature range and are the most stable type of ceramic capacitors.

4.3 Input Capacitor

An input capacitor of 1 µF or greater is recommended when the device is more than 4 inches away from the bulk supply capacitance or when the supply is a battery. Small, surface mount, ceramic chip capacitors can be used for the bypassing. The capacitor should be placed within 1 inch of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the input to the regulator further improving the integrity of the output voltage.

4.4 Minimum Load Current

The MIC69303RT regulator is specified between finite loads. If the output current is too small, leakage currents dominate and the output voltage rises. A 10 mA minimum load current is necessary for proper operation.

4.5 Adjustable Regulator Design

The MIC69303RT allows programming the output voltage anywhere between 0.5V and 5.0V with two resistors. The resistor value between V_{OUT} and the adjusted pin should not exceed 10 kΩ. Larger values can cause instability. The resistor values are calculated by:

EQUATION 4-1:

$$V_{OUT} = 0.5 \times \left(\frac{R1}{R2} + 1\right)$$

Where:

V_{OUT} = Desired output voltage.

4.6 Enable

The fixed output voltage versions of the MIC69303RT feature an active-high enable input (EN) that allows on-off control of the regulator. The current drain reduces to near zero when the device is shut down, with only microamperes of leakage current. EN may be directly tied to VIN and pulled up to the maximum supply voltage.

4.7 Error Flag

The error flag is an open-collector output that can sink current during a fault condition. The error flag circuit monitors the output voltage and signals an error condition when the ADJ voltage is 10% below the reference voltage. The low output voltage can be caused by several problems, including an overcurrent fault (device in the current limit), over temperature protection or low input voltage.

4.8 Thermal Design

Linear regulators are simple to use. The most complicated design parameters to consider are thermal characteristics. Thermal design requires the following application-specific parameters:

- Maximum ambient temperature (T_A)
- Output current (I_{OUT})
- Output voltage (V_{OUT})
- Input voltage (V_{IN})
- Ground current (I_{GND})

First, calculate the power dissipation of the regulator from these numbers and the device parameters from this data sheet.

EQUATION 4-2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The ground current is approximated by using numbers from the Electrical Characteristics table or Typical Performance Curves section. The heat sink thermal resistance is then determined with this formula:

EQUATION 4-3:

$$\theta_{JA} = \left(\frac{T_{J(MAX)} - T_A}{P_D}\right) - (\theta_{JC} + \theta_{CS})$$

Where:

$T_{J(MAX)} \le 125°C$.

θ_{CS} = Between 0°C/W and 2°C/W.

The heat sink may be significantly reduced in applications where the minimum input voltage is known and is large compared with the dropout voltage. Use a series input resistor to drop excessive voltage and distribute the heat between this resistor and the regulator. The low dropout properties of Microchip Super ßeta PNP regulators allow significant reductions in regulator power dissipation and the associated heat sink without compromising performance. When this technique is employed, a capacitor of at least 1.0 µF is needed directly between the input and regulator ground.

4.9 Temperature Protection

When the junction temperature exceeds approximately 165°C with a hysteresis of about 10°C, temperature protection shuts down the output and indirectly triggers the fault flag.

4.10 Short Circuit Current Protection

Under conditions where the output of the regulator is shorted to ground, internal circuitry will limit the device to source 5.2A typical.

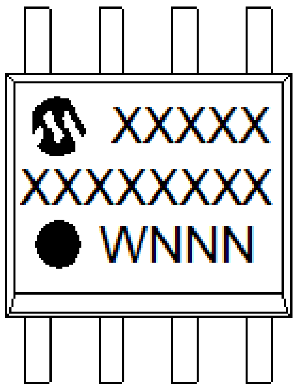
4.11 Turn-on Time

The output voltage rise time to reach 90% of the nominal after enable on is 10 us to 150 µs maximum.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

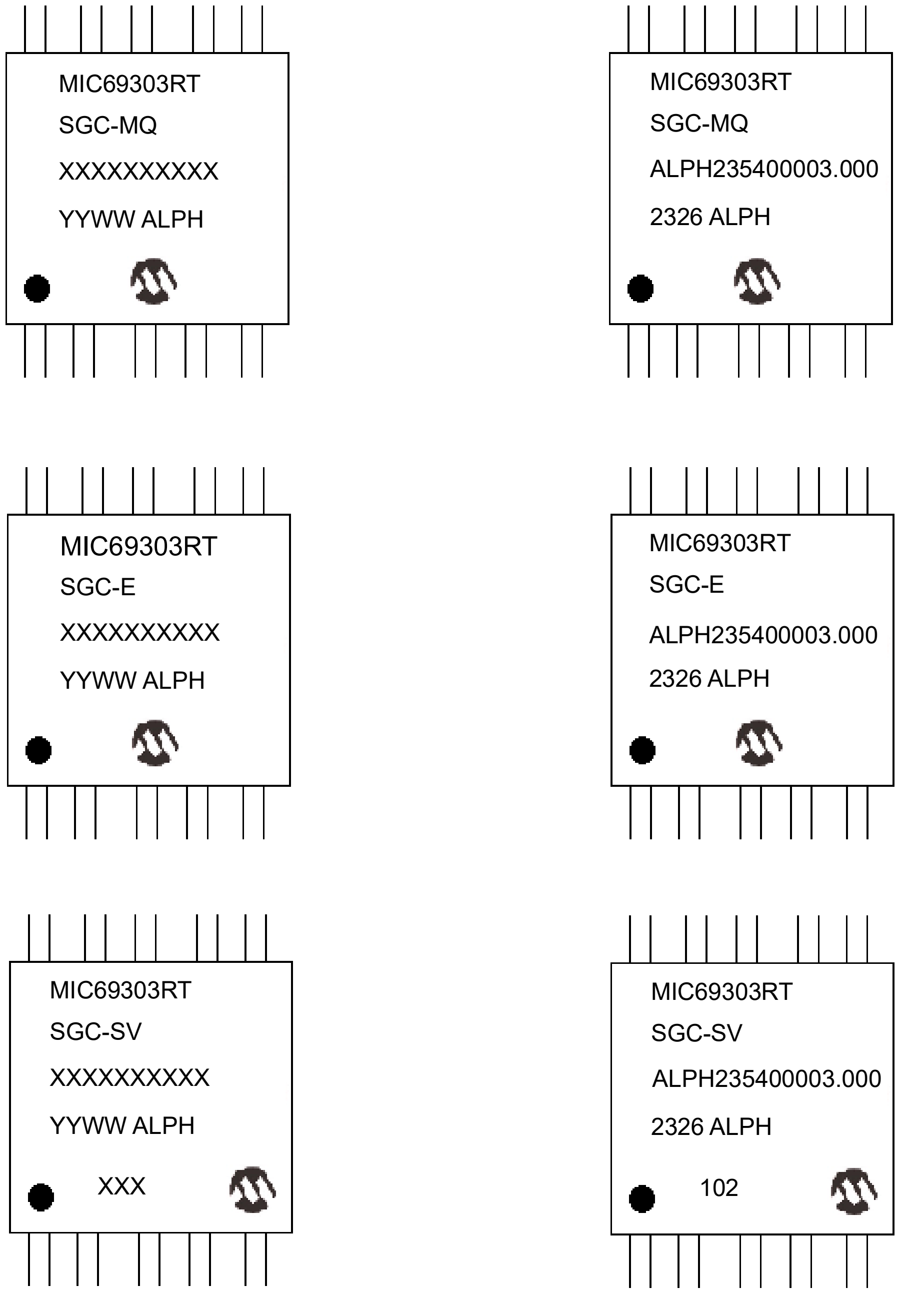
8-Lead SOIC



Example

Legend:	XX...X	Customer-specific information
	W	Week code (week of January 1 is week ‘1’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

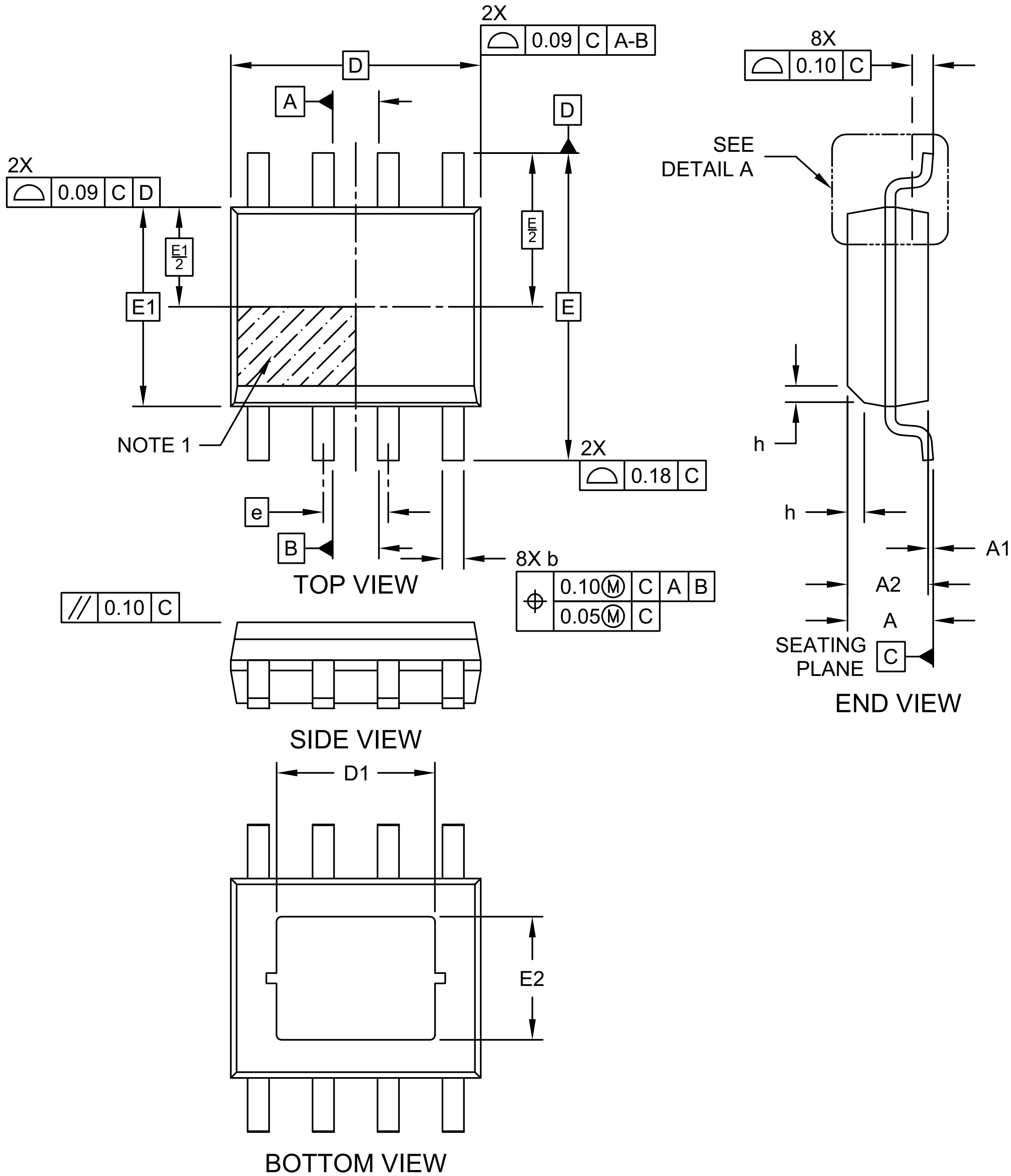
10-Lead Ceramic | Example



Legend:		
	MIC69303RT	Device part number
	SGC-MQ/SGC-E/SGC-SV	Package type – Product Type
	XX...X	Lot reference number
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	ALPH	Location code
	XXX	Serial Number

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

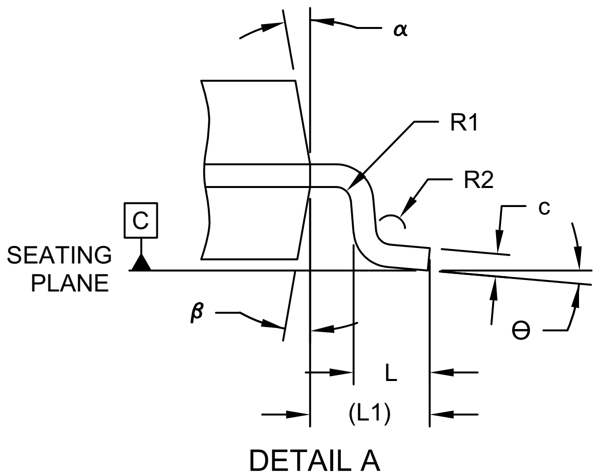
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

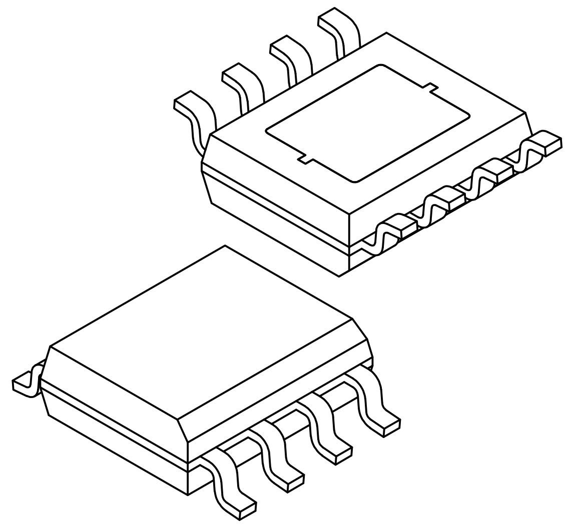


Microchip Technology Drawing C04-1136 Rev C Sheet 1 of 2

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.43	1.55	1.68
Standoff	A1	0.00	0.05	0.10
Molded Package Thickness	A2	1.25	-	-
Overall Length	D		4.89 BSC	
Exposed Pad Length	D1	-	3.10	-
Overall Width	E		6.02 BSC	
Molded Package Width	E1		3.90 BSC	
Exposed Pad Width	E2	-	2.41	-
Pin 1 Chamfer	h	-	0.33	-
Terminal Width	b	0.35	0.41	0.49
Lead Thickness	c	0.19	0.20	0.25
Terminal Length	L	0.41	0.64	0.89
Footprint	L1		1.04 REF	
Foot Angle	Θ	0°	5°	8°
Lead Bend Radius	R1	0.07	-	-
Lead Bend Radius	R2	0.07	-	-
Mold Draft Angle	α	5°	-	15°
Mold Draft Angle	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

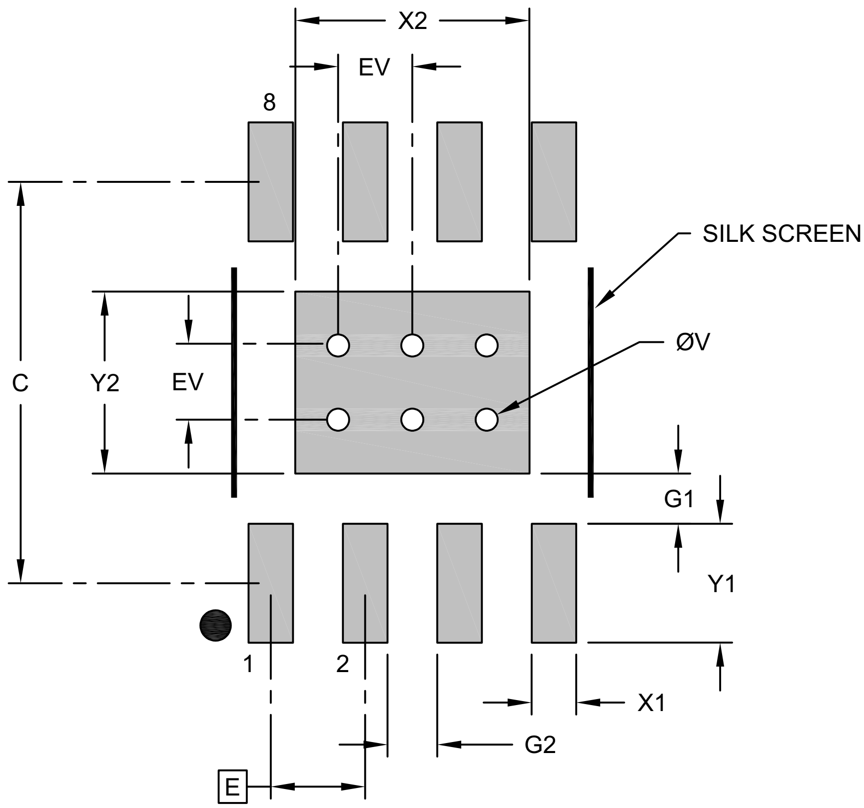
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1136 Rev C Sheet 2 of 2

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			2.45
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.60
Contact Pad to Center Pad (X8)	G1	0.68		
Contact Pad to Contact Pad (X6)	G2	0.67		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

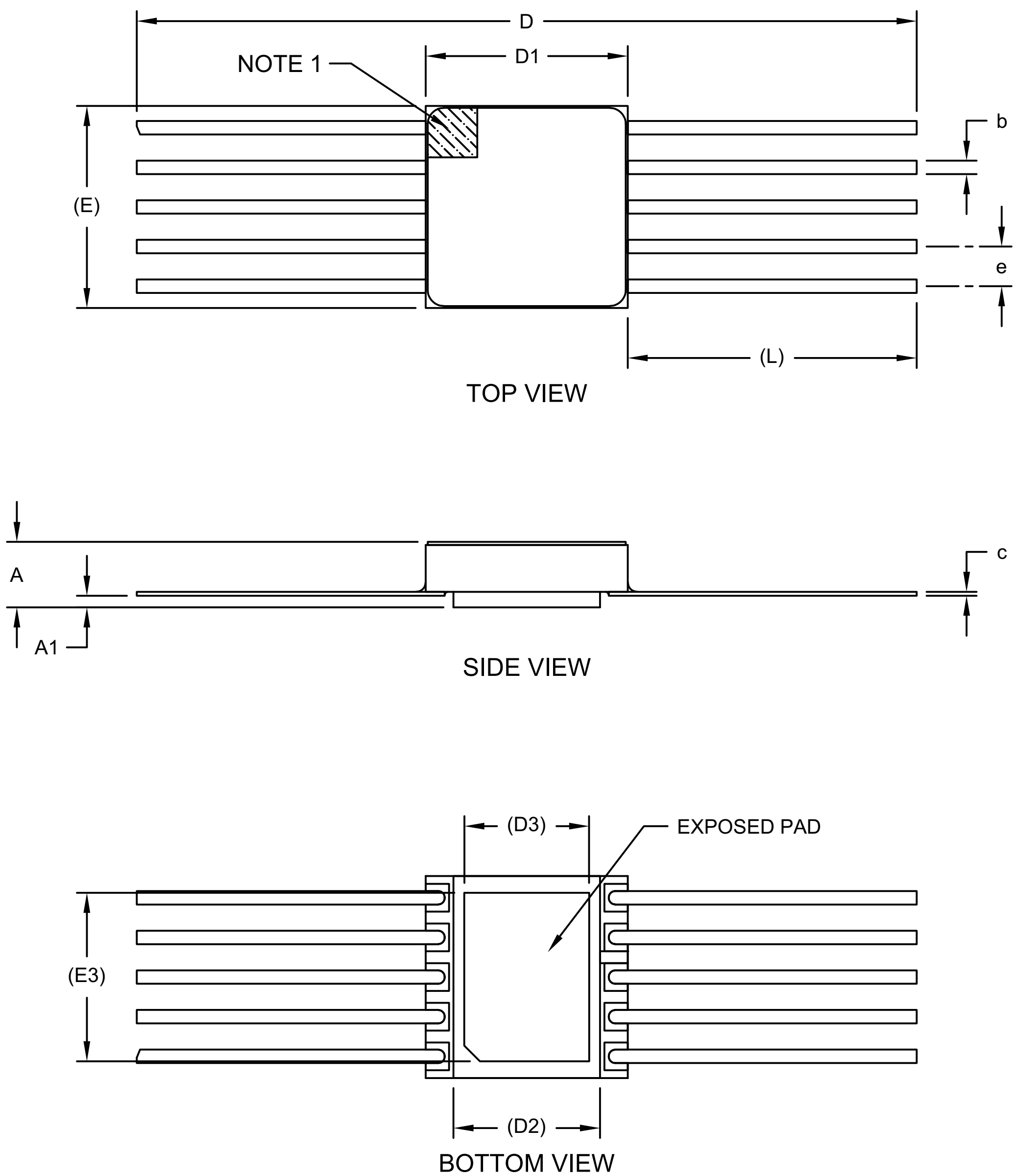
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3136 Rev C

10-Lead Ceramic Dual Flatpack (SGC) - 6.48x6.48 mm Body [CDFP]

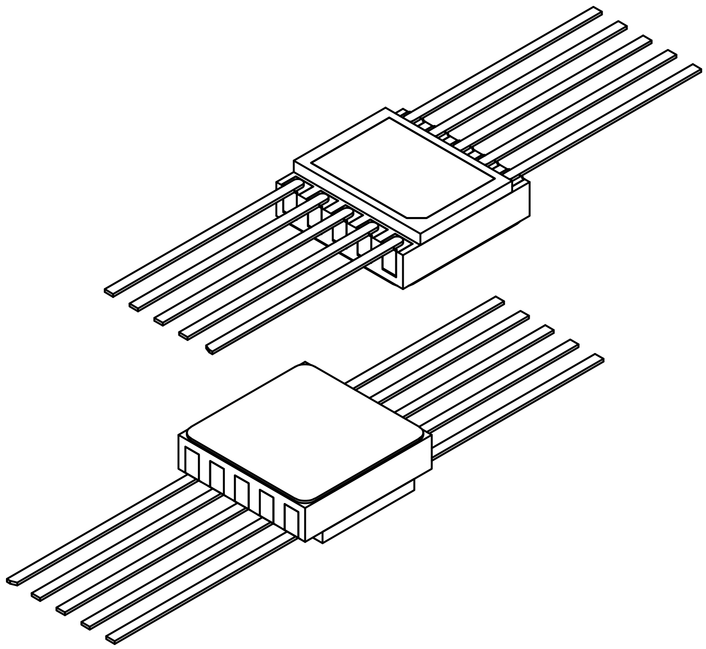
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25641 Rev B Sheet 1 of 2

10-Lead Ceramic Dual Flatpack (SGC) - 6.48x6.48 mm Body [CDFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		1.27	
Overall Height	A	2.23	2.43	2.63
Standoff	A1	0.42	0.50	0.58
Overall Length	D		25.00	
Ceramic Package Length	D1	6.18	6.48	6.78
Pedestal Length	D2		4.699 REF	
Exposed Pad Length	D3		4.00 REF	
Overall Width	E	6.18	6.48	6.78
Exposed Pad Width	E3		5.40 REF	
Terminal Width	b	0.38	0.43	0.48
Terminal Thickness	c	0.102	0.127	0.178
Terminal Length	L		9.26 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

Microchip Technology Drawing C04-25461 Rev B Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision B (June 2023)

- Updated figures 2-2 to 2-8.
- Updated the Electrical Characteristics table.
- Added Figure 2-10, Figure 2-11, Figure 2-12, and Figure 2-13.
- Updated **Section 5.0 "Packaging Information"**.
- Updated the Product Identification System page.

Revision A (December 2022)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	XXX	-XXX
Part No.	Package	Type

Device: MIC69303: Single Supply V_{IN}, Low V_{IN}, Low V_{OUT}, 3A LDO
RT: Radiation Tolerant

Package: YME = 8-Lead Plastic SOIC -ePAD
SGC = 10-Lead Ceramic Dual Flatpack -ePad

Type:
-HP = HiRel Plastic
-MQ = QML-Q Equivalent
-SV = QML-V Equivalent
-E = Engineering Ceramic +25C
-HC = HiRel Ceramic

Examples:

a) MIC69303RTYME-HP: ,Single Supply V_{IN}, Low V_{IN}, Low V_{OUT}, 3A LDO, 8-Lead SOIC package

b) MIC69303RTSGC-E: Single Supply V_{IN}, Low V_{IN}, Low V_{OUT}, 3A LDO, 10-Lead Engineering Ceramic

c) MIC69303RTSGC-SV: Single Supply V_{IN}, Low V_{IN}, Low V_{OUT}, 3A LDO, 10-Lead Ceramic, QML-V Equivalent Type package

d) MIC69303RTSGC-MQ:Single Supply V_{IN}, Low V_{IN}, Low V_{OUT}, 3A LDO, 10-Lead Ceramic, QML-Q Equivalent Type package

e) MIC69303RTSGC-HC:Single Supply V_{IN}, Low V_{IN}, Low V_{OUT}, 3A LDO, 10-Lead Ceramic, (Note 1)

Note 1: On demand special order. Contact Microchip.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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