Question Bank

1. Describe architectural and organizational issues in a computer system? Differentiate computer architecture and organization.
2. Illustrate an instruction set. Discuss CISC and RISC.
3. Differentiate the Von Neumann Machine and Harvard Architecture.
4. Discuss the Von Neumann Architecture and Harvard Architecture.
5. Consider the byte addressable memory unit of a computer has 256 K words of 32 bits each. The computer has an instruction format with 4 fields:
    i. An opcode field.
    ii. A mode field to specify 1 of 7 addressing modes.
    iii. A register address field to specify 1 of 60 registers.
    iv. A memory address field.

    If the instruction size is 32 bits long then determine the number of possible operations that can be represented with the above instruction format.
6. Discuss microprogrammed control unit organization using diagram. Mention advantage and disadvantage to use microprogrammed control unit.
7. Briefly discuss the address modes of the following given syntax.
    i. $R_1 \leftarrow$ Operand
    ii. $R_2 \leftarrow M[Address]$
    iii. $R_3 \leftarrow M[M[Address]]$
    iv. $R_4 \leftarrow R_5$
    v. $R_6 \leftarrow M[R_7]$
    vi. Push: $M[SP] \leftarrow R_8$, $SP \leftarrow SP-1$
    Pop: $SP \leftarrow SP+1$, $R_9 \leftarrow M[SP]$
8. Briefly discuss following address modes.
    i. Immediate Addressing Mode
    ii. Direct Memory Addressing Mode
    iii. Indirect Memory Addressing Mode
    iv. Direct Register Addressing Mode
    v. Indirect Register Addressing Mode
    vi. Stack Addressing Mode
9. Perform the number conversions for the following numbers.
    i. $(35.7)_8 \rightarrow (\ )_2$
    ii. $(AF.4)_H \rightarrow (\ )_{10}$
    iii. $(825.8)_{10} \rightarrow (\ )_2$
    iv. $(11011.1010)_2 \rightarrow (\ )_{10}$
10. Perform the number conversions for the following numbers.
    i. $(357)_8 \rightarrow (\ )_2$
    ii. $(AF4)_H \rightarrow (\ )_{10}$
    iii. $(82.58)_{10} \rightarrow (\ )_2$
    iv. $(11011.1010)_2 \rightarrow (\ )_{10}$
11. Perform the conversions for the following numbers:
    i. $(56.7)_8 \rightarrow (\ )_2$
    ii. $(EF.45)_{16} \rightarrow (\ )_{10}$
    iii. $(21.58)_{10} \rightarrow (\ )_2$
    iv. $(11011.1010)_2 \rightarrow (\ )_{10}$
    v. $(CA.3B)_{16} \rightarrow (\ )_8$
12. Perform the number conversions for the following numbers.
    i. $(742.35)_8 \rightarrow (\ )_2$

ii. $(364.25)_8 \rightarrow (\ )_{16}$
iii. $(A40.A4)_{16} \rightarrow (\ )_{10}$
iv. $(878.25)_{10} \rightarrow (\ )_2$
v. $(1111.1110)_2 \rightarrow (\ )_{10}$
vi. $(265.23)_8 \rightarrow (\ )_{10}$

13. Apply Booth multiplication method to multiple given numbers. Mention the flowchart.
    Multiplicand = (-8)
    Multiplier = (-5)
14. Apply Booth multiplication method to multiple given numbers. Mention the flowchart.
    Multiplicand = (-7)
    Multiplier = (-5)
15. Apply Booth multiplication method to multiple given numbers. Mention the flowchart.
    Multiplicand = (-5)
    Multiplier = (-6)
16. Discuss anyone Division Algorithm and draw the flowchart. Also perform the division algorithm for the given numbers using the same method.
    Dividend = (13)
    Divisor = (3)
17. Discuss anyone Division Algorithm and draw the flowchart. Also perform the division algorithm for the given numbers using the same method.
    Dividend = (15)
    Divisor = (4)
18. Discuss major steps used in non-restoring division method in binary arithmetic, when numbers are represented in sign magnitude form. Apply your steps to divide (-12) by (+4).
19. Discuss the memory hierarchy in terms of cost per bit and access time. Compare SRAM and DRAM.
20. Differentiate secondary memory with primary memory. Discuss briefly the followings.
    i. Magnetic Disk
    ii. Magnetic Tape
    iii. Compact Disk (CD)
    iv. Cache memory
21. Consider a 32-bit microprocessor that has an on-chip 16-kB four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Identify the set number in cache for mapping the given memory address ABCDE8F8.
22. A two-way set associative cache has lines of 16 bytes and a total size of 8K bytes. The 64M bytes main memory is byte addressable. Show the format of main memory addresses.
23. A set of associative cache consists of 64 lines or slots, divided in to four-line sets. Main memory consists 4k blocks of 128 words each. Show the format of main memory addresses.
24. A block set associative cache memory consists of 128 blocks divided in to 4 block sets. The main memory consists of 16,384 blocks and each block contain 256 eight-bit words.
25. For a cache with 2048 lines, a block size of 128 bytes, and a total size of 128KB, determine the associativity of the cache.
26. In certain scientific computations it is necessary to perform the arithmetic operation $(A_i+B_i)*(C_i+D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i= 1 through 6.

27. List and briefly describe the stages of a basic instruction pipeline and draw a space time diagram for a six-segment pipeline showing the time it takes to process eight tasks.
28. Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.
29. Consider a **direct mapped cache** of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find:
30. Number of bits in tag
31. Tag directory size
32. Consider a direct-mapped cache of size 32 KB with a block size of 128 bytes. The size of the main memory is 256 KB. Find:
33. Number of bits in the tag
34. Tag directory size
35. Consider a **2-way set associative mapped cache** of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find:
36. Number of bits in tag
37. Tag directory size
38. Consider a **4-way set associative cache** of size 32 KB with a block size of 128 bytes. The size of the main memory is 256 KB. Find:
39. Number of bits in the tag
40. Tag directory size
41. Consider a direct mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find-Size of main memory.
42. Consider a direct-mapped cache of size 256 KB with a block size of 512 bytes. There are 8 bits in the tag. Find the size of the main memory.
43. Consider a fully associative mapped cache with block size 4 KB. The size of main memory is 16 GB. Find the number of bits in tag.
44. Consider a fully associative cache with a block size of 8 KB. The size of the main memory is 32 GB. Find the number of bits in the tag.
45. Illustrate RAID.
46. Define Handshaking. Briefly discuss the handshaking process.
47. Illustrate interrupts.
48. Discuss briefly the concept of pipelining in computer architecture.
49. Discuss briefly various pipelining hazards.
50. Explore the methods to accomplish asynchronous data transfer.
51. Elucidate step by step procedure for the Direct Memory Access transfer with suitable diagram.
52. Discuss the various methods used to achieve asynchronous data transfer.
53. Illustrate interrupts.
54. Elucidate step by step procedure for the Direct Memory Access transfer with suitable diagram.
55. Describe the key characteristics of a Multiple Instruction, Multiple Data (MIMD) architecture. How can an MIMD architecture be further classified into shared-memory and distributed-memory systems?
56. Define Buses. Discuss its types.