ECEN 5730 Board 2 Good-Bad Layout Report

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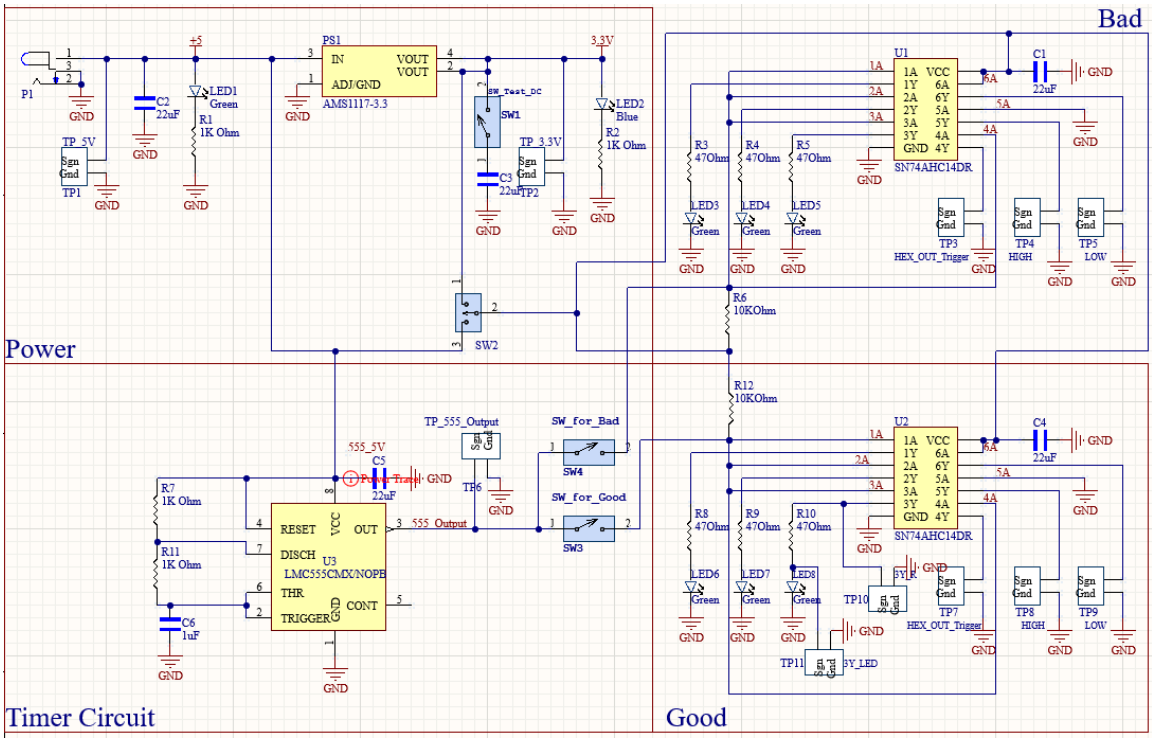
Purpose: The purpose of this board is for you to show off how layout decisions influence the amount of switching noise and the best measurement practices for measuring switching noise in a PCB.

POR:

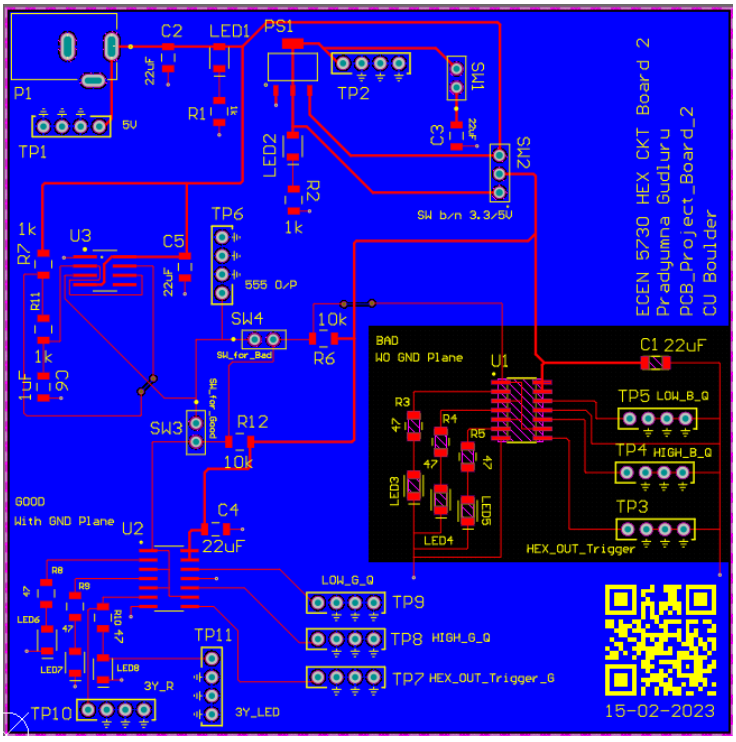
There are certain steps to be followed for developing as per the requirements. (Plan of Record)

1. The input voltage of 5V has to be converted to 3.3V and a clock signal of 500Hz with 50% duty cycle has to be created.
2. Four inputs of Hex inverter has to be demonstrated using good layout and bad layout, with C6942 operating at 5V or 3.3V
3. A switch must be added for updating 555 timer output to good and bad layout to the various inputs of the hex converter. RED LEDs are used for the switching outputs of each hex register.
4. To estimate the current flowing through 50 ohm load and extracting Thevenin resistance of the output pin of one of the I/O.
5. One of the outputs of Hex inverter must be set to trigger scope, one of the outputs to quiet HIGH and one to quiet LOW.
6. Part placement has to be same for good and bad layout except with placing the decoupling capacitor.

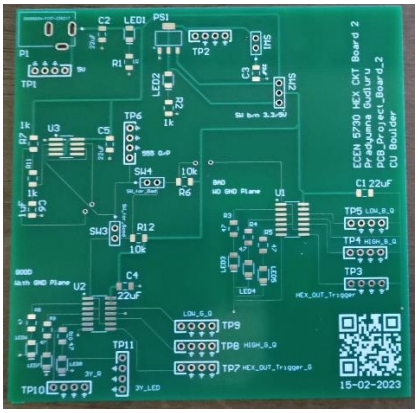
Based on the above requirements, the schematic design is as below:

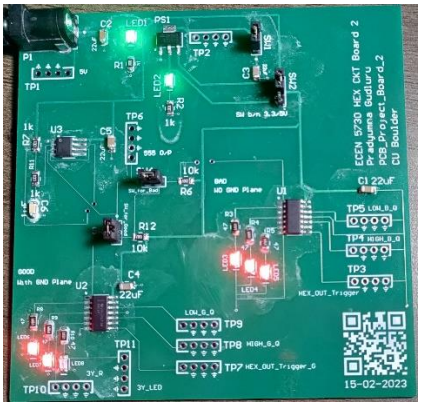


The layout for the above schematic is designed as follows:



After getting the general PCB from JLCPCB, and the board after soldering all the components looks like the following:





Working:

For the board to be in working state,

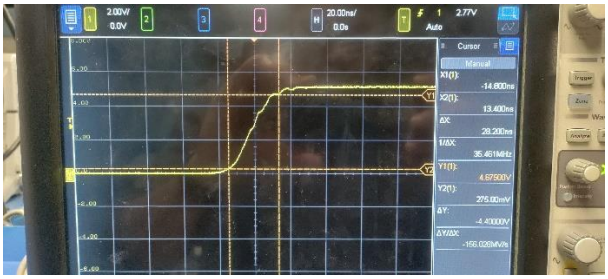
1. The LEDs on 5V and 3.3 V rail should turn ON when connected with power supply.
2. After connecting 3.3V or 5V switch, the 555 Timer output should be visible at TP6 with given voltage and approximately 50% duty cycle.
3. The LEDs should switch ON with good and bad layouts switched ON.

4. Hex trigger outputs should be probed to see with the inverted signal. Low Q and High Q signals should be probed to see with low voltage and high voltage.

The switches 1 and 2 are used to isolate 3.3V and switch between 5V to 3.3V. The switches 3 and 4 are used to switch ON and OFF 555 timer output to good and bad layout respectively.

The LEDs are used to check with the outputs of 1Y, 2Y and 3Y pins of hex inverter. The scope trigger and input and output pins are checked.

The output is observed at the test points at 3.3V and 5V. The 555 output is visible and the rise time and fall time are observed. The following are the screenshots for input voltage and 555 rise time.



The voltages of 3.3V(on channel green) and 5V(on channel yellow) can be seen as above. According to the observations, the 555 IC timer rise time is 28.2nsec and fall time of the 555 output is 24.8nsec.

Analysis of measurements:

Initially considering the 3.3V rail input to the 555 timer and output switching ON to both bad and good layout. The following is the tabular column for rise time, fall time of the trigger, switching noise of quite High and quiet Low signals at rise and fall switching.

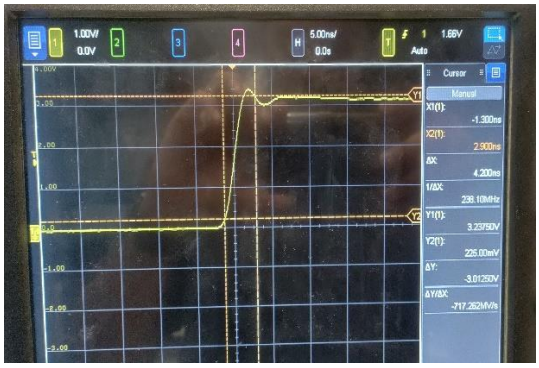
Parameters	**Bad - Bad**	**Good - Good**
3.3V Rail	Bad Decap, Bad GND	Good GND, Good Decap
Rise time trigger signal	7.1 nsec	4.2nsec
Fall time trigger signal	6.1nsec	3.8nsec
Switching noise Q HIGH	at rise time - 612.5mVp-p	at rise time - 560mVp-p
	at Fall time - 968.75mVp-p	at fall time - 320mVp-p
Switching noise Q LOW	at rise time - 790mVp-p	at rise time - 288.75mVp-p
	at Fall time - 820mVp-p	at fall time - 342.5mVp-p

Switching Time:

The Bad-Bad layout is with Bad decoupling capacitor placement (far from IC) and with no ground plane. The Good- Good layout is with decoupling capacitor placed near to the IC and with a GND plane. The trigger rise time for Bad-Bad layout is 7.8nsec and fall time is around 6.1nsec, whereas for the good-good layout it is 4.2nsec and 3.8nsec respectively.

The following are the screenshots for rise time of good-good and bad-bad layout.

Rise time of Bad-Bad layout

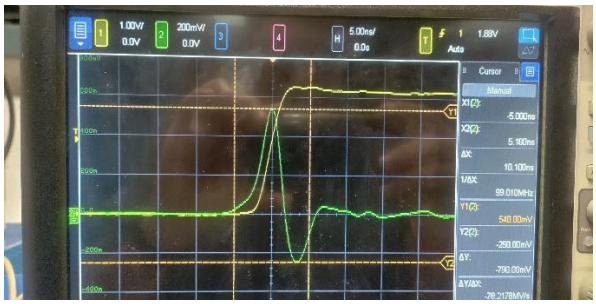


Rise time of Good-Good layout

Quiet LOW pin out:

The switching noises for quiet LOW signals are 790mV and 820mV approximately at rise time and fall time on a bad-bad layout whereas the noises on a good-good layout are 288.75mV and 342.5mV respectively on rise time and fall time of the trigger signal.

The following are the screenshots for noises at quiet LOW test points for bad-bad layout and good-good layout.



Q_LOW noise at Rise time of bad-bad layout

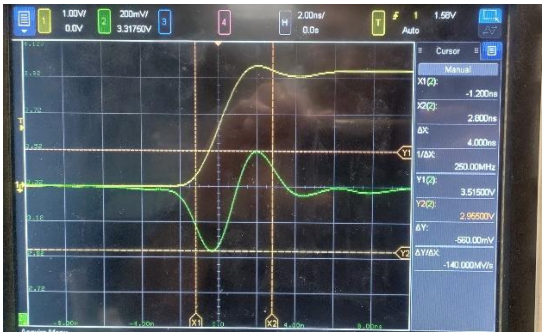
Q_LOW noise at rise time of good-good layout

Quiet HIGH pin out:

The switching noises for quiet HIGH signals are 612.5mV and 968.75mV at the rise time and fall time on a bad-bad layout, whereas the noises on a good-good layout are 560mV and 320mV respectively for rise time and fall time of the trigger signal.

The following are the screenshots for noises at quiet HIGH test points for bad-bad layout and good-good layout.

Q_HIGH noise at rise time of Bad-Bad



Q_HIGH noise at rise time of good-good

There is a decrease in noise with a good layout when compared with a bad layout. There is also a considerable delay in rise time and fall time of the bad layout when compared with good layout. The major reason for the good layout to have a reduced noise while switching and reduced delay in rise and fall time is due to a GND plane all through the layout and having a decoupling capacitor as near to the IC as possible. This reduces the ripples caused by power changes while switching which gives the low noise.

To calculate the Thevenin's Resistance:

The voltage difference across the resistor of 47Ohm resistor on 3Y pin of good layout is given by,

V = 2.7125 – 2.0325 = 0.68V

Resistance, R = 47 Ohm

The current passing through that line is given by 0.68/47 = 14.4mA

For the Thevenin resistance, we calculate the voltage drop due to connecting the load. When no load is connected the voltage is 3.28V, when connected it is 2.0325V. Hence, the equivalent resistance is given by,

$R_L = 3.28/ (14.4*3)*10^{-3} = 76.4$Ohms

$R_{th} = ((V_{th} – V_L)/V_L)*R_L = ((3.28-2.0325)/2.0325)*76.4 = 46.89$ Ohms ~ 47Ohms.

5V Rail – Measurement and Analysis:

The rise time of 555 output of the hex trigger output and the noise at quiet low and quiet high pins are 26.9nsec, 2.6nsec, 1.3V and 550mV. The noise is increased, and the rise time is slightly decreased when the voltage rail is changed from 3.3V to 5V.

The following are the screenshots of rise time of hex trigger of good layout at 5V input and switching noises at 5V for quiet low and quiet high signals.

Rise time of the hex trigger of good layout with 5V

In the above screenshot, the channel-1(yellow curve) is the noise at quiet HIGH pin of the hex inverter. Channel -2 (green curve) is the noise at the quiet LOW pin of the hex inverter. The channel -3(blue curve) is the hex inverter trigger signal at rise time switching.

Math Function Analysis on Oscilloscope:

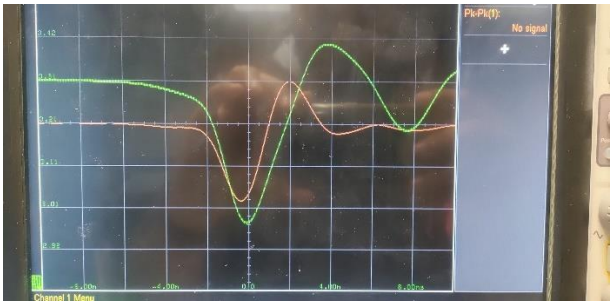
The math function is enabled for finding the voltage between quiet HIGH and quiet LOW pins on the 3.3V rails and 5V rails. The screenshots are as follows.

The voltage obtained with the math function of subtracting channel 1 with channel 2 is 3.24456V. In the above screenshot, the 3.3V rail is the input to the 555 timer and the good layout is switched ON. The channel-1(yellow curve) is a quiet HIGH pin. The channel-2(green curve) is a quiet LOW pin. The channel – 3(blue curve) is the hex trigger output pin. The purple curve is the math function output.

The voltage obtained with the math function of subtracting channel 1 with channel 2 is 5.45209V. In the above screenshot, the 5V rail is the input to the 555 timer and the good layout is switched ON. The channel-1(yellow curve) is a quiet HIGH pin. The channel-2(green curve) is a quiet LOW pin. The channel – 3(blue curve) is the hex trigger output pin. The purple curve is the math function output.

Output Analysis:

The following are the screenshots of good layout and bad layout differences of noises at rise time for quiet HIGH and quiet LOW pins.



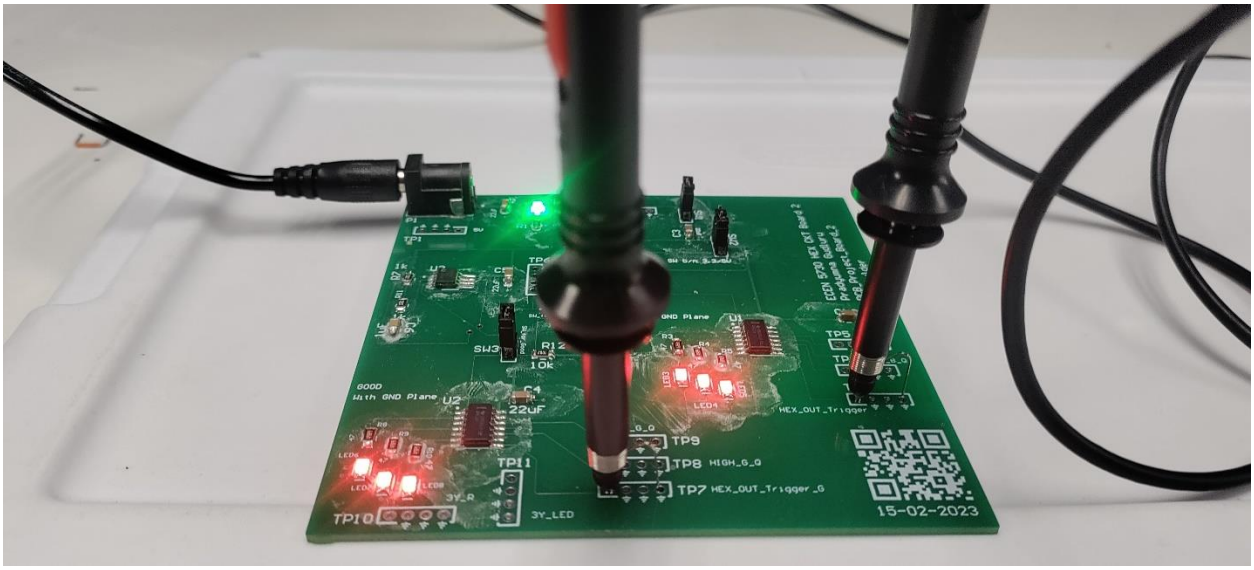
At Quiet HIGH pin

At Quiet LOW pin

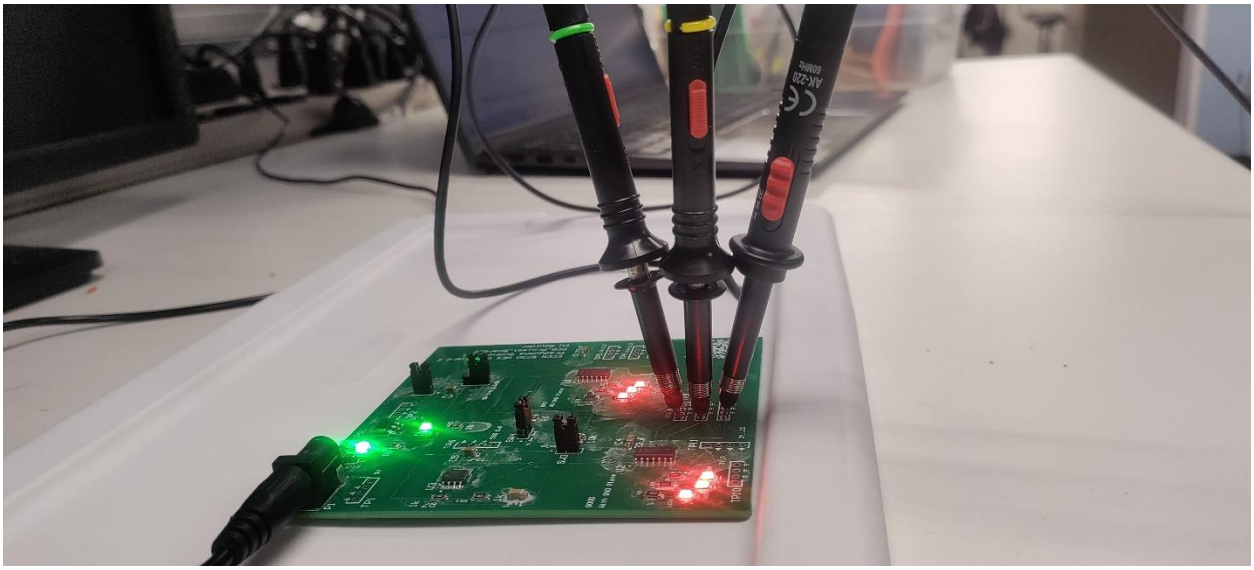
The stored(reference) signal with bad layout and the channel signal is the signal with good layout. There is not much of a difference for a quiet HIGH noise signals as observed and noted in the table, whereas there is a notable change in the quiet LOW signal.

Best practices in design and measurement:

Some of the best design practices like isolating switches, connecting the ground plane on the layout, identifying the blocks of orientation on schematic helped is understanding and profiling signals on the PCB. Labelling every component and the test points made soldering and probing easier. The signals are probed using the spring tip edges which reduce the noise while signal transmission of profiling. The following are screenshots of measurement techniques used to probe for signals at various test points.



The probes are attached to HEX output trigger points of good layout and bad layout simultaneously.



The probes are attached to the good layout with three input channels to the oscilloscope, one for quiet HIGH, one for Quiet LOW and one for hex trigger output.

Analysis of project:

The placing of GND plane is always required to reduce the noise while switching signals are used in the design. Hence, the ground plane is essential when designing a PCB board.

There is a considerable amount of change in reduction of noise and switching rise and fall time when the decoupling capacitor is placed nearest to the switching IC. Hence, it is essential to place the decoupling capacitor as near as possible to the IC.

The resistors are connected first to the output pins and the LEDs are connected at the HEX inverter output pins of 1Y, 2Y and 3Y. This has caused a problem in calculating the current passing through the pins. This also increased the number of test points on the circuit. Hence, from future designs, I would investigate this and connect LEDs and then resistors connected to ground.

There are no hard errors identified in the circuit design.

The soft errors detected are with the LED and resistor connections on the outputs of HEX inverter. The bad layout can also be considered as a soft error, which increases the switching noise and switching time. This can be configured by adding a ground plane to the design and placing a decoupling capacitor nearer to the IC.

References:

1. Lab manual provided by Prof. Eric Bogatin
2. https://sites.google.com/colorado.edu/practicalpcbdesignmanufacture/erics-altium-workshop