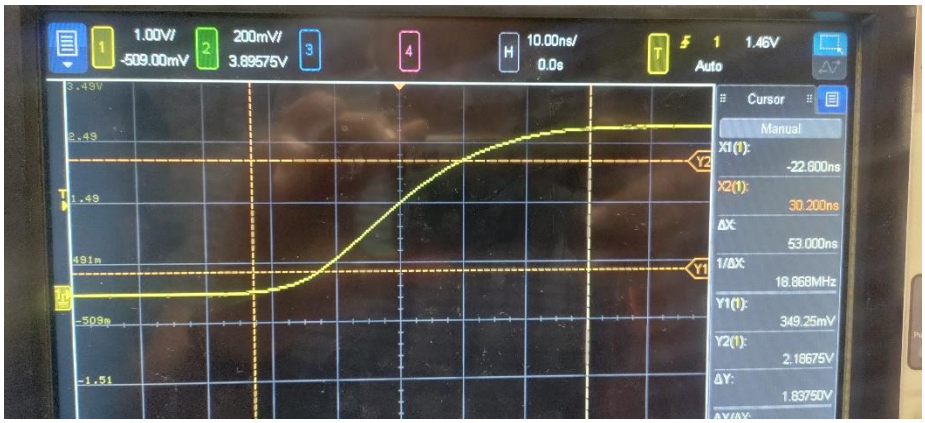
Lab 15 Report:

Good-Bad switching noise board

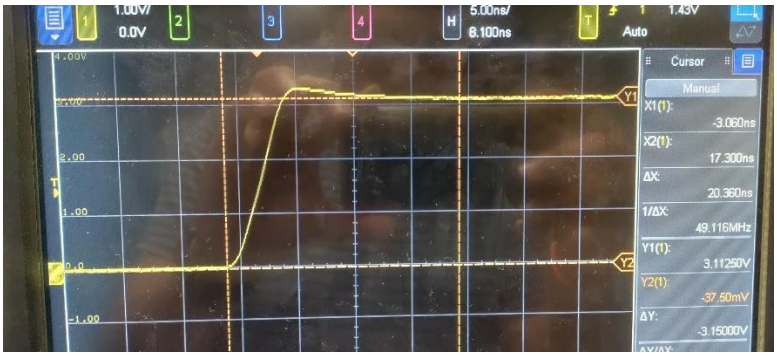
Name: Pradyumna Gudluru Date: 03-05-23

Purpose: Measure some of the switching properties of a version of your board 2

According to the lab manual, the measurements regarding the rise time of hex scope trigger output and 555 timer outputs are, 14.2ns on a bad-bad layout, 6.3ns on a good-good layout and 44ns on a 555 timer output. The following are the screenshots for the signal measurements.



The above screenshot shows the rise curve of 555 timer output.



The above screenshot shows the rising curve of hex trigger output on good-good layout.

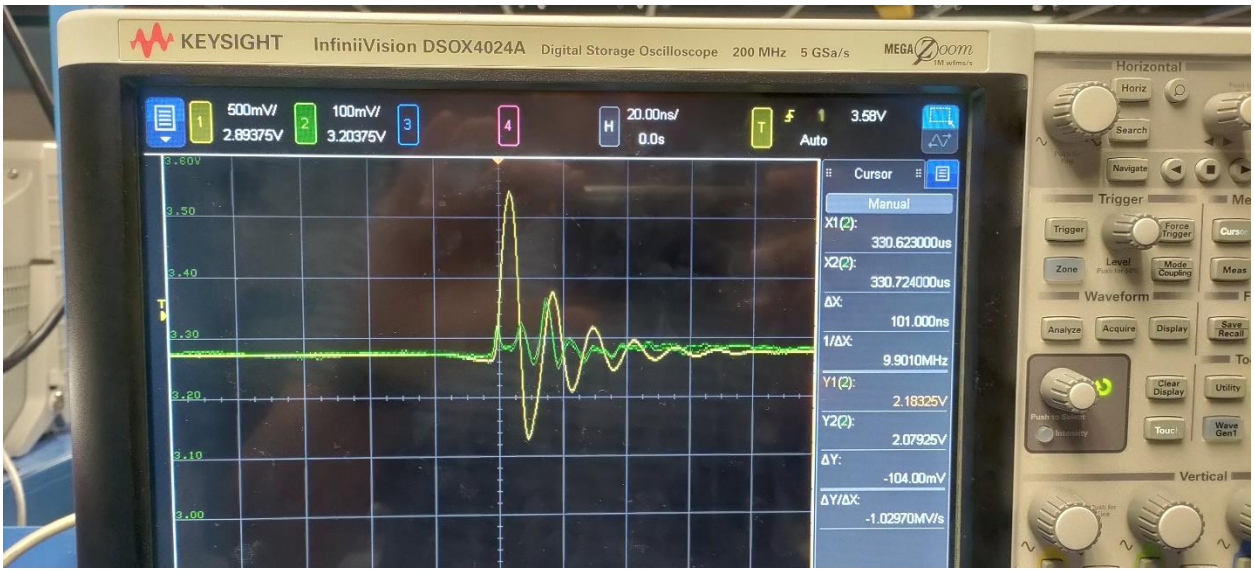
The above screenshot shows the rising curve of hex trigger on bad-bad layout.

The following is the tabular column for rise time fall time, switching noise of Q high and Q low of the Good-Good (with GND plane and decoupling capacitor near to IC), Good – Bad(with GND plane and decoupling capacitor far form IC) and Bad – Bad (with no GND plane and decoupling capacitor far from IC) layouts.

Parameters	**Bad - Bad**	**Good - Bad**	**Good Good**
	Bad Decap, Bad GND	Good GND, Bad Decap	Good GND, Good Decap
Rise time trigger signal	14.2ns	7.5ns	6.3ns
Fall time trigger signal	78.6ns	9.6ns	7.3ns
Switching noise Q High	at rise time - 790mV	at rise time - 212.50mV	at rise time - 175mV
Switching noise Q Low	at rise time - 367.5 mV	at rise time - 130mV	at rise time - 104mV

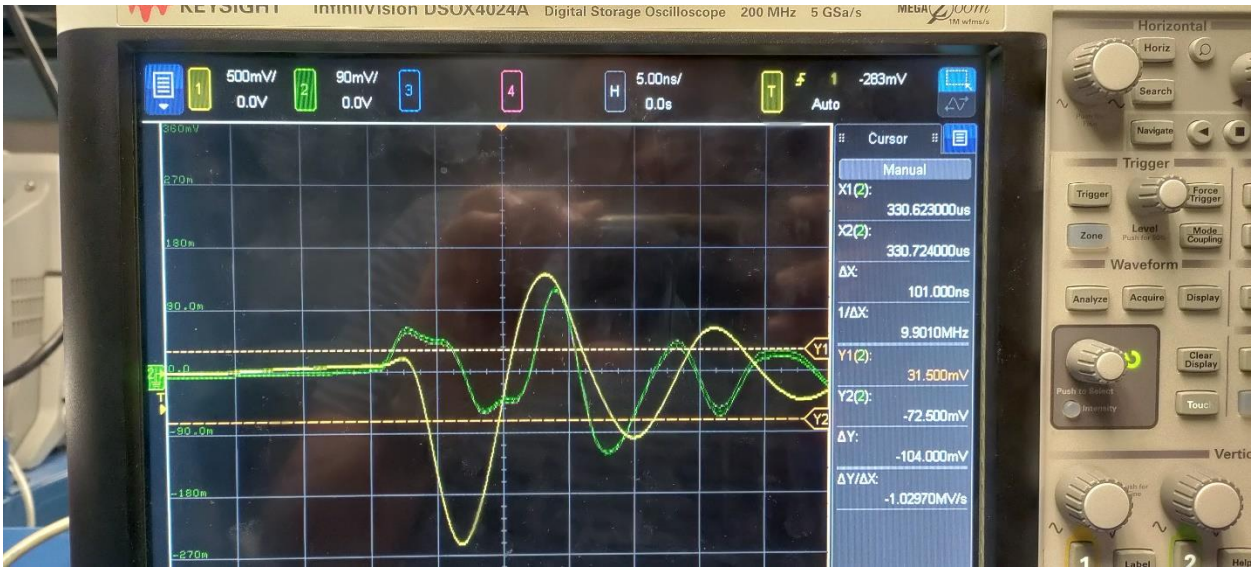
The Q high noise observed in Bad – Bad layout is around 790mV peak to peak whereas on a good – good layout it is 175mV peak to peak. The noise of the bad layout is majorly due to lack of ground plane when compared with good layout.

The following screenshot shows the good and bad layout Q High test point noise signals.



The Q low noise observed in bad – bad layout is 367.5mV whereas it is around 104mV on a good-good layout. The ground plane and the decoupling capacitance are the two main reasons for the reduction of noise while switching.

The following is the screenshot for Q low noise signals for good and bad layouts.



The features like common ground plane and placement of decoupling capacitor (near to the IC) helped to reduce the noise.

The switching noise is approximately 21mV on a 5V power rail when connected to a good layout and approximately 23mV when connected to a bad layout. Similarly on a 3.3V power rail, the good layout has a switching noise of 13mV, and a bad layout has 15mV.

Conclusion:

As per the above observations on checking with rise time, fall time, switching noises of quite high and quite low signals on a hex inverter with good and bad layouts, the following are my learnings.

- A common ground plane is required by all means to minimize the signal return path which ensures low noise effect.
- A decoupling capacitor must be placed in close proximity to the IC, as close as possible, so as to reduce the noise and impact of inductance in the power supply to the board.
- The capacitance should be selected with respect to the voltage being supplied and the frequency of the signals being transferred on the board.