----------ASSIGNMENT 2----------

ASIC ASSIGNMENT 2

MT2021523

PRAFFUL CHOUDHARY

QUESTION (1): **(A) sel_sense (24 marks) "sel_sense" is a simple combinational circuit with two inputs and one output. A plain-English behavioral description of the logic is as follows: 1. The circuit has one output, B, and two inputs, A and S 2. The output B is equal to the input A if S = 0 or is equal to the inverse of input A if S = 1.**

(i) Write a simple behavioral Verilog code for sel_sense.

SOLUTION:

In this part first, I wrote a behavioral Verilog code of sel_sense in which I have defined one xor function which will give the same output A whenever the S=0 and otherwise it will provide the ~A as the output.

```
module sel_sense (A,B,S);
input A;
input S;
output B;
assign B=S ? ~A : A;
endmodule
```

Fig:1.1(Behavioral Verilog Code)

(ii) Draw a schematic of a circuit that implements sel_sense. Your schematic must involve gates like NAND2, NOR2, MUX, INVERTER, XOR, NAND, etc. Choose whichever gates you like to implement the logic.

In this part I draw the schematic of the function by using the universal gate (NOR2) and the Truth table of the function.

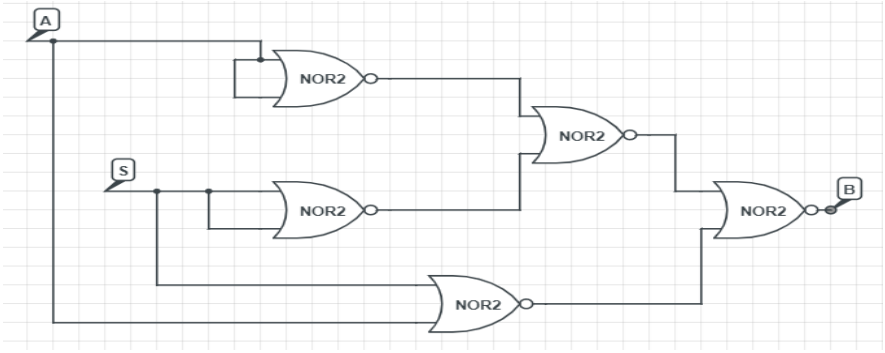


Fig 1.2(NOR2 Gate representation of the xor gate)

(iii) write a truth table for the circuit. Based on your truth-table, if you would like to make an alternative schematic for the circuit, please do so, and you can submit that schematic as well.

A	**S**	**B**
0	0	0
0	1	1
1	0	1
1	1	0

Fig(1.3) Truth table of the XOR Gate

Actual gate which we are aiming to obtain (XOR):

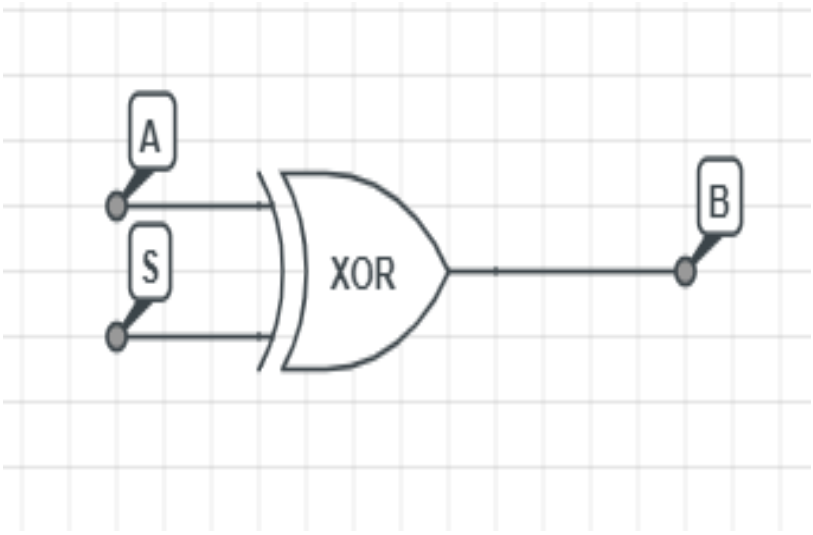


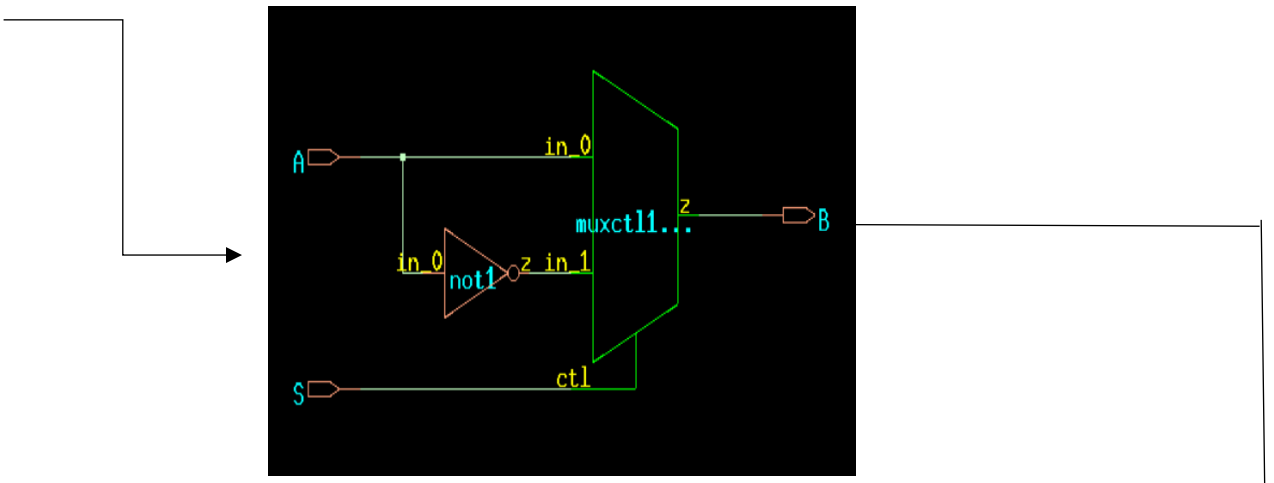
Fig:1.4(schematic of sel_sense)

(iv) Synthesize sel_sense with the SkyWater HS and MS libraries. Use the ss, 150C, 1.6V corner. Specify an output load cap equal to the input pin cap of an X2 buffer, and a max delay from input to output of 50 ps before the optimization step. Submit the resulting netlists, and your synthesis script.

Step:1

After read_hdl sel_sense ----------→ gui_show

We are getting this schematic, this is because after reading the. v file Genus legacy tool automatically generate a schematic with the help of pre-defined gates and components in the tool.



Then after syn_gen command the tool will start to convert the schematic into new one with the help of predefined generic gates

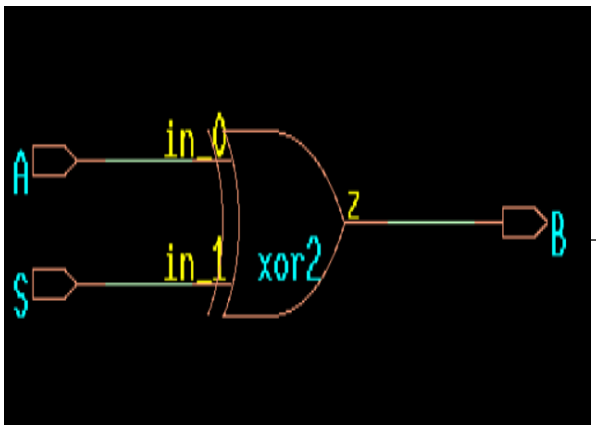


Fig 1.5 (Schematic after syn_gen)

After implementing the syn_map , syn_opt command the we will get the below schematic , this schematic is basically made with the help of sky130_fd_sc_hs__ss_150C_1v60 lib file.

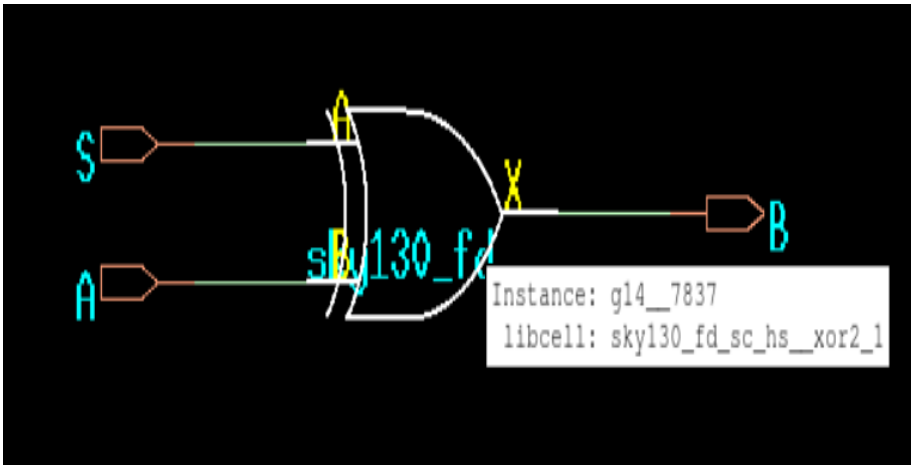


Fig 1.6 (Schematic after syn_opt command with the help of HS file)

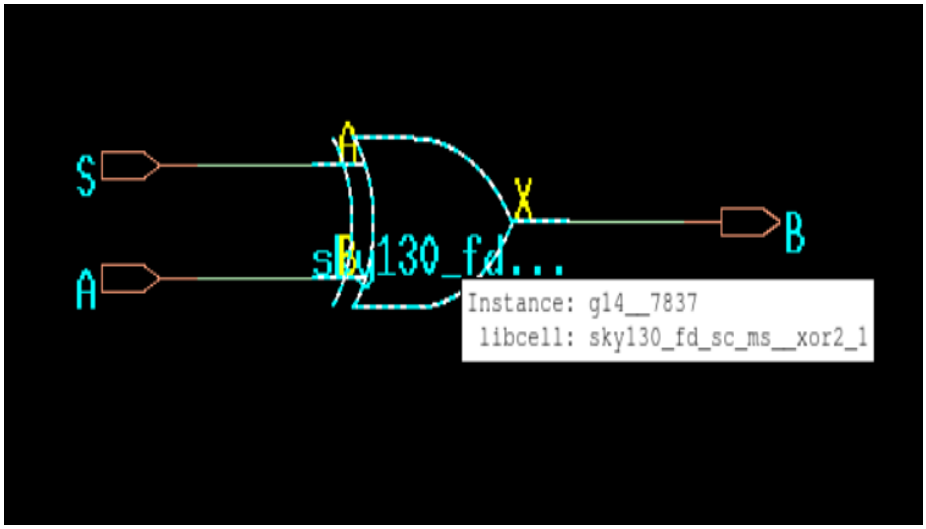


Fig 1.7 (Schematic after syn_opt command with the help of MS file)

Reporting timing /delays with the help of sky130_fd_sc_hs__ss_150C_1v60 lib file.

Path S to B and A to B with input to output delay of 50ps.

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  09:44:00 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_hs__ss_150C_1v60 1.0000000000
  Operating conditions:   max_auto (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

   Pin               Type             Fanout Load Slew Delay Arrival
                                             (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------
S             in port                      1  5.5    0    +0       0 F
g14__7837/A                                            +0       0
g14__7837/X   sky130_fd_sc_hs__xor2_1      1  2.8   70  +171     171 F
B             out port                                 +0     171 F
-------------------------------------------------------------------------
Exception    : 'path_delays/del_2'      50ps
Timing slack :    -121ps (TIMING VIOLATION)
Start-point  : S
End-point    : B
```

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  09:47:13 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_hs__ss_150C_1v60 1.0000000000
  Operating conditions:   max_auto (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

   Pin                 Type             Fanout Load Slew Delay Arrival
                                              (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------
A           <<<  in port                    1  5.0    0    +0       0 F
g14__7837/B                                            +0       0
g14__7837/X      sky130_fd_sc_hs__xor2_1    1  2.8   70  +162     162 F
B           <<<  out port                               +0     162 F
-------------------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'      50ps
Timing slack :    -112ps (TIMING VIOLATION)
Start-point  : A
End-point    : B
```

Fig 1.8 (Report Timings of both path A to B and S to B with the help of hs file)

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  11:00:40 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_ms__ss_150C_1v60 1.0000000000
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

   Pin                 Type             Fanout Load Slew Delay Arrival
                                              (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------
A           <<<  in port                    1  5.2    0    +0       0 F
g14__7837/B                                            +0       0
g14__7837/X      sky130_fd_sc_ms__xor2_1    1  2.8   69  +193     193 F
B           <<<  out port                               +0     193 F
-------------------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'      50ps
Timing slack :    -143ps (TIMING VIOLATION)
Start-point  : A
End-point    : B
```

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  11:07:41 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_ms__ss_150C_1v60 1.0000000000
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

   Pin               Type             Fanout Load Slew Delay Arrival
                                             (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------
S             in port                      1  5.7    0    +0       0 F
g14__7837/A                                            +0       0
g14__7837/X   sky130_fd_sc_ms__xor2_1      1  2.8   69  +204     204 F
B             out port                                 +0     204 F
-------------------------------------------------------------------------
Exception    : 'path_delays/del_2'      50ps
Timing slack :    -154ps (TIMING VIOLATION)
Start-point  : S
End-point    : B
```

Fig 1.9 (Report Timings of both path A to B and S to B with the help of ms file)

(v) Put a “don’t use” on all XOR and XNOR gates, resynthesize, and submit the resulting netlists for both HS and MS libraries.

DON’T_USE XOR, XNOR IN SKY hs file

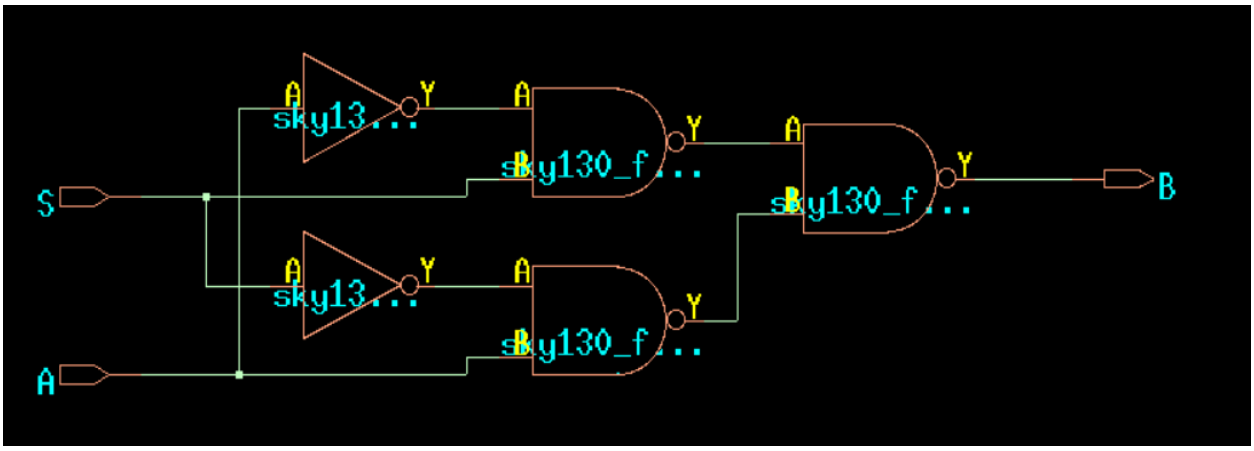


Fig 1.10 Schematic without xor,xnor gate with hs file

```
module sel_sense(A, B, S);
  input A, S;
  output B;
  wire A, S;
  wire B;
  wire n_13, n_14, n_15, n_16;
  sky130_fd_sc_hs__nand2_1 g16(.A (n_14), .B (n_16), .Y (B));
  sky130_fd_sc_hs__nand2_2 g18(.A (n_13), .B (S), .Y (n_14));
  sky130_fd_sc_hs__inv_8 g20(.A (A), .Y (n_13));
  sky130_fd_sc_hs__nand2_2 g17(.A (n_15), .B (A), .Y (n_16));
  sky130_fd_sc_hs__inv_16 g19(.A (S), .Y (n_15));
endmodule
```

Netlist1(netlist after don’t use xor and xnor in hs)

DON’T USE XOR, XNOR IN SKY MS file

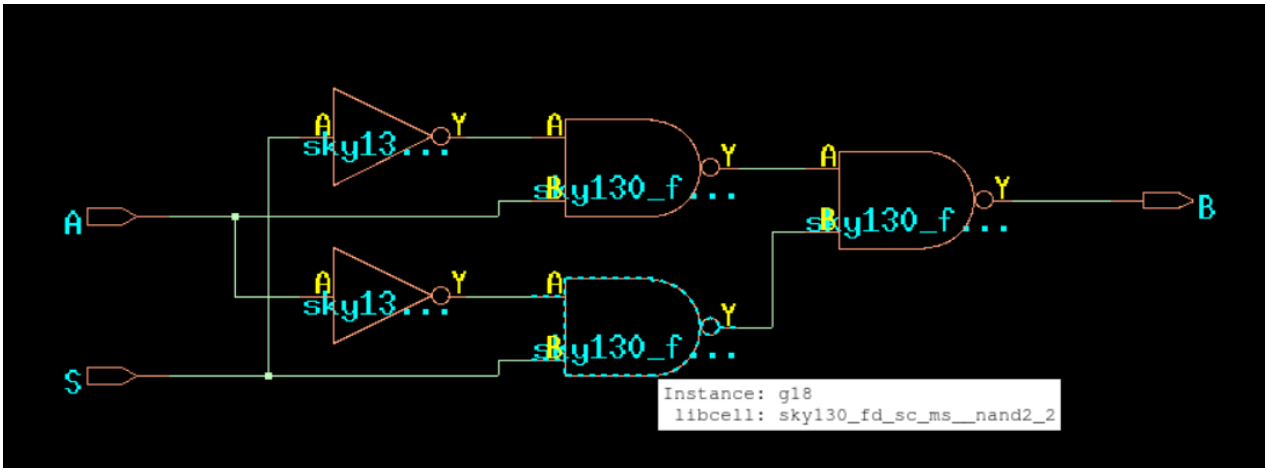


Fig 1.11 Schematic without xor,xnor gate with ms file

```
module sel_sense(A, B, S);
  input A, S;
  output B;
  wire A, S;
  wire B;
  wire n_17, n_18, n_19, n_20;
  sky130_fd_sc_ms__nand2_1 g16(.A (n_18), .B (n_20), .Y (B));
  sky130_fd_sc_ms__nand2_2 g17(.A (n_17), .B (A), .Y (n_18));
  sky130_fd_sc_ms__inv_8 g19(.A (S), .Y (n_17));
  sky130_fd_sc_ms__nand2_2 g18(.A (n_19), .B (S), .Y (n_20));
  sky130_fd_sc_ms__inv_16 g20(.A (A), .Y (n_19));
endmodule
```

Netlist2:(netlist after don’t use xor and xnor in hs)

AFTER DON’T_USE_XOR_XNOR_HS

```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  10:47:27 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_hs__ss_150C_1v60 1.0000000000
  Operating conditions:   max_auto (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

Pin                Type             Fanout Load Slew Delay Arrival
                                           (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------
A     <<<  in port                      2 27.6    0    +0       0 F
g20/A                                                 +0       0
g20/Y      sky130_fd_sc_hs__inv_8       1  5.8   23   +26      26 R
g18/A                                                 +0      26
g18/Y      sky130_fd_sc_hs__nand2_2     1  3.0   37   +45      71 F
g16/A                                                 +0      71
g16/Y      sky130_fd_sc_hs__nand2_1     1  2.8   53   +52     124 R
B     <<<  out port                                    +0     124 R
-------------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'      50ps
Timing slack :     -74ps (TIMING VIOLATION)
Start-point  : A
End-point    : B
```

```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  10:41:51 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_hs__ss_150C_1v60 1.0000000000
  Operating conditions:   max_auto (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

Pin              Type             Fanout Load Slew Delay Arrival
                                         (fF) (ps)  (ps)   (ps)
-----------------------------------------------------------------
S       in port                       2 51.8    0    +0       0 F
g19/A                                               +0       0
g19/Y   sky130_fd_sc_hs__inv_16       1  5.8   19   +23      23 R
g17/A                                               +0      23
g17/Y   sky130_fd_sc_hs__nand2_2      1  2.9   37   +43      66 F
g16/B                                               +0      66
g16/Y   sky130_fd_sc_hs__nand2_1      1  2.8   53   +60     126 R
B       out port                                    +0     126 R
-----------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'      50ps
Timing slack :     -76ps (TIMING VIOLATION)
Start-point  : S
End-point    : B
```

Fig 1.12 (Report Timings of both path A to B and S to B with the help of hs file without xor,xnor gates)

AFTER DON’T_USE_XOR_XNOR_MS

```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  11:19:28 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_ms__ss_150C_1v60 1.0000000000
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

Pin              Type             Fanout Load Slew Delay Arrival
                                         (fF) (ps)  (ps)   (ps)
-----------------------------------------------------------------
A       in port                       2 54.7    0    +0       0 F
g20/A                                               +0       0
g20/Y   sky130_fd_sc_ms__inv_16       1  6.0   22   +28      28 R
g18/A                                               +0      28
g18/Y   sky130_fd_sc_ms__nand2_2      1  3.1   37   +45      74 F
g16/B                                               +0      74
g16/Y   sky130_fd_sc_ms__nand2_1      1  2.8   60   +69     142 R
B       out port                                    +0     142 R
-----------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'      50ps
Timing slack :     -92ps (TIMING VIOLATION)
Start-point  : A
End-point    : B
```

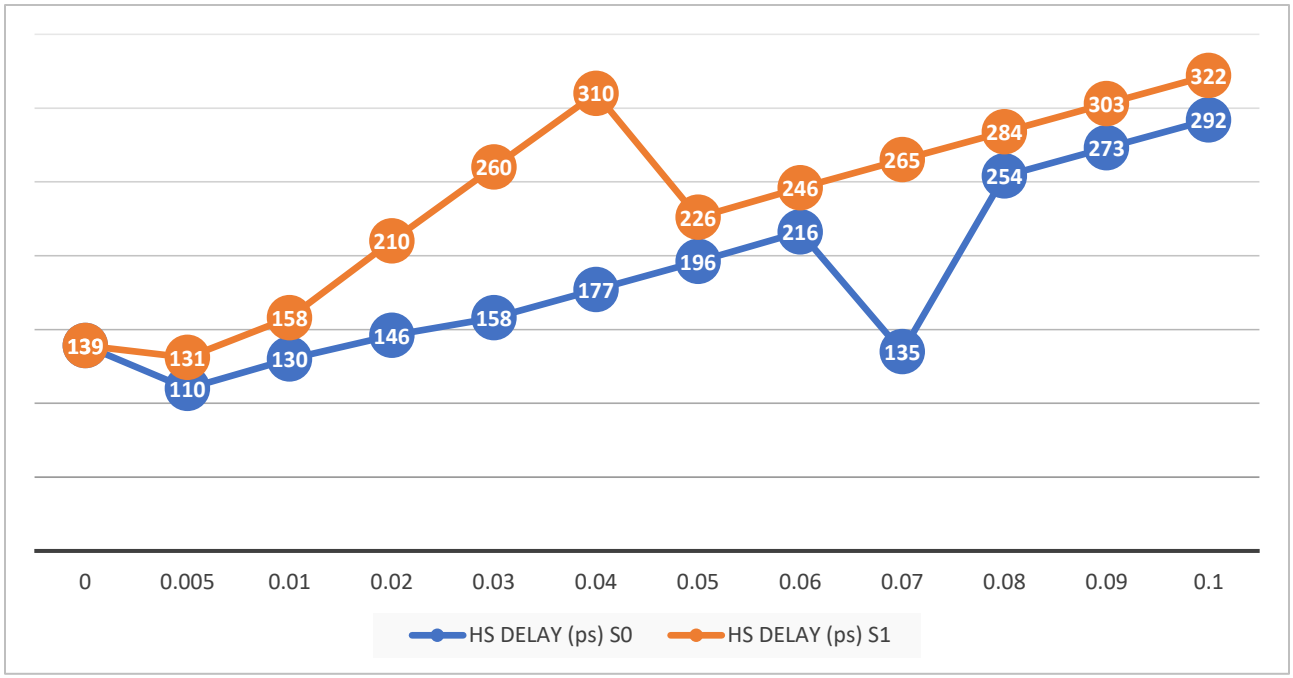
```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 22 2021  11:26:06 pm
  Module:                 sel_sense
  Technology library:     sky130_fd_sc_ms__ss_150C_1v60 1.0000000000
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

Pin                Type             Fanout Load Slew Delay Arrival
                                           (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------
S     <<<  in port                      2 29.7    0    +0       0 F
g19/A                                                 +0       0
g19/Y      sky130_fd_sc_ms__inv_8       1  6.0   26   +32      32 R
g17/A                                                 +0      32
g17/Y      sky130_fd_sc_ms__nand2_2     1  3.0   36   +46      78 F
g16/A                                                 +0      78
g16/Y      sky130_fd_sc_ms__nand2_1     1  2.8   60   +60     138 R
B     <<<  out port                                    +0     138 R
-------------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'      50ps
Timing slack :     -88ps (TIMING VIOLATION)
Start-point  : S
End-point    : B
```

Fig 1.13 (Report Timings of both path A to B and S to B with the help of ms file without xor,xnor gates)

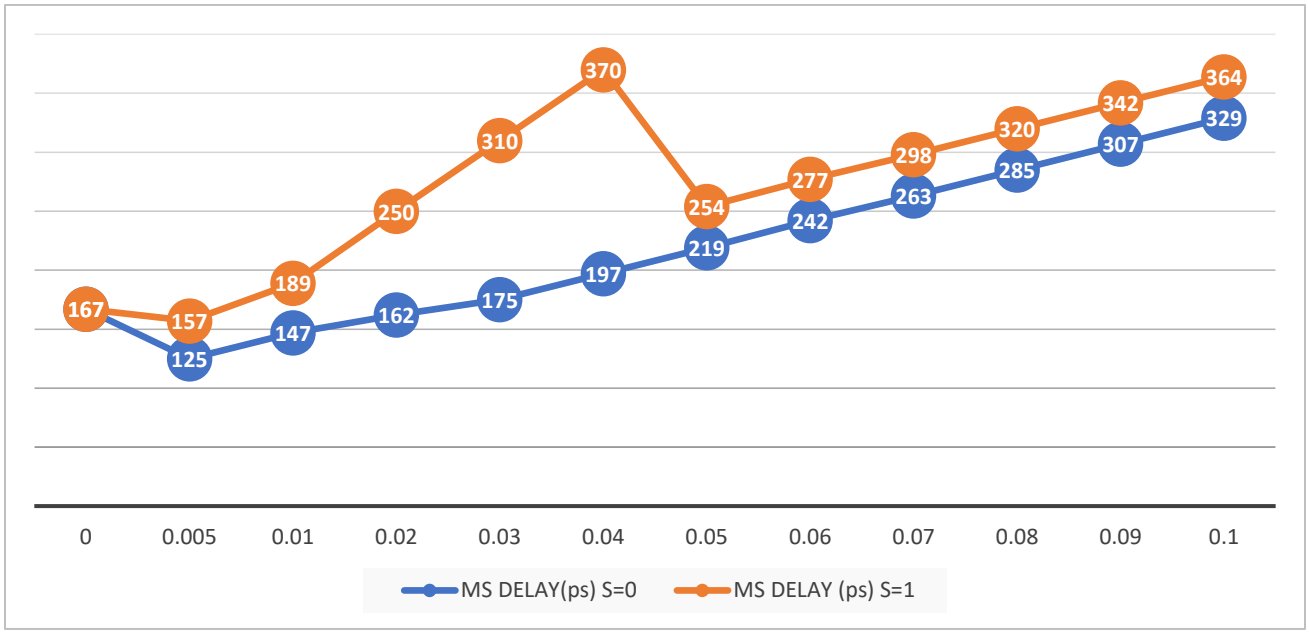
(vi) For the HS and MS netlists with no “don’t use” directives, plot A->B delay as a function of load capacitance at B. Let the capacitance vary from 0.005 to 0.1 pF. For each cap value, report timing before and after doing an incremental optimization (-incr option). Create plots for S = 0 and for S = 1. Let transition time at A be 0.04 ns. Note that for timing to be reported from A to B, you will need to specify a max delay constraint for that path.

CAPACITANCES (Pf)	HS DELAY (ps) S=0	HS DELAY (ps) S=1	MS DELAY (ps) S=0	MS DELAY (ps) S=1
0.000	139	139	167	167
0.005	110	131	125	157
0.010	130	158	147	189
0.020	146	210	162	250
0.030	158	260	175	310
0.040	177	310	197	370
0.050	196	226	219	254
0.060	216	246	242	277
0.070	135	265	263	298
0.080	254	284	285	320
0.090	273	303	307	342
0.100	292	322	329	364

Table 1 (Delay Vs Capacitances)



Graph 1(HS delay for S=0, S=1 VS Capacitances)



Graph 2(MS delay for S=0, S=1 VS Capacitances)

Question2)

(B) Buffers in Standard Cell Libraries (6 marks) From the “slow corner” dotlibs of the standard cell libraries in Cadence RAK, and Nangate_15nm_OCL, fill out the table below for the buffer of drive strength 2: [The number of rows in the table is only for the purpose of indication] Cell Name Name of Input Pin Capacitance of Input Pin (pF)

CELL NAME	NAME OF INPUT PIN	CAPACITANCE OF INPUT PIN
BUF_X2(slow.lib of Cad RAK max)	PIN-A	0.00060159pF
BUF_X2(nangate_15nm_OCL_slow_conditional_nldm.lib)	PIN-I	0.839939fF

Table 2: (Calculating the capacitances in standard files)

```
prafful@prafful-Lenovo-ideapad-310-15IKB:~/homework2$ grep -A 50 'cell (BUFX2)' slow.lib | grep -A 5 'pin(A)'
  pin(A)  {
    direction : input;
    input_signal_level : RAIL_VDD;
    capacitance : 0.000601595;
    rise_capacitance : 0.000601052;
    fall_capacitance : 0.000601595;
```

Fig 1.14(Showing the capacitance and input pin in CADENCE RAK)

```
prafful@prafful-Lenovo-ideapad-310-15IKB:~/homework2$ grep -A50 'cell (BUF_X2' NanGate_15nm_OCL_slow_conditional_nldm.lib | grep -A8 'pin (I)'
      pin (I) {

            direction             : input;
            related_power_pin     : "VDD";
            related_ground_pin    : "VSS";
            capacitance           : 0.839939;
            fall_capacitance      : 0.841850;
            rise_capacitance      : 0.838029;
            fall_capacitance_range        (0.613036, 0.966941);
```

Fig 1.15(Showing the capacitance and input pin in Nangate15nm)

QUESTION (3)

(i) Write behavioral Verilog code for a combinational logic function called “mux_comparator” that compares two three-bit numbers x and y, and outputs whichever one of the two numbers is numerically less. Output should be called z. Verify it simulates as expected

```
module mux_comparator(x,y,z);
input [2:0] x;
input [2:0] y;
output reg[2:0] z;
always @(*)
begin
 if(x>y)  z=y;
 else if(x<y) z=x;
 else z=0;
end
 endmodule
```

Fig 1.16(Behavioral Verilog code for mux_comparator)

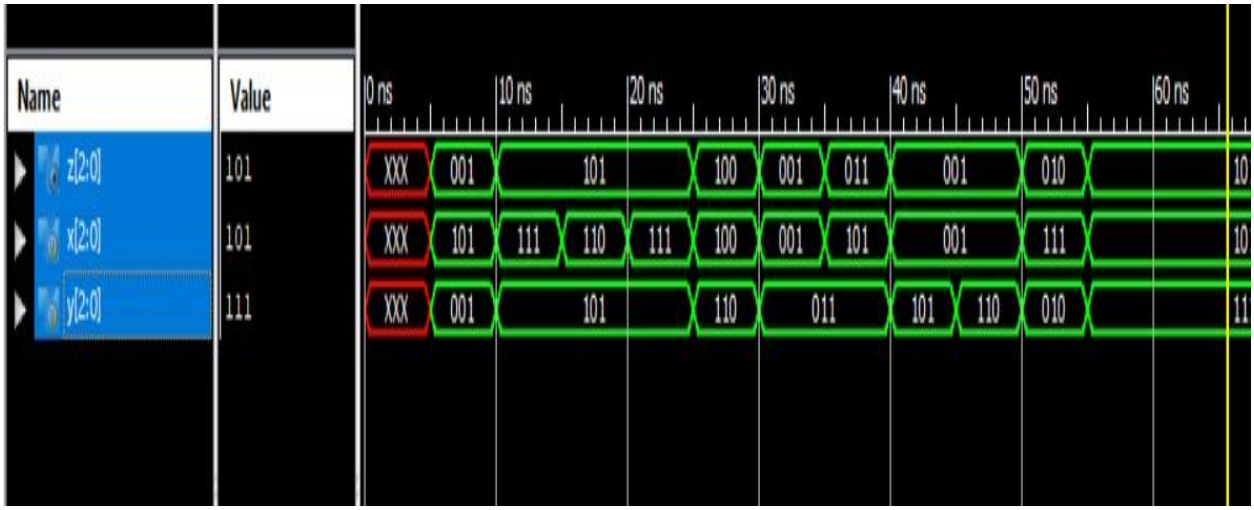


Fig 1.17(Simulation result of mux_comparator)

(ii) Specify the load capacitance at all outputs to be equal to the input pin capacitance of a drive-strength=2 buffer from the standard cell library, using the table you generated in Section B. Specify the transition time at all inputs to be 100 ps. Set a “max delay” constraint of 250 ps from all Put this value in the table Don’t put this value in the table inputs to all outputs. Put these specifications in an SDC file called “mux_comparator_.sdc”

```
set_input_transition -rise 0.1 [get_ports "x"]
set_input_transition -rise 0.1 [get_ports "y"]
set_input_transition -fall 0.1 [get_ports "x"]
set_input_transition -fall 0.1 [get_ports "y"]

set_max_delay 0.25 -from x -to z
set_max_delay 0.25 -from y -to z
set_load 0.000601595 z
```

Fig (1.18 SDC file for mux_comparator for Cadence_RAK)

HERE I ASSUME that 0.839939pF capacitance rather that 0.000839939 it gives me a different schematic when I changed the load capacitance, I tried out this load and found out something really new, here the schematic is without any unknown combinational box

```
set_input_transition -rise 0.1 [get_ports "x"]
set_input_transition -rise 0.1 [get_ports "y"]
set_input_transition -fall 0.1 [get_ports "x"]
set_input_transition -fall 0.1 [get_ports "y"]

set_max_delay 0.25 -from x -to z
set_max_delay 0.25 -from y -to z
set_load 0.839939 z
```

Fig (1.19 SDC file for mux_comparator for Nan_Gate15nm)

(iii) Synthesize this function with the libraries Cadence RAK and Nangate_15nm_OCL. Submit the three netlists that result

a) CADENCE_RAK

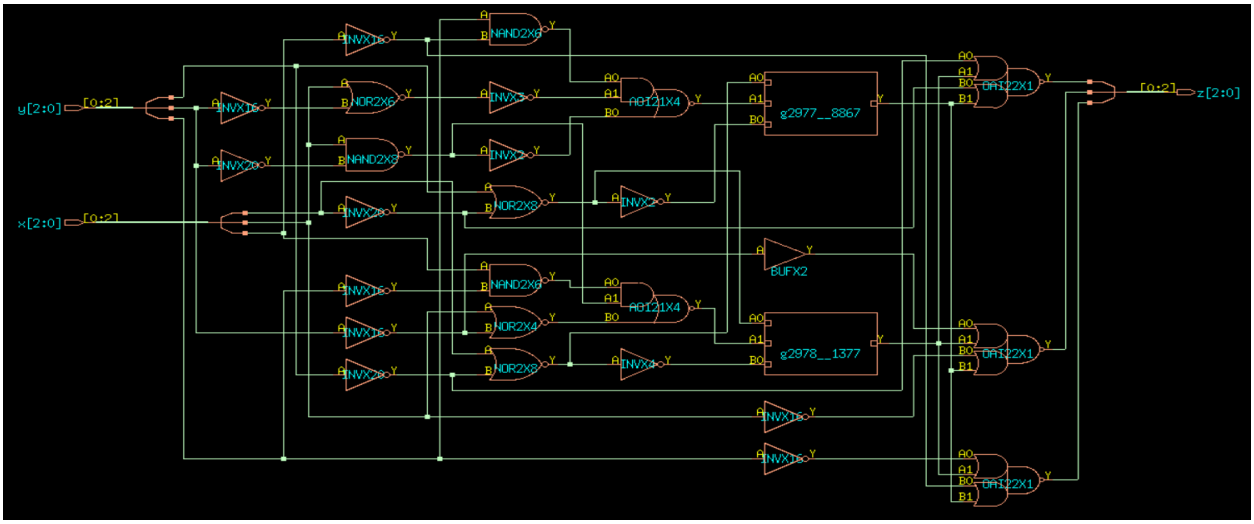


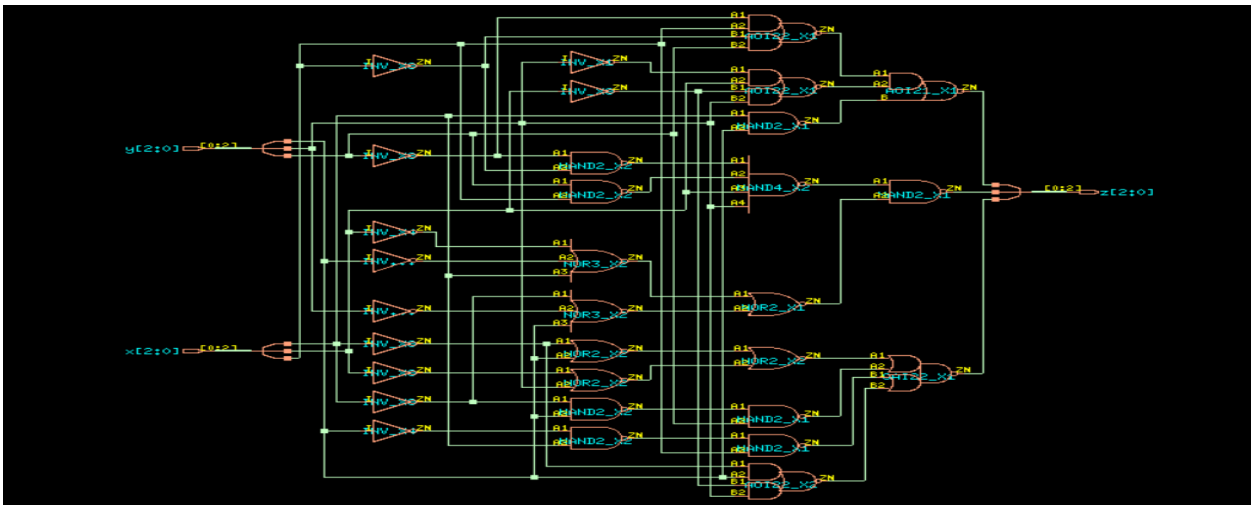
Fig (1.20 Schematic of mux_comparator after using Cadence_RAK)

```
module mux_comparator(x, y, z);
  input [2:0] x, y;
  output [2:0] z;
  wire [2:0] x, y;
  wire [2:0] z;
  wire n_0, n_2, n_3, n_4, n_5, n_8, n_9, n_10;
  wire n_11, n_13, n_15, n_16, n_17, n_19, n_20, n_49;
  wire n_50, n_51, n_52, n_53, n_54, n_55, n_56, n_58;
  wire n_59;
  OAI22X1 g2974__7837(.A0 (n_4), .A1 (n_20), .B0 (n_5), .B1 (n_19), .Y
       (z[2]));
  OAI21X4 g2977__8867(.A0 (n_10), .A1 (n_17), .B0 (n_9), .Y (n_19));
  OAI21X4 g2978__1377(.A0 (n_8), .A1 (n_16), .B0 (n_11), .Y (n_20));
  AOI21X4 g2979__3717(.A0 (n_3), .A1 (n_15), .B0 (n_13), .Y (n_17));
  AOI21X4 g2980__4599(.A0 (n_59), .A1 (n_55), .B0 (n_50), .Y (n_16));
  INVX3 g2987(.A (n_53), .Y (n_15));
  INVX2 g2981(.A (n_55), .Y (n_13));
  INVX4 g2982(.A (n_10), .Y (n_11));
  INVX2 g2983(.A (n_8), .Y (n_9));
  NOR2X8 g2986__2007(.A (y[2]), .B (n_5), .Y (n_8));
  NOR2X8 g2985__1237(.A (x[2]), .B (n_4), .Y (n_10));
  NAND2X6 g2989__1297(.A (y[0]), .B (n_2), .Y (n_3));
  INVX16 g2995(.A (x[1]), .Y (n_0));
  INVX20 g2996(.A (x[2]), .Y (n_5));
  INVX16 g2992(.A (x[0]), .Y (n_2));
  INVX20 g2994(.A (y[2]), .Y (n_4));
  OAI22X1 g2975__3002(.A0 (n_51), .A1 (n_20), .B0 (n_0), .B1 (n_19), .Y
       (z[1]));
  NOR2X4 g2990_dup__3010(.A (x[1]), .B (n_49), .Y (n_50));
  INVX16 g3003_dup(.A (y[1]), .Y (n_49));
  BUFX2 g3011(.A (n_49), .Y (n_51));
  NOR2X6 g2998__3012(.A (x[1]), .B (n_52), .Y (n_53));
  INVX16 g3013(.A (y[1]), .Y (n_52));
  NAND2X8 g2984__3014(.A (x[1]), .B (n_54), .Y (n_55));
  INVX20 g3008_dup(.A (y[1]), .Y (n_54));
  OAI22X1 g2976__3015(.A0 (n_56), .A1 (n_20), .B0 (n_2), .B1 (n_19), .Y
       (z[0]));
  INVX16 g3016(.A (y[0]), .Y (n_56));
  NAND2X6 g2988__3017(.A (x[0]), .B (n_58), .Y (n_59));
  INVX16 g2991_dup(.A (y[0]), .Y (n_58));
endmodule
```

Netlist3: (netlist after of mux_comparator after using cadence_RAK)

NanGate_15nm_OCL_slow_conditional_nldm

This circuit is more understandable because all the gates are used here rather than any particular unknown box.

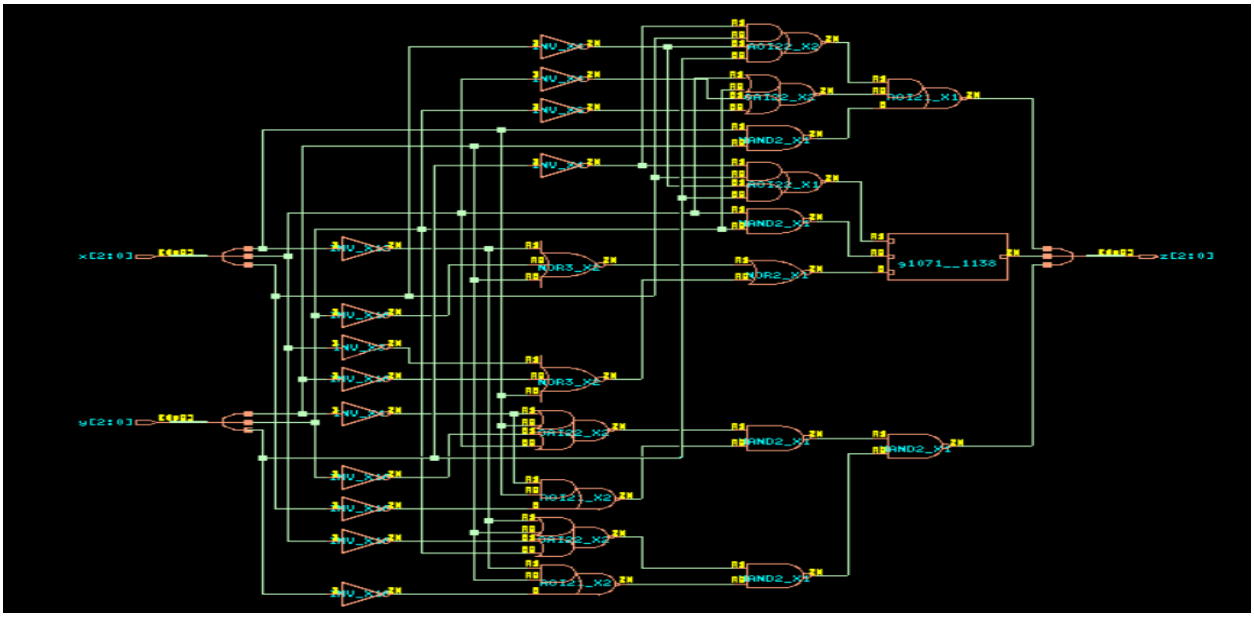


Fig(1.21 Schematic of mux_comparator after using NanGate_15nm_OCL_slow_conditional_nldm)

```
module mux_comparator(x, y, z);
  input [2:0] x, y;
  output [2:0] z;
  wire [2:0] x, y;
  wire [2:0] z;
  wire n_2, n_12, n_48, n_111, n_117, n_137, n_139, n_140;
  wire n_141, n_251, n_296, n_297, n_298, n_299, n_300, n_301;
  wire n_302, n_303, n_306, n_313, n_314, n_315, n_320, n_321;
  wire n_322, n_349, n_350, n_351;
  AOI21_X1 g1069__7654(.A1 (n_48), .A2 (n_12), .B (n_2), .ZN (z[2]));
  AOI22_X1 g1078__2006(.A1 (n_117), .A2 (x[1]), .B1 (n_302), .B2
       (y[1]), .ZN (n_12));
  NAND2_X1 g1083__6789(.A1 (x[2]), .A2 (y[2]), .ZN (n_2));
  AOI22_X1 g1079__1099(.A1 (n_137), .A2 (x[0]), .B1 (n_306), .B2
       (y[0]), .ZN (n_48));
  INV_X8 g18(.I (x[2]), .ZN (n_111));
  INV_X1 g31(.I (y[1]), .ZN (n_117));
  NAND2_X1 g259(.A1 (n_141), .A2 (n_322), .ZN (z[1]));
  NAND4_X2 g66(.A1 (n_139), .A2 (n_140), .A3 (x[1]), .A4 (y[1]), .ZN
       (n_141));
  NAND2_X2 g67(.A1 (n_137), .A2 (n_306), .ZN (n_139));
  INV_X8 g69(.I (y[0]), .ZN (n_137));
  NAND2_X2 g68(.A1 (y[0]), .A2 (x[0]), .ZN (n_140));
  INV_X4 g1134(.I (y[2]), .ZN (n_251));
  OAI22_X1 g287(.A1 (n_296), .A2 (n_298), .B1 (n_300), .B2 (n_303), .ZN
       (z[0]));
  NOR2_X2 g290(.A1 (n_313), .A2 (n_315), .ZN (n_296));
  NAND2_X1 g289(.A1 (n_297), .A2 (y[0]), .ZN (n_298));
  NAND2_X2 g292(.A1 (n_111), .A2 (y[2]), .ZN (n_297));
  NAND2_X1 g288(.A1 (n_299), .A2 (x[0]), .ZN (n_300));
  NAND2_X2 g293(.A1 (n_251), .A2 (x[2]), .ZN (n_299));
  AOI22_X2 g291(.A1 (n_301), .A2 (y[2]), .B1 (n_302), .B2 (y[1]), .ZN
       (n_303));
  INV_X8 g296(.I (x[2]), .ZN (n_301));
  INV_X8 g298(.I (x[1]), .ZN (n_302));
  INV_X8 g299(.I (x[0]), .ZN (n_306));
  NOR2_X2 g11(.A1 (n_301), .A2 (y[2]), .ZN (n_313));
  NOR2_X2 g1143(.A1 (n_314), .A2 (y[1]), .ZN (n_315));
  INV_X8 g1144(.I (x[1]), .ZN (n_314));
  NOR2_X1 g89(.A1 (n_351), .A2 (n_321), .ZN (n_322));
  NOR3_X2 g90(.A1 (n_111), .A2 (n_320), .A3 (y[2]), .ZN (n_321));
  INV_X16 g93(.I (y[1]), .ZN (n_320));
  NOR3_X2 g21(.A1 (n_349), .A2 (n_350), .A3 (x[2]), .ZN (n_351));
  INV_X4 g24(.I (x[1]), .ZN (n_349));
  INV_X16 g22(.I (y[2]), .ZN (n_350));
endmodule
```

Netlist4: (netlist after of mux_comparator after using NanGate_15nm_OCL_slow_conditional_nldm)

NanGate_15nm_OCL_fast_conditional_nldm



Fig(1.22 Schematic of mux_comparator after using NanGate_15nm_OCL_fast_conditional_nldm)

```
module mux_comparator(x, y, z);
  input [2:0] x, y;
  output [2:0] z;
  wire [2:0] x, y;
  wire [2:0] z;
  wire n_2, n_12, n_48, n_111, n_117, n_137, n_139, n_140;
  wire n_141, n_251, n_296, n_297, n_298, n_299, n_300, n_301;
  wire n_302, n_303, n_306, n_313, n_314, n_315, n_320, n_321;
  wire n_322, n_349, n_350, n_351;
  AOI21_X1 g1069__7654(.A1 (n_48), .A2 (n_12), .B (n_2), .ZN (z[2]));
  AOI22_X1 g1078__2006(.A1 (n_117), .A2 (x[1]), .B1 (n_302), .B2
       (y[1]), .ZN (n_12));
  NAND2_X1 g1083__6789(.A1 (x[2]), .A2 (y[2]), .ZN (n_2));
  AOI22_X1 g1079__1099(.A1 (n_137), .A2 (x[0]), .B1 (n_306), .B2
       (y[0]), .ZN (n_48));
  INV_X8 g18(.I (x[2]), .ZN (n_111));
  INV_X1 g31(.I (y[1]), .ZN (n_117));
  NAND2_X1 g259(.A1 (n_141), .A2 (n_322), .ZN (z[1]));
  NAND4_X2 g66(.A1 (n_139), .A2 (n_140), .A3 (x[1]), .A4 (y[1]), .ZN
       (n_141));
  NAND2_X2 g67(.A1 (n_137), .A2 (n_306), .ZN (n_139));
  INV_X8 g69(.I (y[0]), .ZN (n_137));
  NAND2_X2 g68(.A1 (y[0]), .A2 (x[0]), .ZN (n_140));
  INV_X4 g1134(.I (y[2]), .ZN (n_251));
  OAI22_X1 g287(.A1 (n_296), .A2 (n_298), .B1 (n_300), .B2 (n_303), .ZN
       (z[0]));
  NOR2_X2 g290(.A1 (n_313), .A2 (n_315), .ZN (n_296));
  NAND2_X1 g289(.A1 (n_297), .A2 (y[0]), .ZN (n_298));
  NAND2_X2 g292(.A1 (n_111), .A2 (y[2]), .ZN (n_297));
  NAND2_X1 g288(.A1 (n_299), .A2 (x[0]), .ZN (n_300));
  NAND2_X2 g293(.A1 (n_251), .A2 (x[2]), .ZN (n_299));
  AOI22_X2 g291(.A1 (n_301), .A2 (y[2]), .B1 (n_302), .B2 (y[1]), .ZN
       (n_303));
  INV_X8 g296(.I (x[2]), .ZN (n_301));
  INV_X8 g298(.I (x[1]), .ZN (n_302));
  INV_X8 g299(.I (x[0]), .ZN (n_306));
  NOR2_X2 g11(.A1 (n_301), .A2 (y[2]), .ZN (n_313));
  NOR2_X2 g1143(.A1 (n_314), .A2 (y[1]), .ZN (n_315));
  INV_X8 g1144(.I (x[1]), .ZN (n_314));
  NOR2_X1 g89(.A1 (n_351), .A2 (n_321), .ZN (n_322));
  NOR3_X2 g90(.A1 (n_111), .A2 (n_320), .A3 (y[2]), .ZN (n_321));
  INV_X16 g93(.I (y[1]), .ZN (n_320));
  NOR3_X2 g21(.A1 (n_349), .A2 (n_350), .A3 (x[2]), .ZN (n_351));
  INV_X4 g24(.I (x[1]), .ZN (n_349));
  INV_X16 g22(.I (y[2]), .ZN (n_350));
endmodule
```

Netlist5: (netlist after of mux_comparator after using NanGate_15nm_OCL_fast_conditional_nldm)

(iv) In each case, identify the critical path from input to output, listing the max_delay from input to output. List the number of standard cells in the critical path.

A)CADENCE_RAK MAX_TIMING

```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 24 2021  01:03:22 am
  Module:                 mux_comparator
  Technology library:     gpdk045bc
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
==============================================================

     Pin           Type      Fanout Load Slew Delay Arrival
                               (fF) (ps)  (ps)    (ps)
--------------------------------------------------------------
y[0]              in port         3 26.9  100     +0        0 R
g2991_dup/A                                       +0        0
g2991_dup/Y       INVX16          1  4.5   32    +42       42 F
g2988__3017/B                                     +0       42
g2988__3017/Y     NAND2X6         1  3.2   37    +24       66 R
g2980__4599/A0                                    +0       66
g2980__4599/Y     AOI21X4         1  3.0   68    +63      129 F
g2978__1377/A1                                    +0      129
g2978__1377/Y     OAI21X4         3  2.4   61    +57      186 R
g2976__3015/A1                                    +0      186
g2976__3015/Y     OAI22X1         1  0.6   86    +84      270 F
z[0]              out port                        +0      270 F
--------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'     250ps
Timing slack :      -20ps (TIMING VIOLATION)
Start-point  : y[0]
End-point    : z[0]
```

B) NanGate_15nm_OCL_slow_conditional_nldm MAX_TIMING

```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 24 2021  03:09:35 pm
  Module:                 mux_comparator
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
==============================================================

  Pin           Type      Fanout Load Slew Delay Arrival
                               (fF) (ps)  (ps)   (ps)
---------------------------------------------------------------
y[1]              in port         6 24.2    0     +0        0 R
g93/I                                               +0        0
g93/ZN            INV_X16         1  1.8    0     +0        0 F
g90/A2                                              +0        0
g90/ZN            NOR3_X2         1  1.0    5     +3        4 R
g89/A2                                              +0        4
g89/ZN            NOR2_X1         1  1.0    3     +2        6 F
g259/A2                                             +0        6
g259/ZN           NAND2_X1        1  0.8    3     +2        8 R
z[1]     <<<      out port                          +0        8 R
---------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'         0ps
Timing slack :      -8ps (TIMING VIOLATION)
Start-point  : y[1]
End-point    : z[1]
```

C) NanGate_15nm_OCL_fast_conditional_nldm MAX_TIMING

```
|=============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.25-s068_1
  Generated on:           Sep 24 2021  01:30:48 am
  Module:                 mux_comparator
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   fast (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
==============================================================

     Pin           Type      Fanout Load Slew Delay Arrival
                               (fF) (ps)  (ps)   (ps)
---------------------------------------------------------------
y[2]              in port         6 40.2    0     +0        0 R
g1119/I                                             +0        0
g1119/ZN          INV_X16         1  1.7    0     +0        0 F
g1118/B1                                            +0        0
g1118/ZN          OAI22_X2        1  1.9    6     +3        4 R
g153/A1                                             +0        4
g153/ZN           NAND2_X2        1  1.2    3     +2        6 F
g1068__7837/A1                                      +0        6
g1068__7837/ZN    NAND3_X1        1  0.0    2     +2        8 R
z[0]              out port                          +0        8 R
---------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'         0ps
Timing slack :      -8ps (TIMING VIOLATION)
Start-point  : y[2]
End-point    : z[0]
```

(v) In each case, identify the min_delay path and tabulate the min delay. List the number of standard cells in the min_delay path.

A) CADENCE_RAK MIN_TIMING

```
path 132:

     Pin          Type     Fanout Load Slew Delay Arrival
                                  (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------
x[1]             in port       4 24.8  100    +0       0 R
g2995/A                                       +0       0
g2995/Y          INVX16        1  0.8   29   +39      39 F
g2975__3002/B0                                +0      39
g2975__3002/Y    OAI22X1       1  0.6   92   +48      87 R
z[1]             out port                     +0      87 R
-------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'     250ps
Timing slack :     163ps
Start-point  : x[1]
End-point    : z[1]
```

B) NanGate_15nm_OCL_slow_conditional_nldm MIN_TIMING

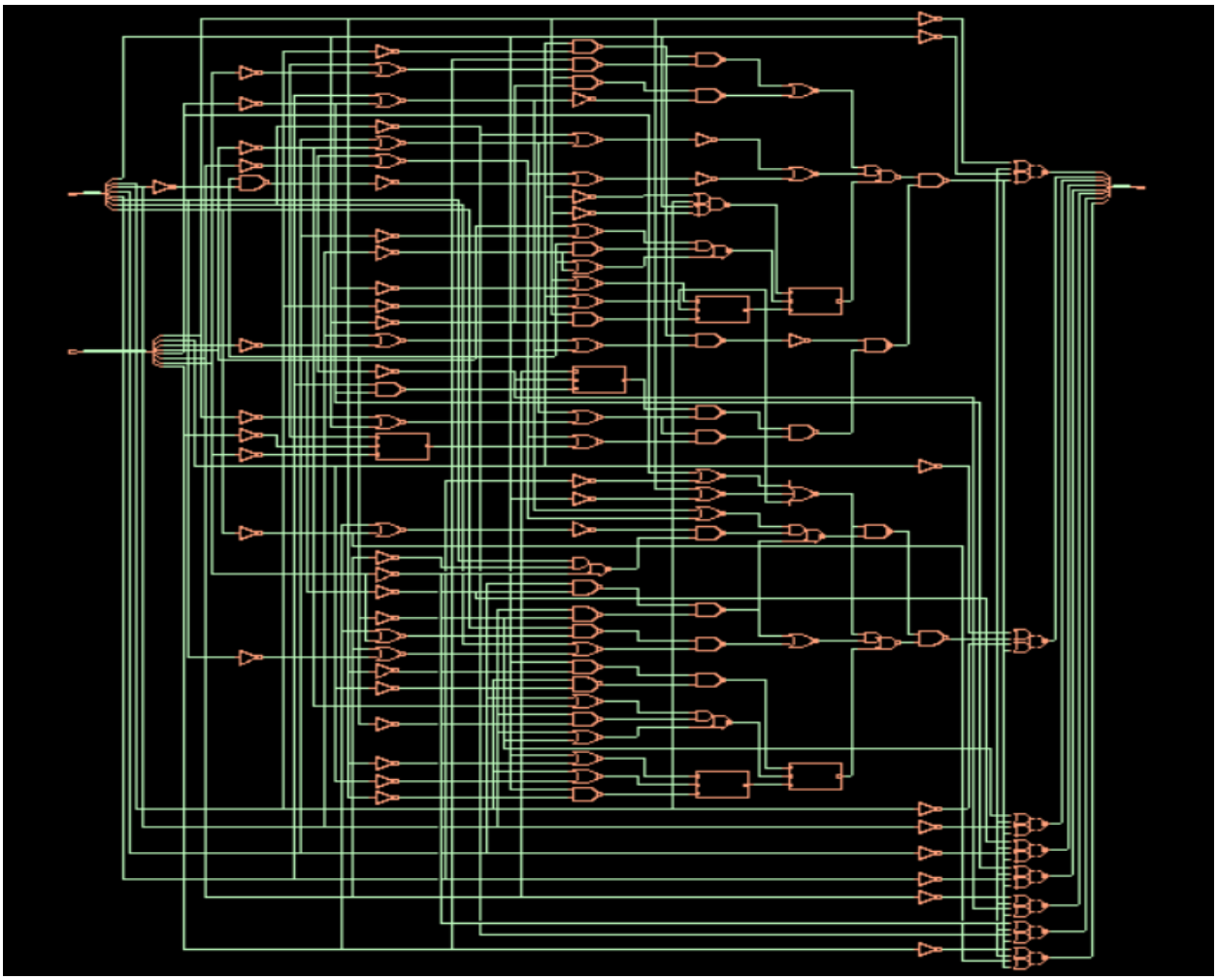
```
path  72:

     Pin          Type     Fanout Load Slew Delay Arrival
                                  (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------
x[2]             in port       5 21.8    0    +0       0 F
g1083__6789/A1                                +0       0
g1083__6789/ZN   NAND2_X1      1  1.0    2    +1       1 R
g1069__7654/B                                 +0       1
g1069__7654/ZN   AOI21_X1      1  0.8    4    +2       4 F
z[2]             out port                     +0       4 F
-------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'       0ps
Timing slack :      -4ps (TIMING VIOLATION)
Start-point  : x[2]
End-point    : z[2]
```

C) NanGate_15nm_OCL_fast_conditional_nldm MAX_TIMING

```
path  72:

     Pin          Type     Fanout Load Slew Delay Arrival
                                  (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------
x[2]             in port       5 18.5    0    +0       0 F
g1081__9719/A1                                +0       0
g1081__9719/ZN   NAND2_X1      1  1.1    2    +2       2 R
g1070__1142/B                                 +0       2
g1070__1142/ZN   AOI21_X1      1  0.8    3    +2       4 F
z[2]             out port                     +0       4 F
-------------------------------------------------------------
Exception    : 'path_delays/zipped_path_delay_0'       0ps
Timing slack :      -4ps (TIMING VIOLATION)
Start-point  : x[2]
End-point    : z[2]
```

(vi) Change the three-bit numbers x and y to eight-bit numbers. Resynthesize, and report the number of standard cells in the critical (max_delay) path for just the Cadence RAK PDK.

```
module mux_comparator(x,y,z);
input [7:0] x;
input [7:0] y;
output reg[7:0] z;
always @(*)
begin
 if(x>y)  z=y;
 else if(x<y) z=x;
 else z=0;
end
 endmodule
```



Fig(1.23) : Schematic of eightbit number mux_comparator

THANKYOU

Submitted By: Prafful Choudhary

MT2021523