

-----ASSIGNMENT 3: INNOVUS RAK-----

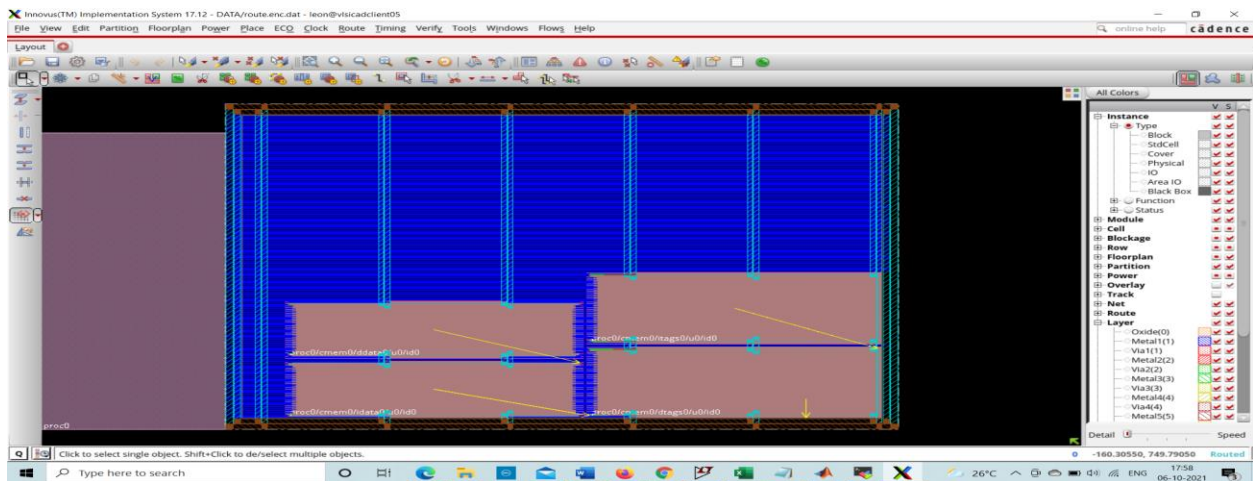
Submitted By: Group Members

Praful Choudhary MT2021523

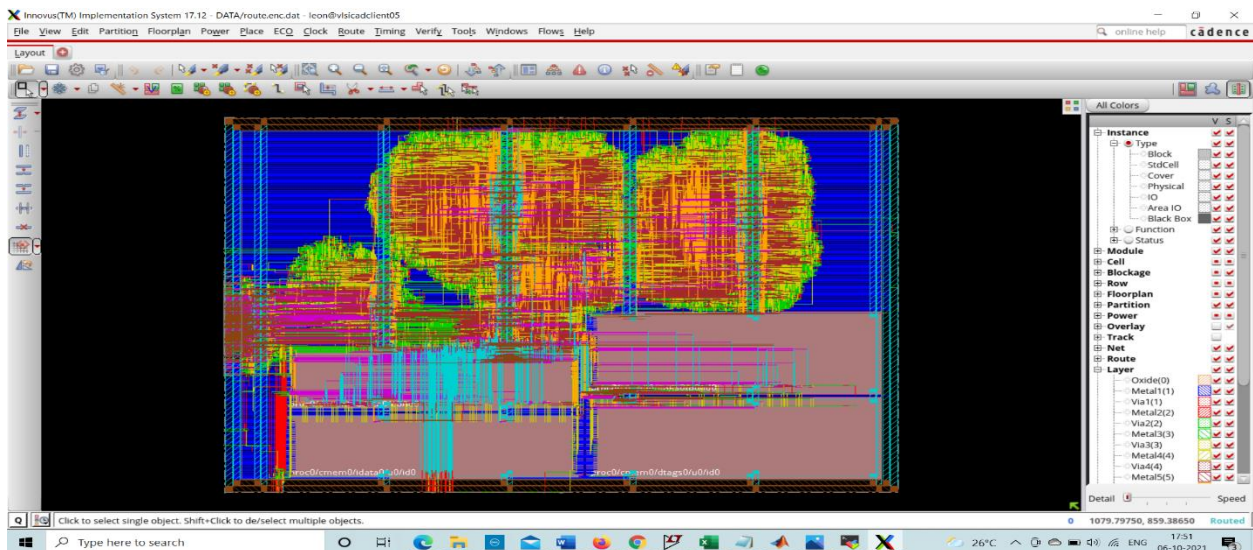
Komatreddy Vikram Kumar MT2021516

Step 1) Extract the RAK database and change directory to the work directory:

The floorplan has the blocks placed and power routing complete. From here we can do the implementation flow



Fig(1.1): Floorplan



Fig(1.2):Physical view after placement and preCTS optimization

When both the placement and preCTS optimizations done, we can start looking at the placed design in the Physical views. We can Observe the placed standard cells are shown in the Physical view

- ```
192.168.200.14 (cad)
```

```
terminal Sessions View X Server Tools Games Settings Macros Help
```

```
Session Servers Tools Games Sessions View Split MultExec Tunneling Packages Settings Help
```

```
Quick connect...
```

```
NZ 192.168.200.14 (cad)
```

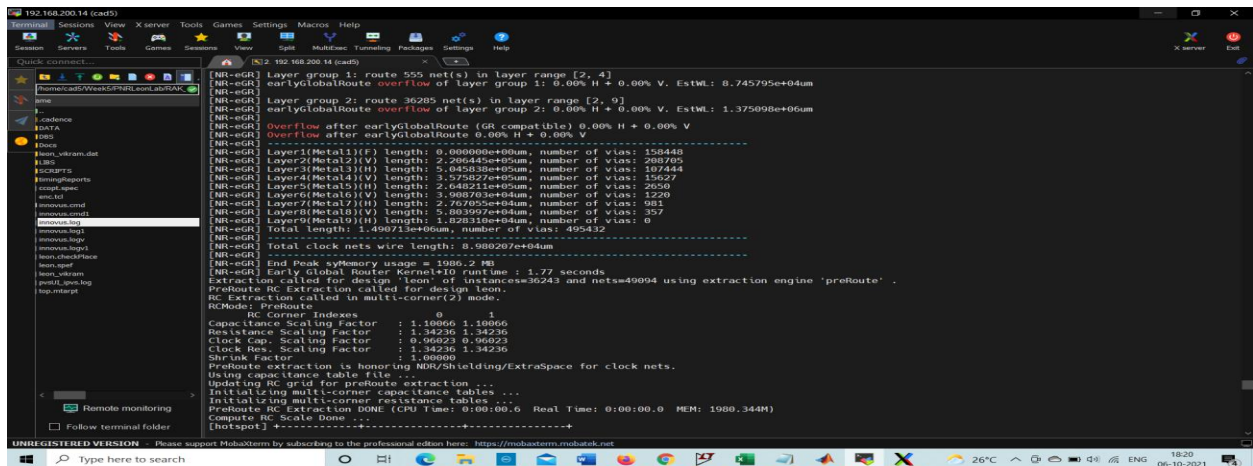
```
[NR-eGR] earlyGlobalRoute overflow of layer group 1: 0.00% H + 0.00% V. EstWL: 8.747595e+04m
[NR-eGR]
[NR-eGR] Layer group 2: route 36274 net(s) in layer range [2, 9]
[NR-eGR] earlyGlobalRoute overflow of layer group 2: 0.00% H + 0.00% V. EstWL: 1.374905e+06m
[NR-eGR]
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.00% H + 0.00% V
[NR-eGR] Overflow after earlyGlobalRoute 0.00% H + 0.00% V
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00, normalized total congestion hotspot area = 0.00 (area is in unit of 4 std-cell row bins)

[NR-eGR] Skipped repairing congestion.

[NR-eGR]
[NR-eGR] Layer1(Metal1)(F) length: 0.060800e+06um, number of vias: 159425
[NR-eGR] Layer2(Metal2)(V) length: 2.282414e+05um, number of vias: 208632
[NR-eGR] Layer3(Metal3)(H) length: 5.038613e+05um, number of vias: 107666
[NR-eGR] Layer4(Metal4)(S) length: 3.744526e+05um, number of vias: 53760
[NR-eGR] Layer5(Metals)(H) length: 2.635947e+05um, number of vias: 2664
[NR-eGR] Layer6(Metal6)(V) length: 3.894233e+04um, number of vias: 1223
[NR-eGR] Layer7(Metal7)(H) length: 2.897080e+04um, number of vias: 1000
[NR-eGR] Layer8(Metal8)(V) length: 5.831252e+04um, number of vias: 359
[NR-eGR] Layer9(Metal9)(H) length: 1.916808e+04um, number of vias: 0
[NR-eGR] Total length: 1.490955e+06um, number of vias: 495609
[NR-eGR] -----
[NR-eGR] Total clock nets wire length: 0.981078e+06um
[NR-eGR]
End of congrepair (cpu=00:01.8, real=00:02.0)
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1968.7M)
Extraction called for design 'leon' of instances36232 and nets=49882 using extraction engine 'preRoute'.
PreRoute RC Extraction called for design leon.
RC Extraction called in multi-corner(2) mode.
RCMode: PreRoute
RC Corner Indexes 0 1
Capacitance Scaling Factor 1.18066 1.18066
Resistance Scaling Factor 1.34236 1.34236
Clock Cap. Scaling Factor 0.96023 0.96023
Clock Res. Scaling Factor 1.34236 1.34236
Shrink Factor 1.08900
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
```

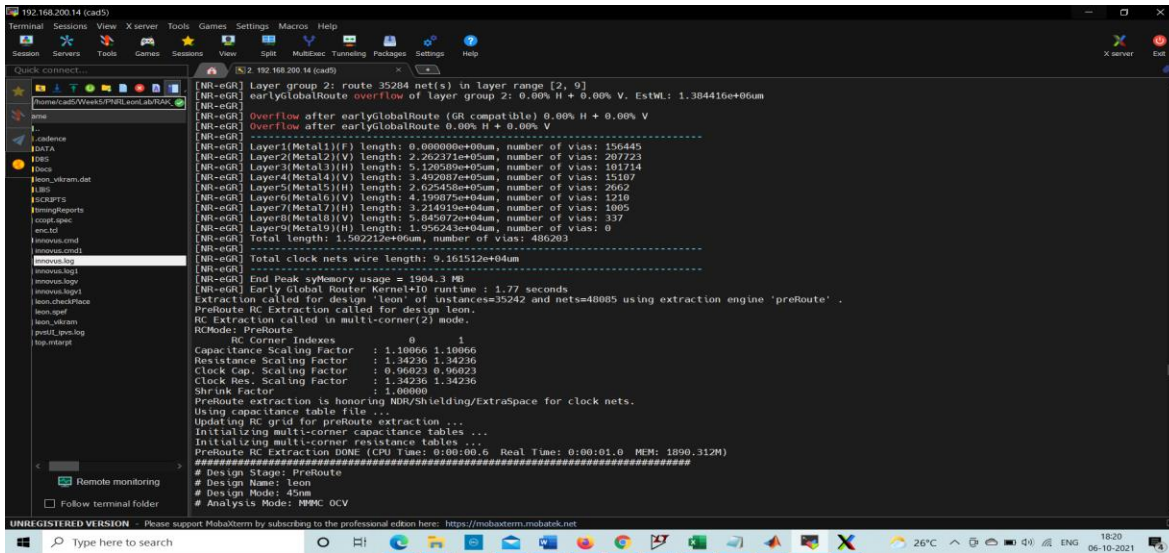
Metal Layer = 9  
Number of vias = 495609

| Layer1 | Layer2 | Layer3 | Layer4 | Layer5 | Layer6 | Layer7 | Layer8 | Layer9 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 158425 | 208632 | 107606 | 15700  | 2664   | 1223   | 1000   | 359    | 0      |



Metal Layer = 9  
Number of vias = 495432

| Layer1 | Layer2 | Layer3 | Layer4 | Layer5 | Layer6 | Layer7 | Layer8 | Layer9 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 158448 | 208705 | 107444 | 15627  | 2650   | 1220   | 981    | 357    | 0      |

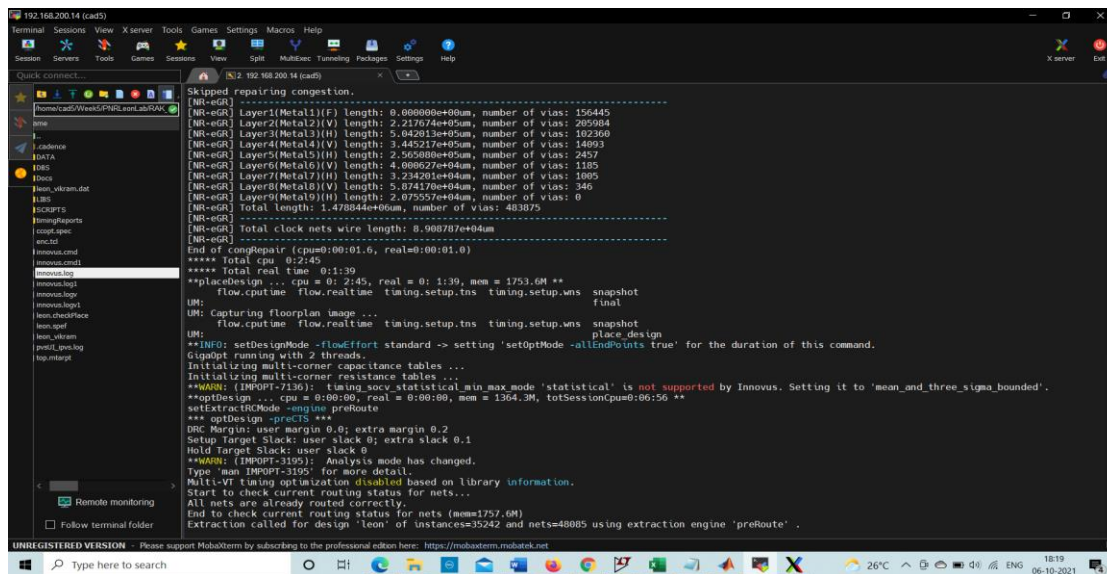


Fig(1.3.3): Number of Metal Layer and Vias

Metal Layer = 9

Number of vias = 486203

| Layer1 | Layer2 | Layer3 | Layer4 | Layer5 | Layer6 | Layer7 | Layer8 | Layer9 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 156445 | 207723 | 101714 | 15107  | 2662   | 1210   | 1005   | 337    | 0      |



Fig(1.3.4): Number of Metal Layer and Vias

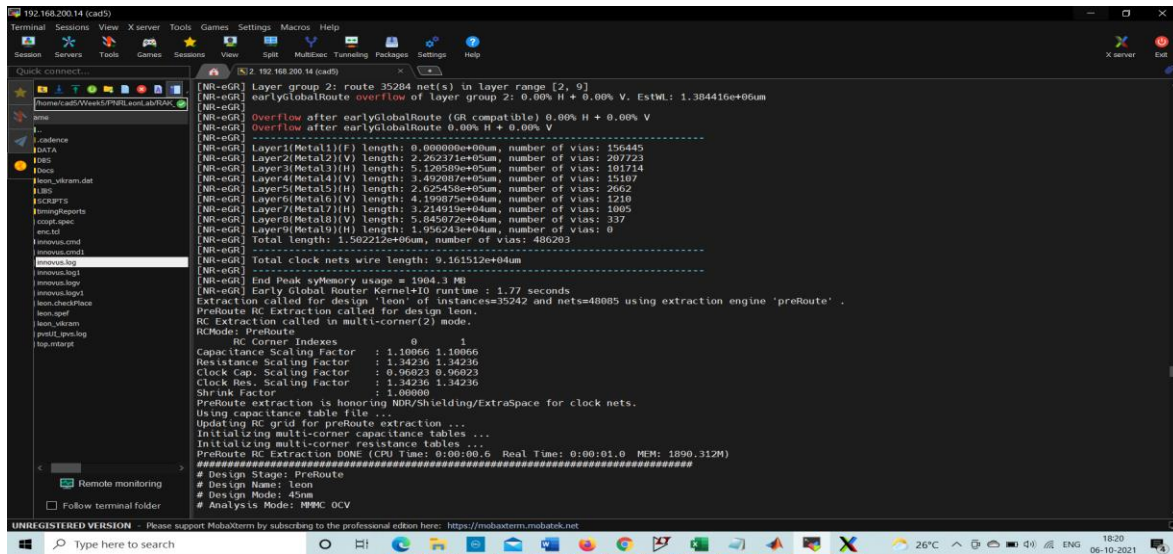
Metal Layer = 9

Number of vias = 483875

| Layer1 | Layer2 | Layer3 | Layer4 | Layer5 | Layer6 | Layer7 | Layer8 | Layer9 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 156445 | 205984 | 102360 | 14093  | 2457   | 1185   | 1005   | 346    | 0      |

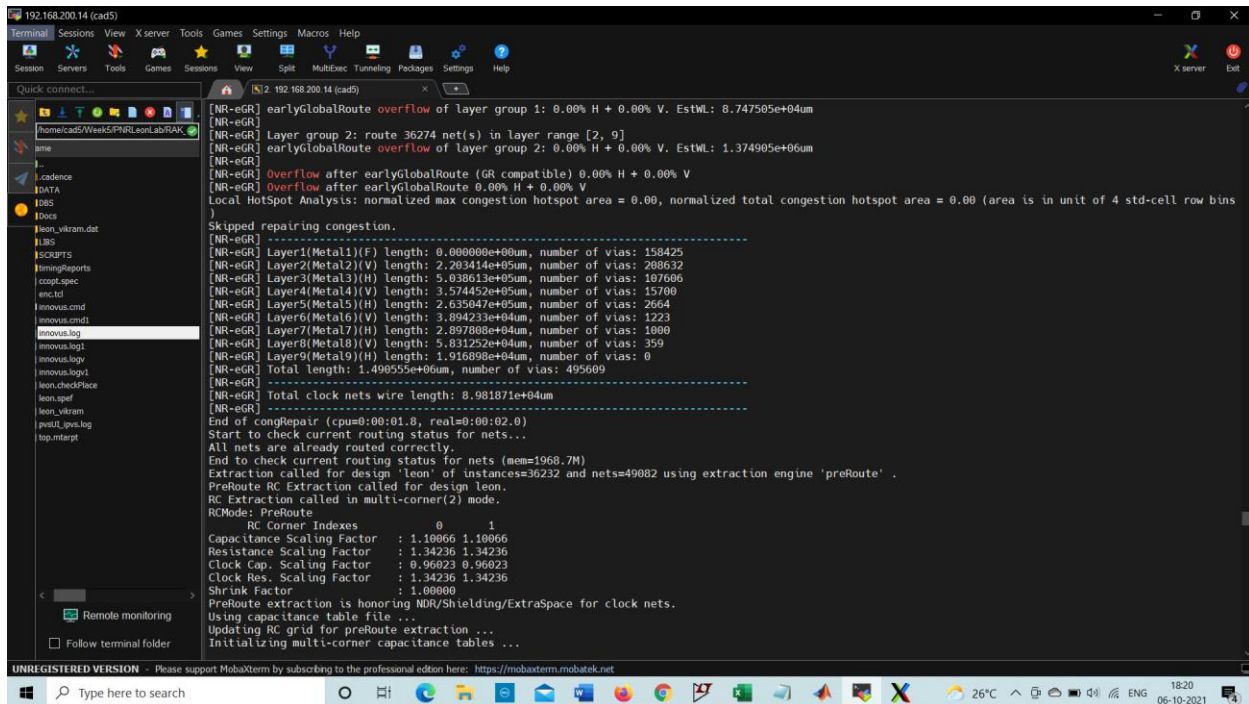


- b. During preRoute, how many instances and nets exist in the Leon design during the “preRoute” stage



```
[NR-eGR] Layer group 2: route 35204 net(s) in layer range [2, 9]
[NR-eGR] earlyGlobalRoute overflow of layer group 2: 0.00% H + 0.00% V. EstWL: 1.384416e+06um
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.00% H + 0.00% V
[NR-eGR] Overflow after earlyGlobalRoute 0.00% H + 0.00% V
[NR-eGR] -----
[NR-eGR] Layer1(Metal1)(F) length: 0.000000e+00um, number of vias: 156445
[NR-eGR] Layer2(Metal2)(V) length: 2.262371e+05um, number of vias: 207723
[NR-eGR] Layer3(Metal3)(H) length: 5.120509e+05um, number of vias: 101714
[NR-eGR] Layer4(Metal4)(V) length: 3.492007e+05um, number of vias: 15107
[NR-eGR] Layer5(Metal5)(H) length: 2.625458e+05um, number of vias: 2662
[NR-eGR] Layer6(Metal6)(V) length: 4.199075e+04um, number of vias: 1216
[NR-eGR] Layer7(Metal7)(H) length: 3.214935e+04um, number of vias: 1905
[NR-eGR] Layer8(Metal8)(V) length: 5.845072e+04um, number of vias: 337
[NR-eGR] Layer9(Metal9)(H) length: 1.956245e+04um, number of vias: 0
[NR-eGR] Total length: 5.562212e+06um, number of vias: 486293
[NR-eGR] -----
[NR-eGR] Total clock nets wire length: 9.161512e+04um
[NR-eGR] -----
[NR-eGR] End Peak sYstem memory usage = 1004.3 MB
[NR-eGR] Early Global Router Kernel+10 runtime : 1.77 seconds
Extraction called for design 'leon' of instances=35242 and nets=48005 using extraction engine 'preRoute'.
PreRoute RC Extraction called for design leon.
RC Extraction called in multi-corner(2) mode.
RCMode: PreRoute
RC Corner Indexes 0 1
Capacitance Scaling Factor : 1.10066 1.10066
Resistance Scaling Factor : 1.34236 1.34236
Clock Cap. Scaling Factor : 0.96023 0.96023
Clock Res. Scaling Factor : 1.34236 1.34236
Shrink Factor : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0 Real Time: 0:00:01.0 MEM: 1890.312M)
=====
Design Stage: PreRoute
Design Name: leon
Design Mode: 45nm
Analysis Mode: PPRMC_OCV
```

Fig(1.4): Instances = 35242 and Nets= 48005 (Leon Design) during PreRoute



```
[NR-eGR] earlyGlobalRoute overflow of layer group 1: 0.00% H + 0.00% V. EstWL: 8.747585e+04um
[NR-eGR] Layer group 2: route 36274 net(s) in layer range [2, 9]
[NR-eGR] earlyGlobalRoute overflow of layer group 2: 0.00% H + 0.00% V. EstWL: 1.374905e+06um
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.00% H + 0.00% V
[NR-eGR] Overflow after earlyGlobalRoute 0.00% H + 0.00% V
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00, normalized total congestion hotspot area = 0.00 (area is in unit of 4 std-cell row bins)
Skipped repairing congestion.
[NR-eGR] -----
[NR-eGR] Layer1(Metal1)(F) length: 0.000000e+00um, number of vias: 158425
[NR-eGR] Layer2(Metal2)(V) length: 2.293414e+05um, number of vias: 208632
[NR-eGR] Layer3(Metal3)(H) length: 5.038613e+05um, number of vias: 107606
[NR-eGR] Layer4(Metal4)(V) length: 3.574452e+05um, number of vias: 15700
[NR-eGR] Layer5(Metal5)(H) length: 2.635047e+05um, number of vias: 2664
[NR-eGR] Layer6(Metal6)(V) length: 3.894233e+04um, number of vias: 1223
[NR-eGR] Layer7(Metal7)(H) length: 2.897808e+04um, number of vias: 1080
[NR-eGR] Layer8(Metal8)(V) length: 5.831252e+04um, number of vias: 359
[NR-eGR] Layer9(Metal9)(H) length: 1.916898e+04um, number of vias: 0
[NR-eGR] Total length: 1.490555e+06um, number of vias: 495609
[NR-eGR] -----
[NR-eGR] Total clock nets wire length: 8.981071e+04um
[NR-eGR] -----
End of congRepair (cpu=0:00:01.8, real=0:00:02.0)
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1968.7M)
Extraction called for design 'leon' of instances=36232 and nets=49082 using extraction engine 'preRoute'.
PreRoute RC Extraction called for design leon.
RC Extraction called in multi-corner(2) mode.
RCMode: PreRoute
RC Corner Indexes 0 1
Capacitance Scaling Factor : 1.10066 1.10066
Resistance Scaling Factor : 1.34236 1.34236
Clock Cap. Scaling Factor : 0.96023 0.96023
Clock Res. Scaling Factor : 1.34236 1.34236
Shrink Factor : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
```

Fig(1.5): Instances=36232and Nets=49082 (Leon Design) during PreRoute

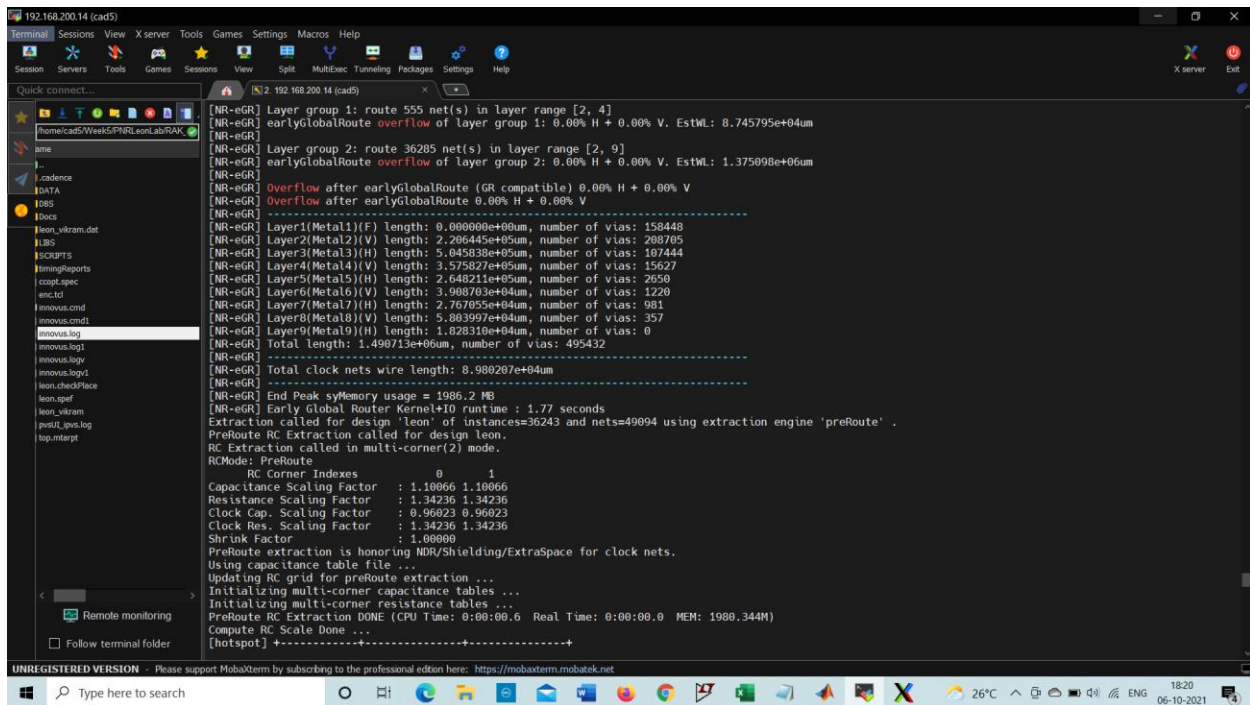
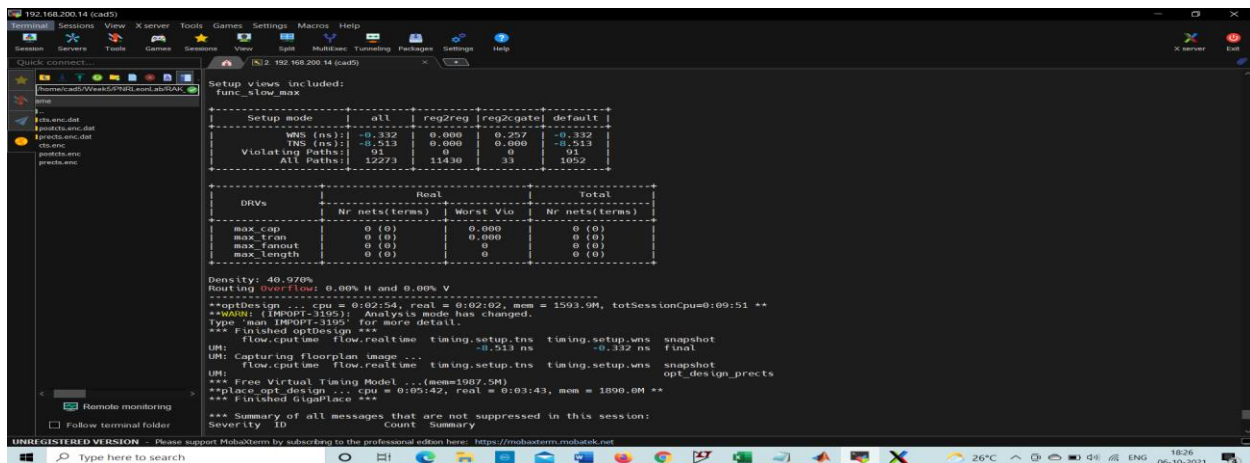


Fig (1.6): Instances=36243 and Nets=49094 (Leon Design) during PreRoute

- After you run Check Placement, what is the Placement density? How many cells have been placed? (Take a screenshot)

Here we are showing the Timing summary , so that we can easily see timing results after optimization as well as standard cell utilization (density) and it give us the EarlyGlobalRoute overflow values.



Fig(2.1) :Placement Density=40.970%

The total number of cell which are placed after optimization

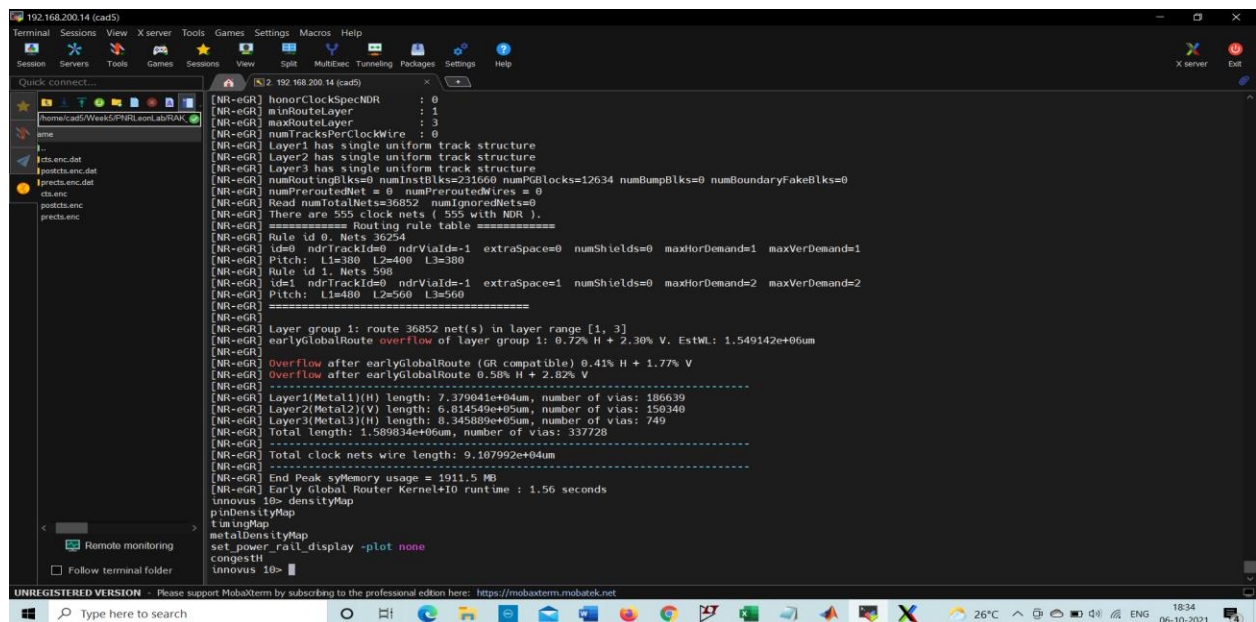
Number of Cells placed = 36339

## Step: Running Early Global Route

Early Global Route defined as the group of global routing & track assignment which correlates well to detail route while running in a very small amount of the time. here we are demonstrating the route congestion by limiting the number of metal routing layers from 1 to 3

3. a. After you run Early Global Route with just 3 Metal Layers, what is the number of vias on each layer.

| Layer1 | Layer2 | Layer3 |
|--------|--------|--------|
| 186639 | 150340 | 749    |



```
[NR-eGR] honorClockSpecNDR : 0
[NR-eGR] minRouteLayer : 1
[NR-eGR] maxRouteLayer : 3
[NR-eGR] numTracksPerClockWire : 0
[NR-eGR] Layer1 has single uniform track structure
[NR-eGR] Layer2 has single uniform track structure
[NR-eGR] Layer3 has single uniform track structure
[NR-eGR] numRoutingBlks=0 numInstBlks=231660 numPGBlks=12634 numBumpBlks=0 numBoundaryFakeBlks=0
[NR-eGR] numPreoutedNet=0 numPreoutedNet=0
[NR-eGR] Read numTotalNets=36852 numIgnoredNets=0
[NR-eGR] There are 555 clock nets (555 with NDR).
[NR-eGR] ===== Routing rule table =====
[NR-eGR] Rule id 0, Nets 36254
[NR-eGR] id=0 ndrTrackId=0 ndrViaId=1 extraSpace=0 numShields=0 maxHorDemand=1 maxVerDemand=1
[NR-eGR] Pitch: L1=380 L2=400 L3=380
[NR-eGR] Rule id 1, Nets 590
[NR-eGR] id=1 ndrTrackId=0 ndrViaId=1 extraSpace=1 numShields=0 maxHorDemand=2 maxVerDemand=2
[NR-eGR] Pitch: L1=480 L2=560 L3=560
[NR-eGR] =====
[NR-eGR] Layer group 1: route 36852 net(s) in layer range [1, 3]
[NR-eGR] earlyGlobalRoute overflow of layer group 1: 0.72% H + 2.30% V. EstWL: 1.549142e+06um
[NR-eGR]
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.41% H + 1.77% V
[NR-eGR] Overflow after earlyGlobalRoute 0.58% H + 2.82% V
[NR-eGR] =====
[NR-eGR] Layer1(Metal1)(H) length: 7.379841e+04um, number of vias: 186639
[NR-eGR] Layer2(Metal2)(V) length: 6.814549e+05um, number of vias: 150340
[NR-eGR] Layer3(Metal3)(H) length: 8.345809e+05um, number of vias: 749
[NR-eGR] Total length: 1.389534e+06um, number of vias: 337728
[NR-eGR] =====
[NR-eGR] Total clock nets wire length: 9.107992e+04um
[NR-eGR] =====
[NR-eGR] End Peak syMemory usage = 1911.5 MB
[NR-eGR] Early Global Router Kernel+IO runtime : 1.56 seconds
innovus 10> densityMap
pInDensityMap
tuningMap
metalDensityMap
set_power_rail_display -plot none
congestH
innovus 10>
```

Fig(3.1):Number of Vias on each metal layer after EGR with 3Metal Layer

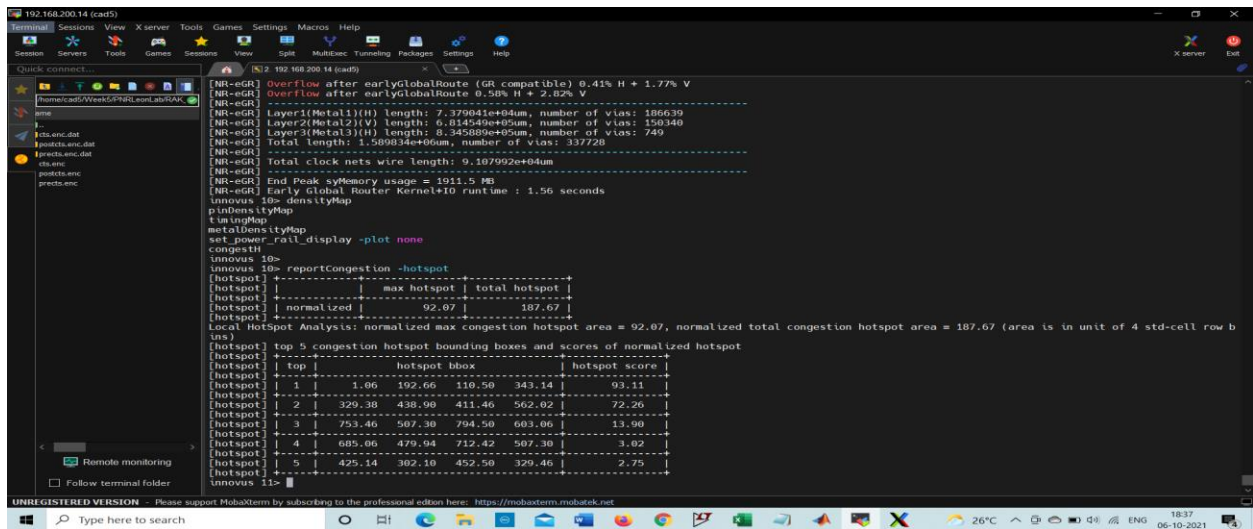
- b. which is of these layers is Vertical?

Layer2(Metal2)=Vertical

- c. What is the Congestion Report after EarlyGlobal Route with just 3 layers

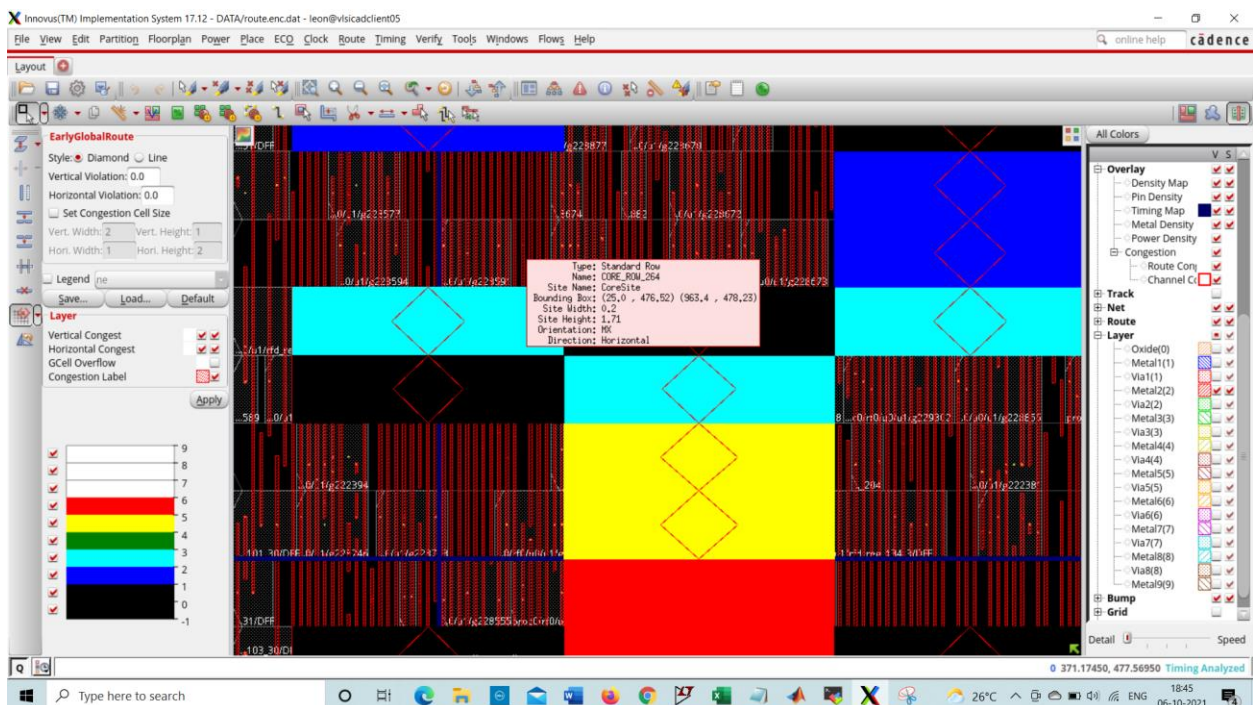
Here we can see the total number of Hotspots are 5 when we are using the 3layers.





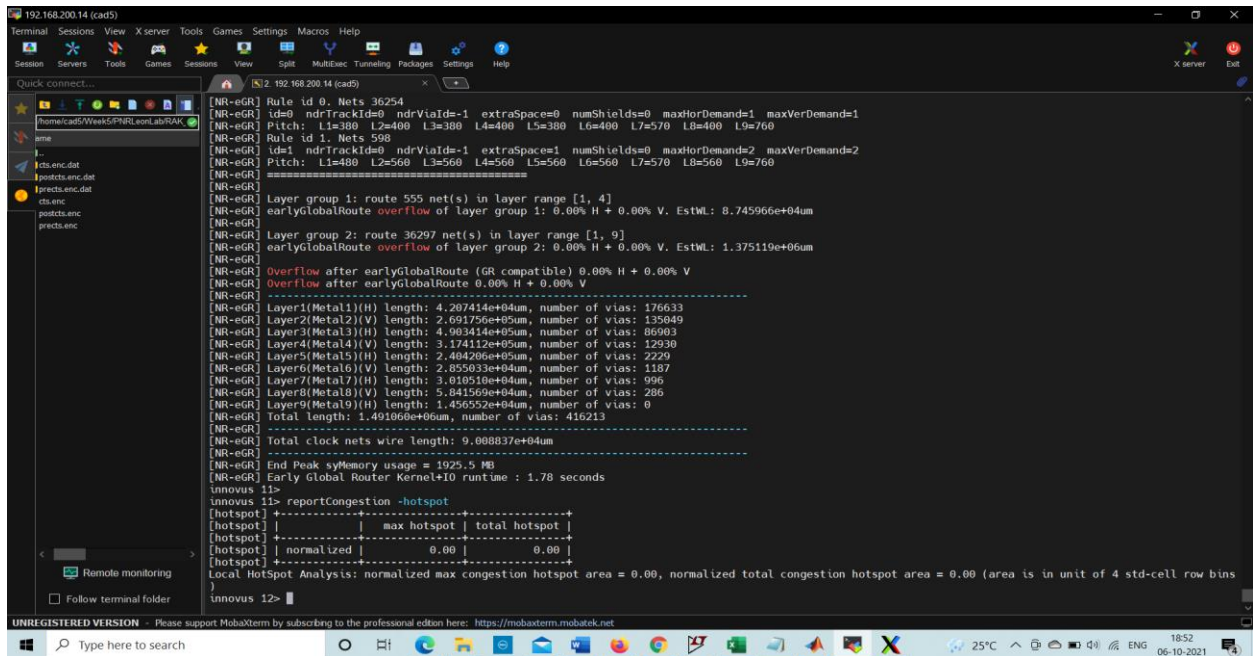
Fig(3.2):Congestion Report (for 3 Layers)

d. With Overlay and Net highlighted, only on Metal 2, Zoom into Core\_Row\_264. Now Zoom out and take a snapshot of the entire Innovus window which shows congestion marks.



Fig(3.3): 2-D view of Early Global Congestion of Core\_Row\_264

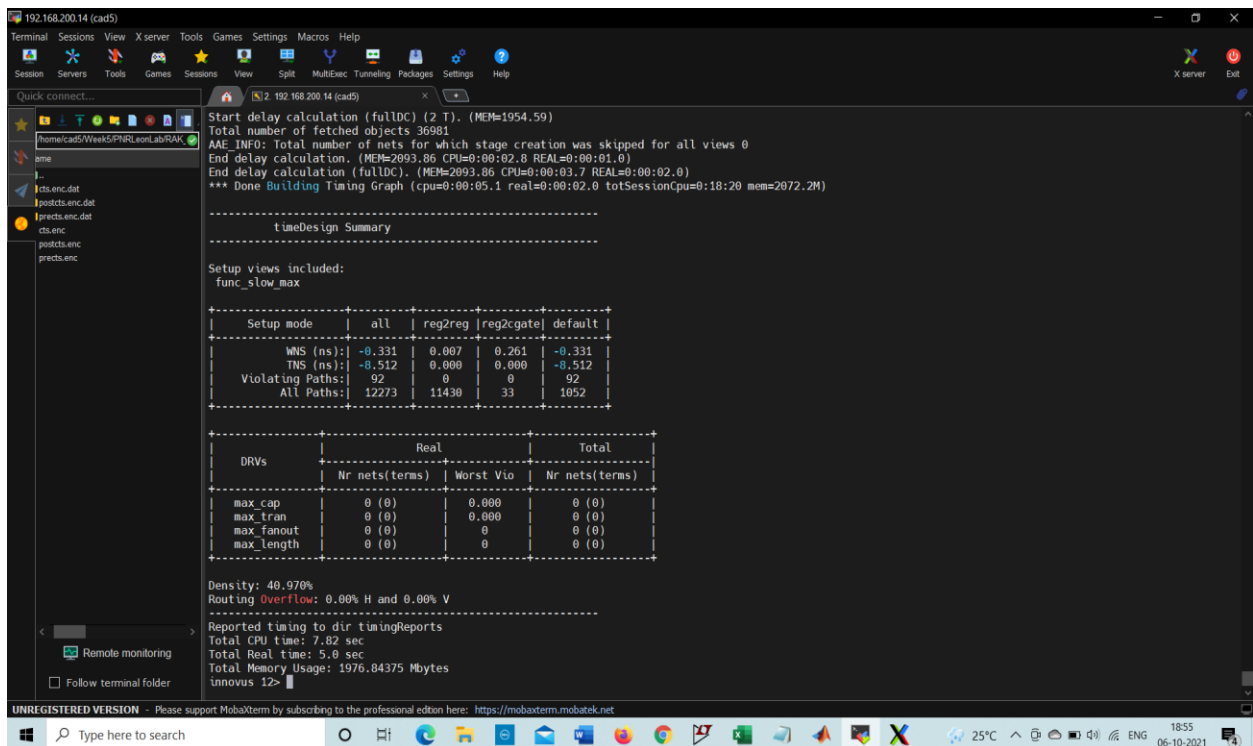
4. Now, after you change the number of Layers to 9, report Congestion again. Provide a snapshot of how many hotspots exist now?



```
[NR-eGR] Rule id 0. Nets 36254
[NR-eGR] id=0 ndrTrackId=0 ndrViaId=1 extraSpaces=0 numShields=0 maxHorDemand=1 maxVerDemand=1
[NR-eGR] Pitch: L1=380 L2=400 L3=380 L4=400 L5=380 L6=400 L7=570 L8=400 L9=760
[NR-eGR] Rule id 1. Nets 598
[NR-eGR] id=1 ndrTrackId=0 ndrViaId=1 extraSpaces=1 numShields=0 maxHorDemand=2 maxVerDemand=2
[NR-eGR] Pitch: L1=480 L2=560 L3=560 L4=560 L5=560 L6=560 L7=570 L8=560 L9=760
[NR-eGR]
[NR-eGR] Layer group 1: route 555 net(s) in layer range [1, 4]
[NR-eGR] earlyGlobalRoute overflow of layer group 1: 0.00% H + 0.00% V. EstWL: 8.745966e+04um
[NR-eGR]
[NR-eGR] Layer group 2: route 36297 net(s) in layer range [1, 9]
[NR-eGR] earlyGlobalRoute overflow of layer group 2: 0.00% H + 0.00% V. EstWL: 1.375119e+06um
[NR-eGR]
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.00% H + 0.00% V
[NR-eGR] Overflow after earlyGlobalRoute 0.00% H + 0.00% V
[NR-eGR]
[NR-eGR] -----
[NR-eGR] Layer1(Metal1)(H) length: 4.207414e+04um, number of vias: 176633
[NR-eGR] Layer2(Metal2)(V) length: 2.691756e+05um, number of vias: 135049
[NR-eGR] Layer3(Metal3)(H) length: 4.903414e+05um, number of vias: 86003
[NR-eGR] Layer4(Metal4)(V) length: 3.174112e+05um, number of vias: 12930
[NR-eGR] Layer5(Metal5)(H) length: 2.404206e+05um, number of vias: 2229
[NR-eGR] Layer6(Metal6)(V) length: 2.855033e+04um, number of vias: 1187
[NR-eGR] Layer7(Metal7)(H) length: 3.010510e+04um, number of vias: 996
[NR-eGR] Layer8(Metal8)(V) length: 5.841569e+04um, number of vias: 286
[NR-eGR] Layer9(Metal9)(H) length: 1.456552e+04um, number of vias: 0
[NR-eGR] Total length: 1.491060e+06um, number of vias: 416213
[NR-eGR]
[NR-eGR] -----
[NR-eGR] Total clock nets wire length: 9.008837e+04um
[NR-eGR]
[NR-eGR] End Peak sXMemory usage = 1925.5 MB
[NR-eGR] Early Global Router Kernel+IO runtime : 1.78 seconds
innovus 11>
innovus 11> reportCongestion -hotspot
[hotspot] +-----+
[hotspot] | max hotspot | total hotspot |
[hotspot] +-----+
[hotspot] | normalized | 0.00 | 0.00 |
[hotspot] +-----+
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00, normalized total congestion hotspot area = 0.00 (area is in unit of 4 std-cell row bins)
innovus 12>
```

Fig(4.1):Number of Hotspots after giving range to 9 layers

5. After Pre-CTS timing, how many reg2reg paths have violated Setup timing?



```
Start delay calculation (fullDC) (2 T). (MEM=1954.59)
Total number of fetched objects 36981
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2093.86 CPU=0:00:02.8 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=2093.86 CPU=0:00:03.7 REAL=0:00:02.0)
*** Aae Building Timing Graph (cpu=0:00:05.1 real=0:00:02.0 totSessionCpu=0:18:20 mem=2072.2M)

timeDesign Summary

Setup views included:
func_slow_max

+-----+
| Setup mode | all | reg2reg | reg2cgate | default |
+-----+
WNS (ns):	-0.331	0.007	0.261	-0.331
TNS (ns):	-0.512	0.000	0.000	-0.512
Violating Paths:	92	0	0	92
All Paths:	12273	11430	33	1052
+-----+

+-----+
| | Real | Total |
| | Nr nets(terms) | Worst Vto | Nr nets(terms) |
+-----+
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)
+-----+

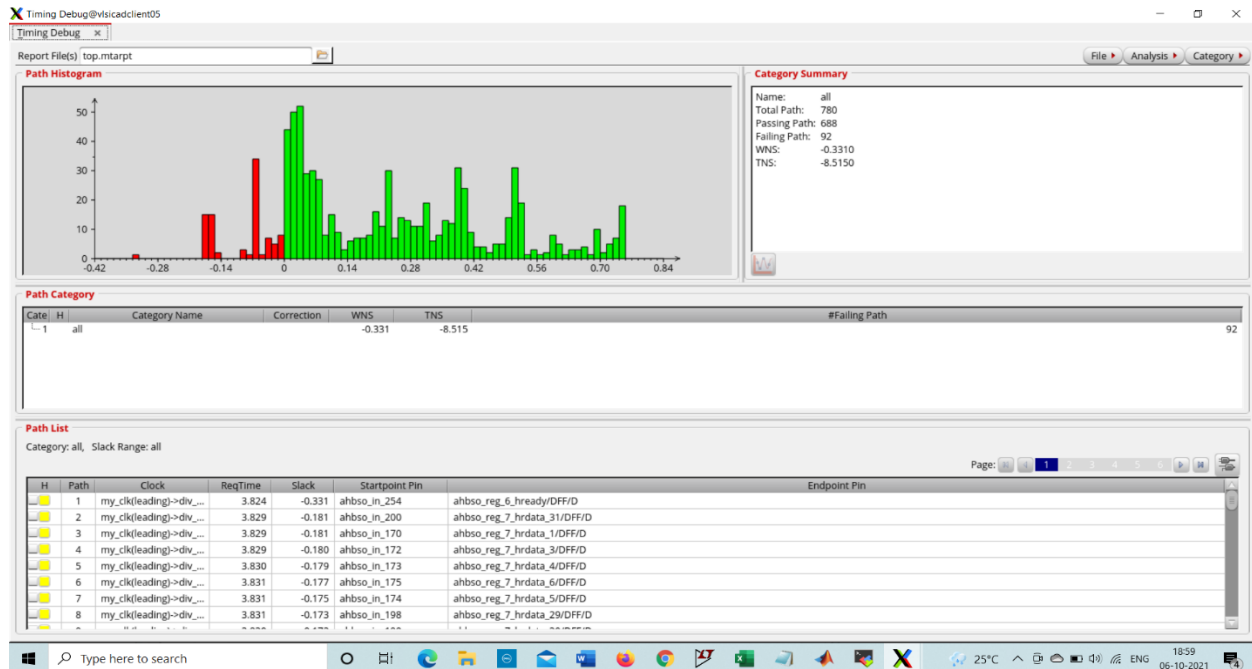
Density: 40.970%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 7.82 sec
Total Real time: 5.0 sec
Total Memory Usage: 1976.84375 Mbytes
innovus 12>
```

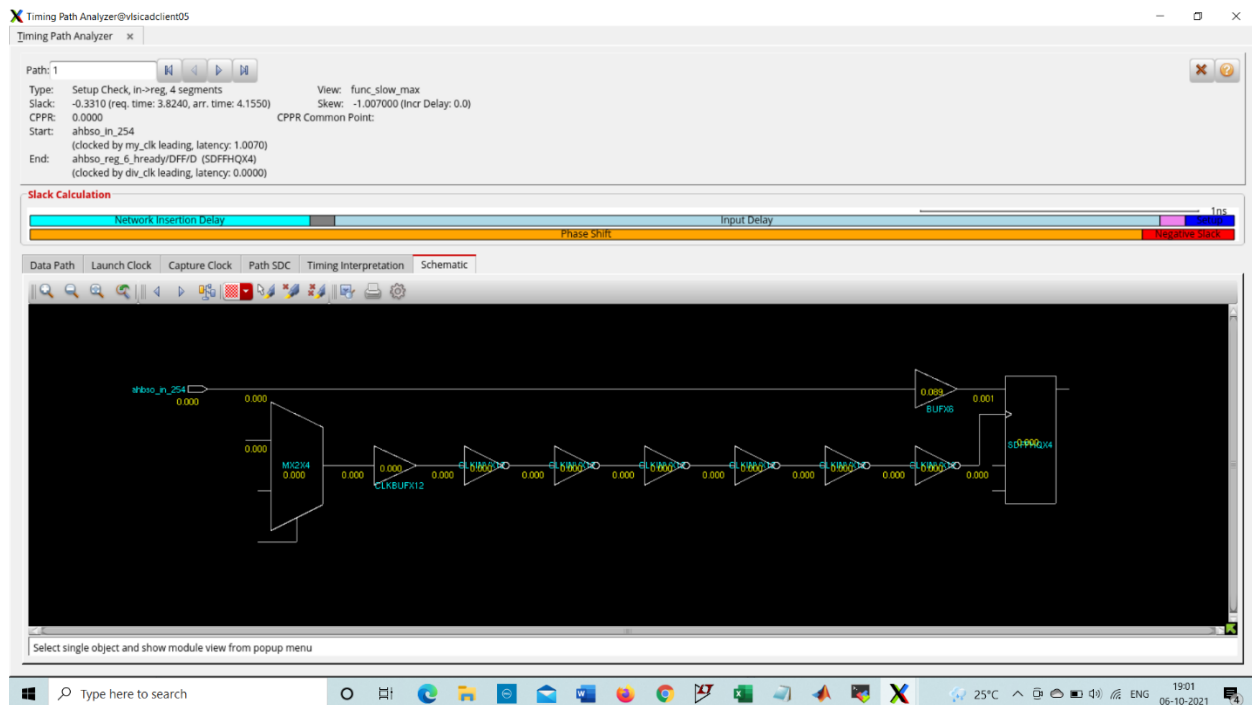
Fig(5.1):reg2reg paths have violated setup timing=92



- Open global timing debug after the pre-cts timing and take a snapshot of the Schematic of the 1st path that violated timing



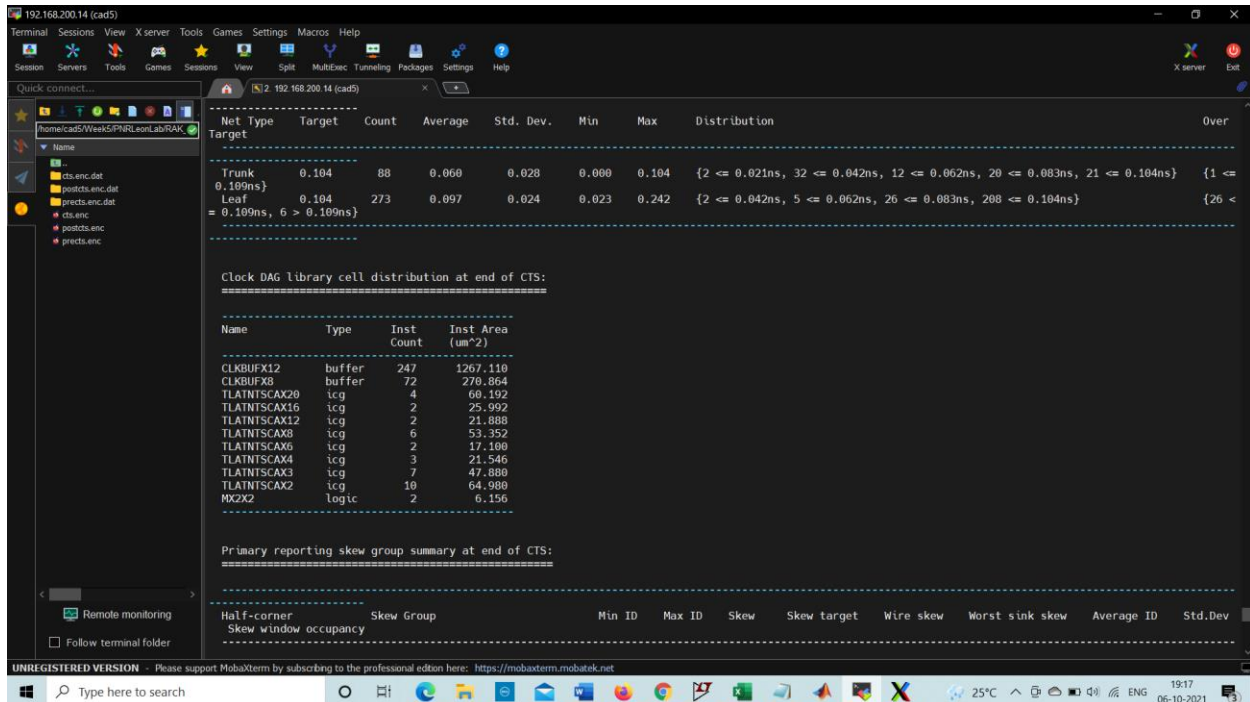
Fig(6.1):Global Timing Debug Interface



Fig(6.2): Schematic of the 1st path that violated timing

- After running CTS, list the names and the number of the CLK Buffer cells and Clock Gating cells (ICG) used in the design

Total= (319) CLKBUFFER+ (36) ICG were used in the design of different drive strengths



Fig(7.1): Number of the CLK Buffer cells and Clock Gating cells (ICG) used in the design

- After running CTS, what is the total wire capacitance and gate capacitance reported by CCOPT

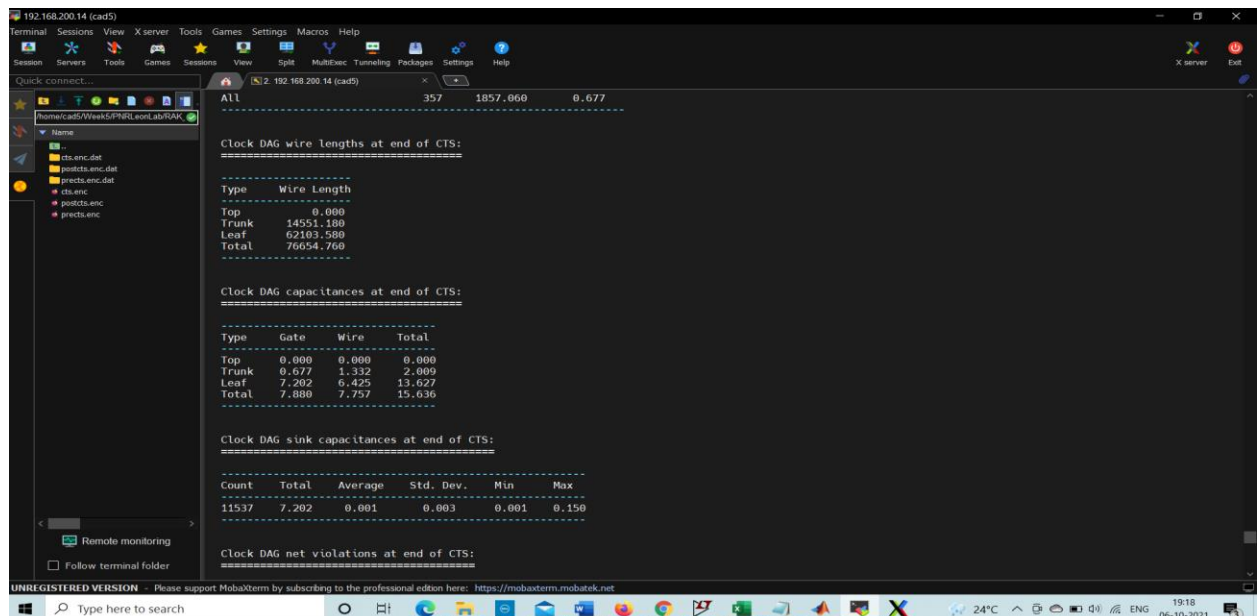


Fig (8.1): The total wire capacitance and gate capacitance reported by CCOPT

9. What are the different steps (or functions) the tool went through during CTS

Start the CCOpt Design: Here the Process is Clock concurrent optimization merges physical optimization into clock tree synthesis and simultaneously optimizes clock delay and logic delay using a single unified cost metric

Routing table rules are specified, layers and vias details read

Updating RC grid for preRoute extraction.

Initializing multi-corner capacitance tables.

Initializing multi-corner resistance tables.

Pre-route RC extraction done

Slew time targets are specified

Delays of BUFFERS, INV and ICG's are specified along with other specifications

Delay constraint for Via's is reported

In resynthesis clock gate merging summary is created and reason of merging is also mentioned  
New netlist is created and merged clocks are removed.

Then clock tree optimization is carry out using different type of methods clustering is one of them and after each step the innovus sees if the pre-requisites are met if not it tries other method of optimisation.

Verification done and after the final optimization the result for worst and total delay paths are reported.

Total Wire and gate capacitances are reported

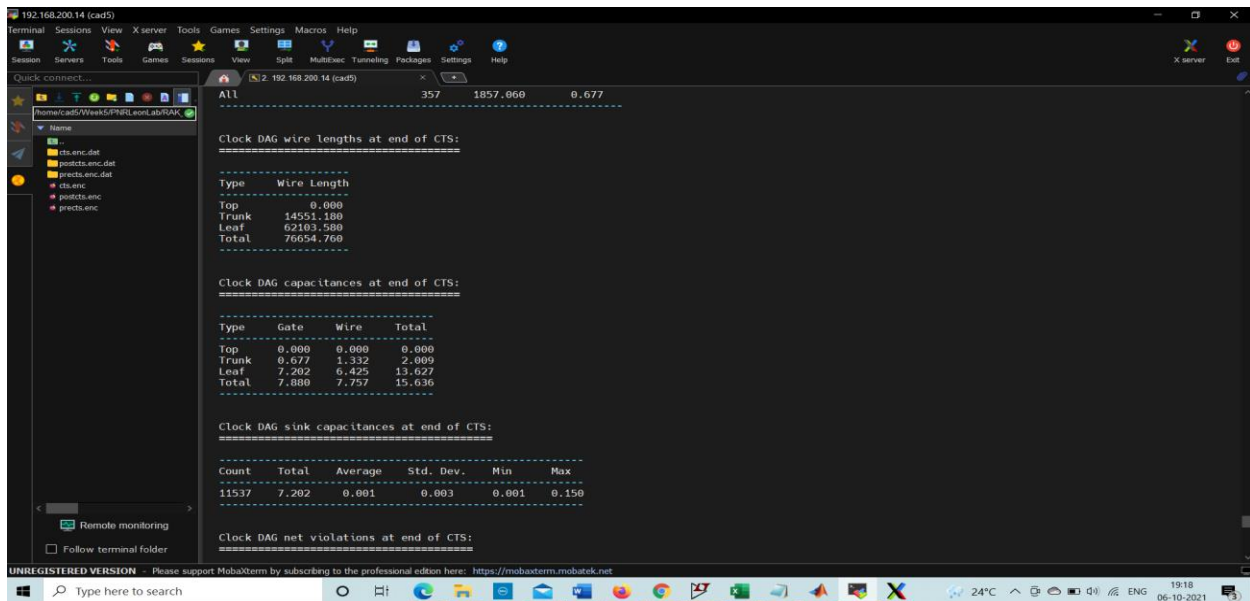
Total wire length is reported

Worst and total set-up and hold delays are reported

Also, all the timing violations are reported after the CTS and the cells or instances for timing violations are reported.



## 10. Provide a snapshot of the total wire length after Routing



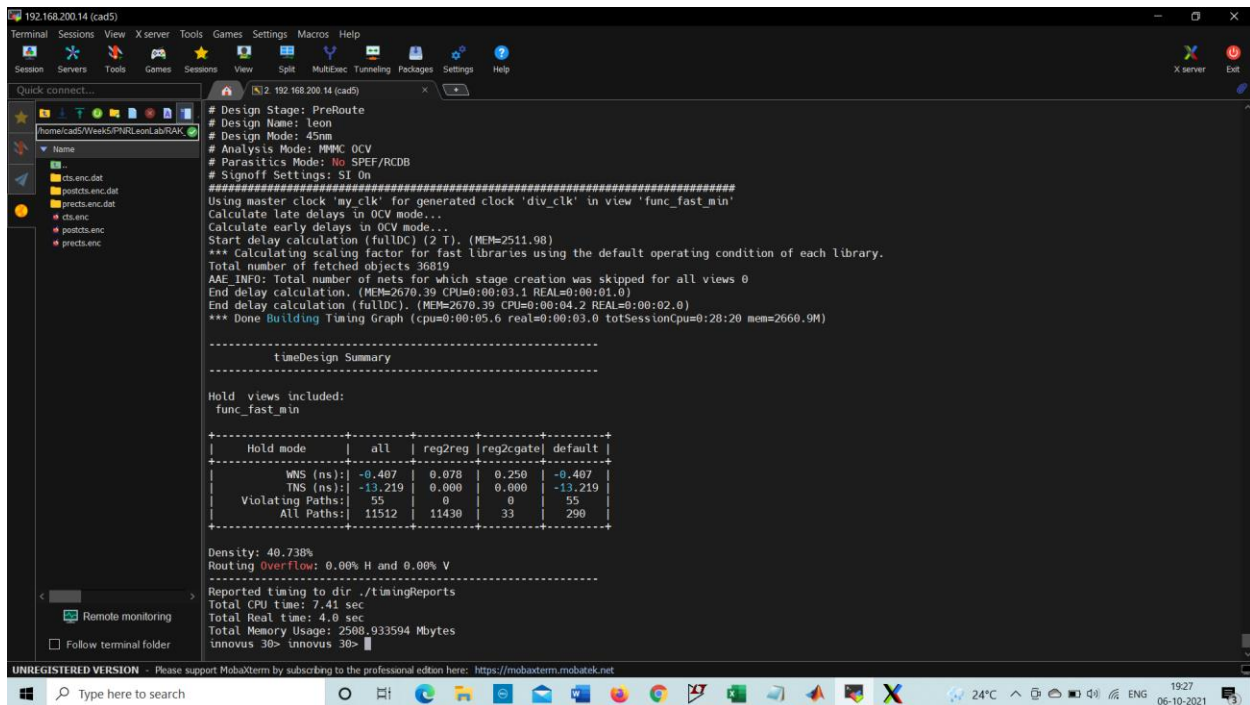
Fig(10.1): The total wire length after Routing

## 11. Provide a timing summary of post Route hold timing and mention the violating paths

We are getting the updated values of Violation Path and Density

Violation Path =55

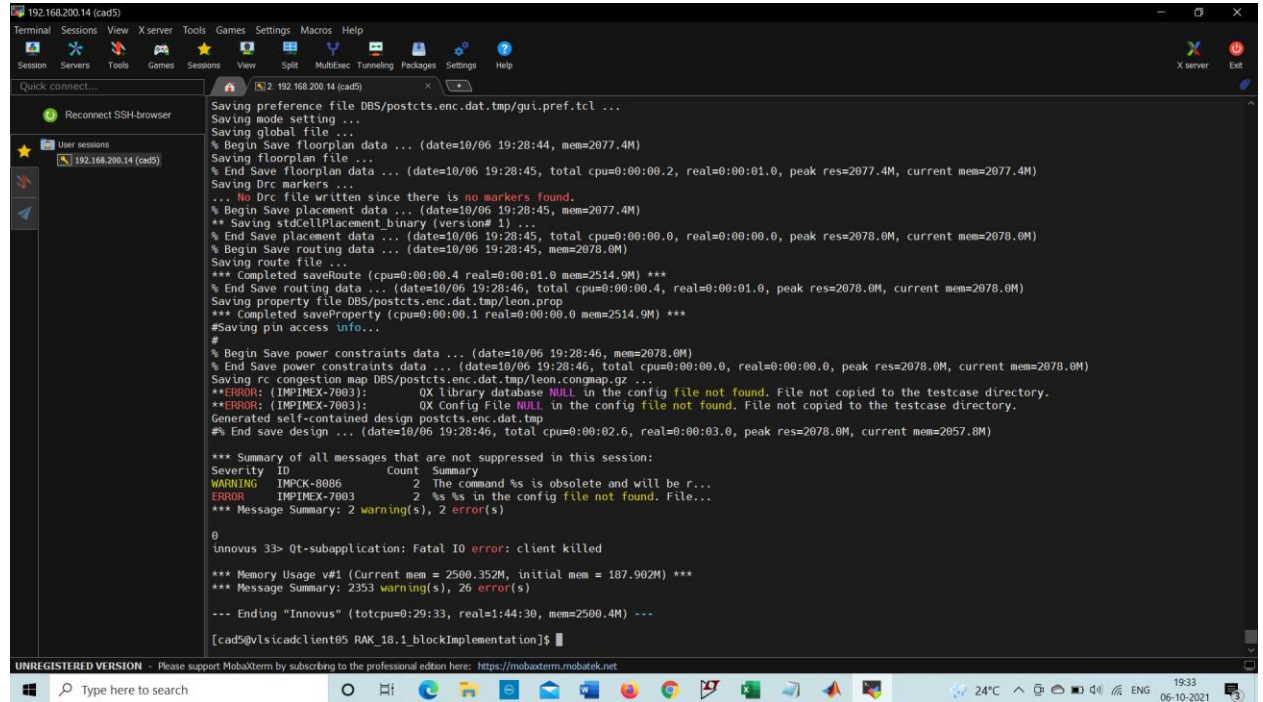
Density=40.738%



Fig(11.1): Timing summary of post Route hold timing

12) After you streamout GDS, what is the total instance count

After finishing post-route hold timing, we tried executing the further processes required to extract GDS. But we got exited from innovus multiple times (screenshots are attached ) and we were unable to move ahead.

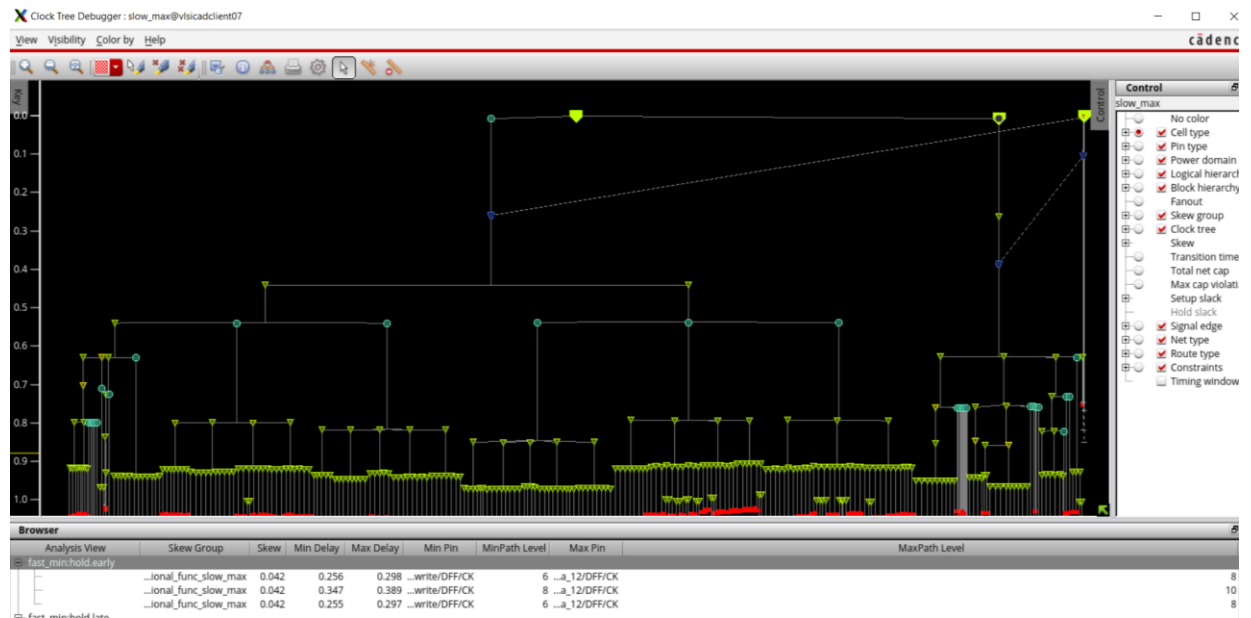


```
192.168.200.14 (cad5)
Terminal Sessions View X server Tools Games Settings Macros Help
Quick connect...
Reconnect SSH-browser
User sessions
192.168.200.14 (cad5)
Saving preference file DBS/postcts.enc.dat.tmp/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=10/06 19:28:44, mem=2077.4M)
Saving floorplan file ...
% End Save floorplan data ... (date=10/06 19:28:45, total cpu=0:00:00.2, real=0:00:01.0, peak res=2077.4M, current mem=2077.4M)
Saving Drc markers ...
... No Drc file written since there is no markers found.
** Saving stdCellPlacement_binary (version# 1) ...
% End Save placement data ... (date=10/06 19:28:45, total cpu=0:00:00.0, real=0:00:00.0, peak res=2078.0M, current mem=2078.0M)
% Begin Save routing data ... (date=10/06 19:28:45, mem=2078.0M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.4 real=0:00:01.0 mem=2514.9M) ***
% End Save routing data ... (date=10/06 19:28:46, total cpu=0:00:00.4, real=0:00:01.0, peak res=2078.0M, current mem=2078.0M)
Saving property file DBS/postcts.enc.dat.tmp/leon.prop
*** Completed saveProperty (cpu=0:00:00.1 real=0:00:00.0 mem=2514.9M) ***
#Saving pin access info...
% Begin Save power constraints data ... (date=10/06 19:28:46, mem=2078.0M)
% End Save power constraints data ... (date=10/06 19:28:46, total cpu=0:00:00.0, real=0:00:00.0, peak res=2078.0M, current mem=2078.0M)
Saving rc congestion map DBS/postcts.enc.dat.tmp/leon.congmap.gz ...
**ERROR: (IMPIMEX-7003): OX library database NULL in the config file not found. File not copied to the testcase directory.
**ERROR: (IMPIMEX-7003): OX config File NULL in the config file not found. File not copied to the testcase directory.
% End save design ... (date=10/06 19:28:46, total cpu=0:00:02.6, real=0:00:03.0, peak res=2078.0M, current mem=2057.8M)

*** Summary of all messages that are not suppressed in this session:
Severity ID Count Summary
WARNING IMPCK-8006 2 The command %s is obsolete and will be r...
ERROR IMPIMEX-7003 2 %s %s in the config file not found. File...
*** Message Summary: 2 warning(s), 2 error(s)

0
innovus 33> Qt-subapplication: Fatal I/O error: client killed
*** Memory Usage v#1 (Current mem = 2500.352M, initial mem = 187.902M) ***
*** Message Summary: 2353 warning(s), 26 error(s)

--- Ending "Innovus" (totcpu=0:29:33, real=1:44:30, mem=2500.4M) ---
[cad5@vlsicadclient05 RAK_18.1_blockImplementation]$
```



IP ADDRESS :

```
192.168.200.14 (cad5)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
home/cad5/Week5/PNRLLeonLabRAK
Name
 cadence
 DATA
 files
 Docs
 leon_vkrum.dat
 LIBS
 SCRIPTS
 timingReports
 crypt.spec
 enc.tcl
 innovus.cmd
 innovus.cmd1
 innovus.log
 innovus.log1
 innovus.logv
 innovus.logv1
 leon_checkPlace
 leon.spf
 leon_vkrum
 postILPns.log
 top.martip

Remote monitoring
Follow terminal folder

Global 'timing.disable.inferred.clock.gating.checks.sequential' has become obsolete. It will be removed in the next release.
**WARN: (GLOBAL-100): Global 'timing.disable.default.arc' has become obsolete. It will be removed in the next release.
**ERROR: (GLOBAL-105): Unknown global 'timing.enable.backward.compatible.case.analysis.mode' specified
**WARN: (GLOBAL-100): Global 'timing.aocv.slack.threshold' has become obsolete. It will be removed in the next release.
**WARN: (GLOBAL-100): Global 'timing.enable.backward.compatible.pulse.width.check' has become obsolete. It will be removed in the next release.
**ERROR: (GLOBAL-105): Unknown global 'timing.enable.efficient.input.output.delay.mode' specified
**WARN: (GLOBAL-100): Global 'timing.enable.backward.compatible.cpr.mode' has become obsolete. It will be removed in the next release.
**ERROR: (GLOBAL-105): Unknown global 'timing.enable.backward.compatible.pessimistic.cpr.mode' specified
**WARN: (GLOBAL-100): Global 'timing.aocv.enable.gba.combine.launch.capture' has become obsolete. It will be removed in the next release.
**WARN: (IMPCK-8086): The command specifyClockTree is obsolete and will be removed in the next release. This command still works in this release, but by the
next release you must transition to the COOpt-based CTS flow.
source DATA/route.enc.dat/leon_power_constraints.tcl
innovus >
innovus > ifconfig
em1: flags=4163<UP,BROADCAST,RUNNING,MULTICAST> mtu 1500
 inet 192.168.200.14 netmask 255.255.0.0 broadcast 192.168.255.255
 inet6 fe80::ea15:c58b:a194:29a9 prefixlen 64 scopeid 0x20<link>
 ether e4:54:00:a7:7a:09 txqueuelen 1000 (Ethernet)
 RX packets 1367054 bytes 1191545585 (1.1 GiB)
 RX errors 0 dropped 37 overruns 0 frame 0
 TX packets 1099483 bytes 937508652 (894.0 MiB)
 TX errors 0 dropped 0 overruns 0 carrier 0 collisions 0
 device interrupt 16 memory 0xa2c00000-a2c20000

lo: flags=73<UP,LOOPBACK,RUNNING> mtu 65536
 inet 127.0.0.1 netmask 255.0.0.0
 inet6 ::1 prefixlen 128 scopeid 0x10<host>
 loop txqueuelen 1000 (Local Loopback)
 RX packets 63171 bytes 1508697858 (1.4 GiB)
 RX errors 0 dropped 0 overruns 0 frame 0
 TX packets 63171 bytes 1508697858 (1.4 GiB)
 TX errors 0 dropped 0 overruns 0 carrier 0 collisions 0

virbr0: flags=4099<UP,BROADCAST,MULTICAST> mtu 1500
 inet 192.168.122.1 netmask 255.255.255.0 broadcast 192.168.122.255
 ether 52:54:00:a7:7a:09 txqueuelen 1000 (Ethernet)
 RX packets 0 bytes 0 (0.0 B)
 RX errors 0 dropped 0 overruns 0 frame 0
 TX packets 0 bytes 0 (0.0 B)
 TX errors 0 dropped 0 overruns 0 carrier 0 collisions 0

innovus >

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```

IP ADDRESS LOG FILE

```
192.168.200.14 (cad5)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
home/cad5/Week5/PNRLLeonLabRAK
Name
 cadence
 DATA
 files
 Docs
 leon_vkrum.dat
 LIBS
 SCRIPTS
 timingReports
 crypt.spec
 enc.tcl
 innovus.cmd
 innovus.cmd1
 innovus.log
 innovus.log1
 innovus.logv
 innovus.logv1
 leon_checkPlace
 leon.spf
 leon_vkrum
 postILPns.log
 top.martip

Remote monitoring
Follow terminal folder

next release you must transition to the COOpt-based CTS flow.
source DATA/route.enc.dat/leon_power_constraints.tcl
innovus >
innovus > ifconfig
em1: flags=4163<UP,BROADCAST,RUNNING,MULTICAST> mtu 1500
 inet 192.168.200.14 netmask 255.255.0.0 broadcast 192.168.255.255
 inet6 fe80::ea15:c58b:a194:29a9 prefixlen 64 scopeid 0x20<link>
 ether e4:54:00:a7:7a:09 txqueuelen 1000 (Ethernet)
 RX packets 1367054 bytes 1191545585 (1.1 GiB)
 RX errors 0 dropped 37 overruns 0 frame 0
 TX packets 1099483 bytes 937508652 (894.0 MiB)
 TX errors 0 dropped 0 overruns 0 carrier 0 collisions 0
 device interrupt 16 memory 0xa2c00000-a2c20000

lo: flags=73<UP,LOOPBACK,RUNNING> mtu 65536
 inet 127.0.0.1 netmask 255.0.0.0
 inet6 ::1 prefixlen 128 scopeid 0x10<host>
 loop txqueuelen 1000 (Local Loopback)
 RX packets 63171 bytes 1508697858 (1.4 GiB)
 RX errors 0 dropped 0 overruns 0 frame 0
 TX packets 63171 bytes 1508697858 (1.4 GiB)
 TX errors 0 dropped 0 overruns 0 carrier 0 collisions 0

virbr0: flags=4099<UP,BROADCAST,MULTICAST> mtu 1500
 inet 192.168.122.1 netmask 255.255.255.0 broadcast 192.168.122.255
 ether 52:54:00:a7:7a:09 txqueuelen 1000 (Ethernet)
 RX packets 0 bytes 0 (0.0 B)
 RX errors 0 dropped 0 overruns 0 frame 0
 TX packets 0 bytes 0 (0.0 B)
 TX errors 0 dropped 0 overruns 0 carrier 0 collisions 0

innovus > ls -lrt innovus*
-rw-rw-r-- 1 cad5 cad5 125864 Oct 2 23:10 innovus.cmd
-rw-rw-r-- 1 cad5 cad5 1570996 Oct 2 23:15 innovus.logv
-rw-rw-r-- 1 cad5 cad5 678808 Oct 2 23:15 innovus.log
-rw-rw-r-- 1 cad5 cad5 1357 Oct 2 23:20 innovus.cmd1
-rw-rw-r-- 1 cad5 cad5 3722 Oct 2 23:29 innovus.logv1
-rw-rw-r-- 1 cad5 cad5 1595 Oct 2 23:29 innovus.log1
-rw-rw-r-- 1 cad5 cad5 171018 Oct 6 17:52 innovus.logv2
-rw-rw-r-- 1 cad5 cad5 132720 Oct 6 17:52 innovus.log2
-rw-rw-r-- 1 cad5 cad5 2214 Oct 6 17:52 innovus.cmd2

innovus >

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```