----------ASSIGNMENT 3: INNOVUS RAK----------

Submitted By: Group Members

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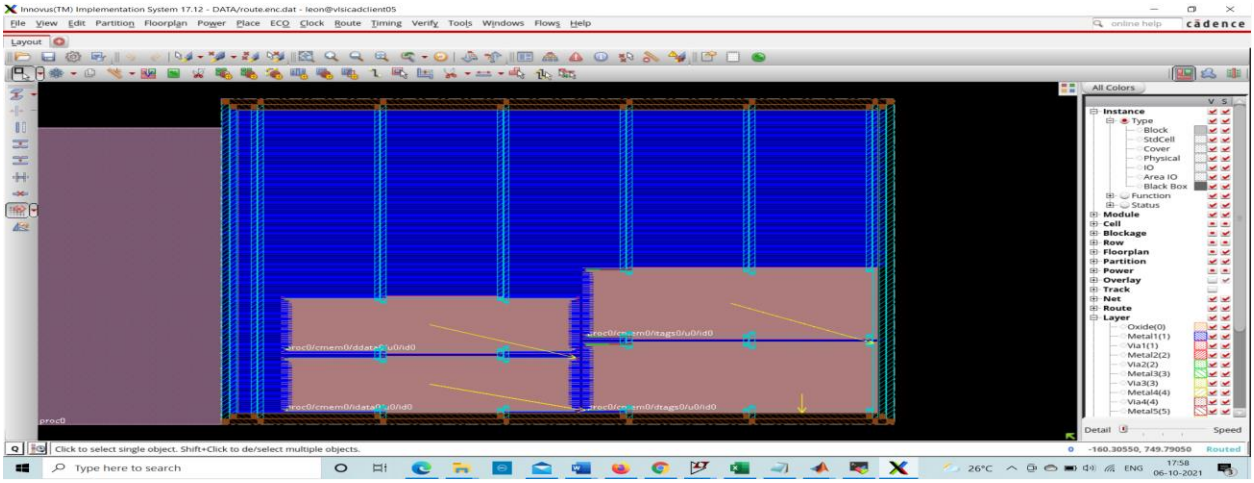
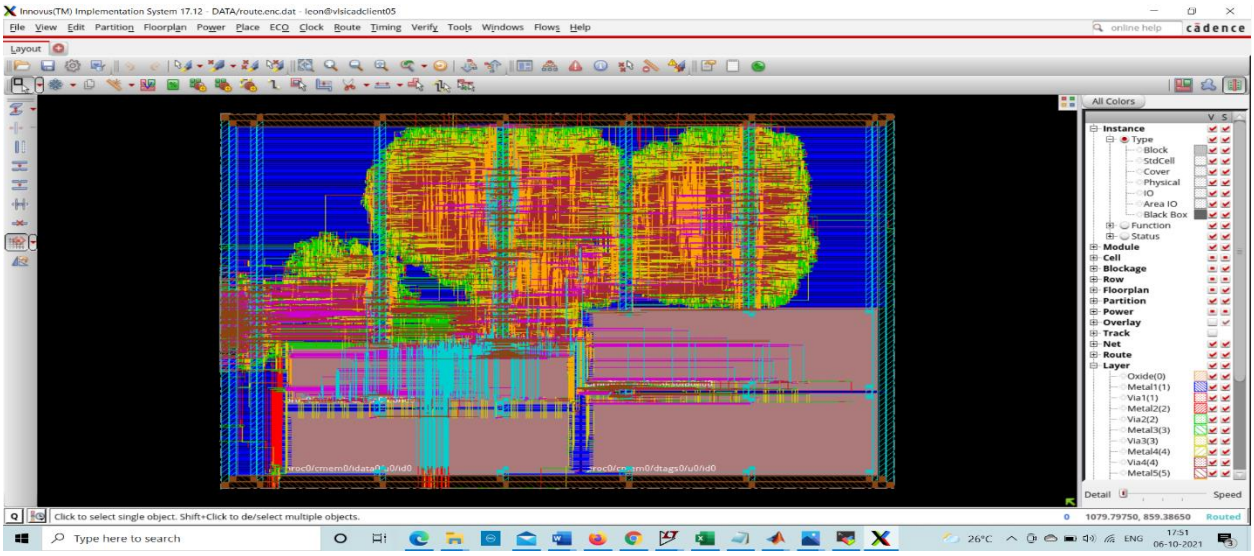
Step 1) Extract the RAK database and change directory to the work directory:

The floorplan has the blocks placed and power routing complete. From here we can do the implementation flow



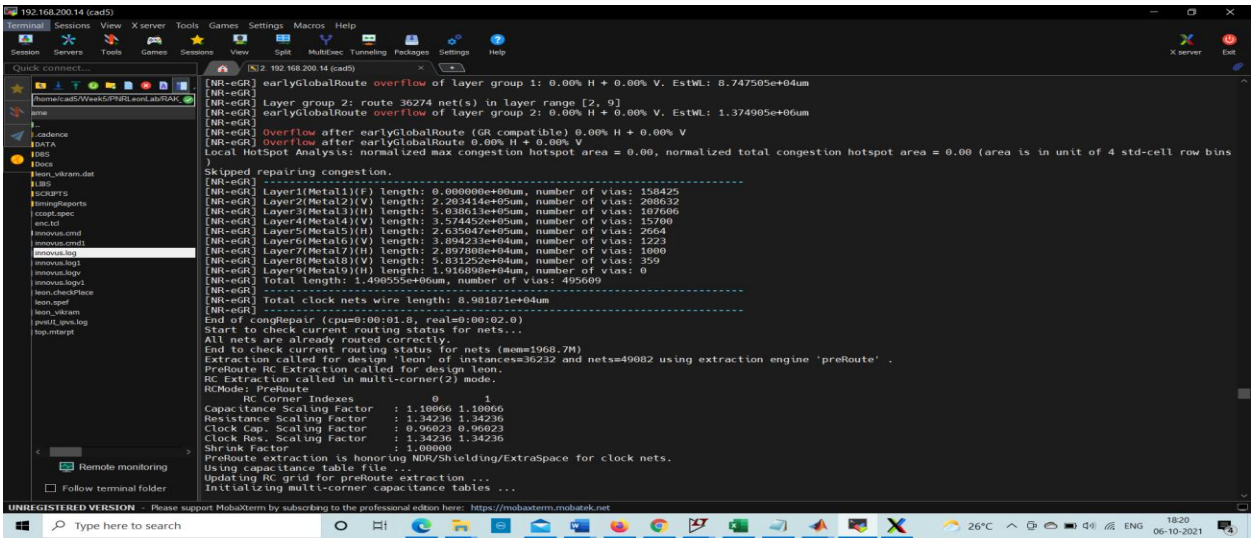
Fig(1.1): Floorplan



Fig(1.2):Physical view after placement and preCTS optimization

When both the placement and preCTS optimizations done, we can start looking at the placed design in the Physical views. We can Observe the placed standard cells are shown in the Physical view

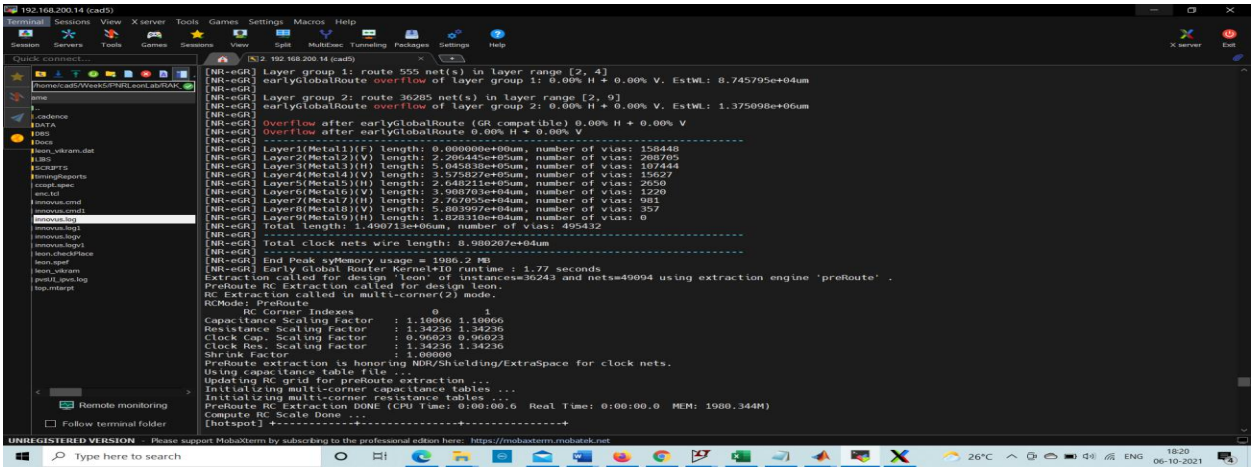
1. After you run the place_opt_design,
    a. How many metal layers exist in the design and how many vias exist in each layer



Fig(1.3.1): Number of Metal Layer and Vias

Metal Layer = 9
Number of vias = 495609

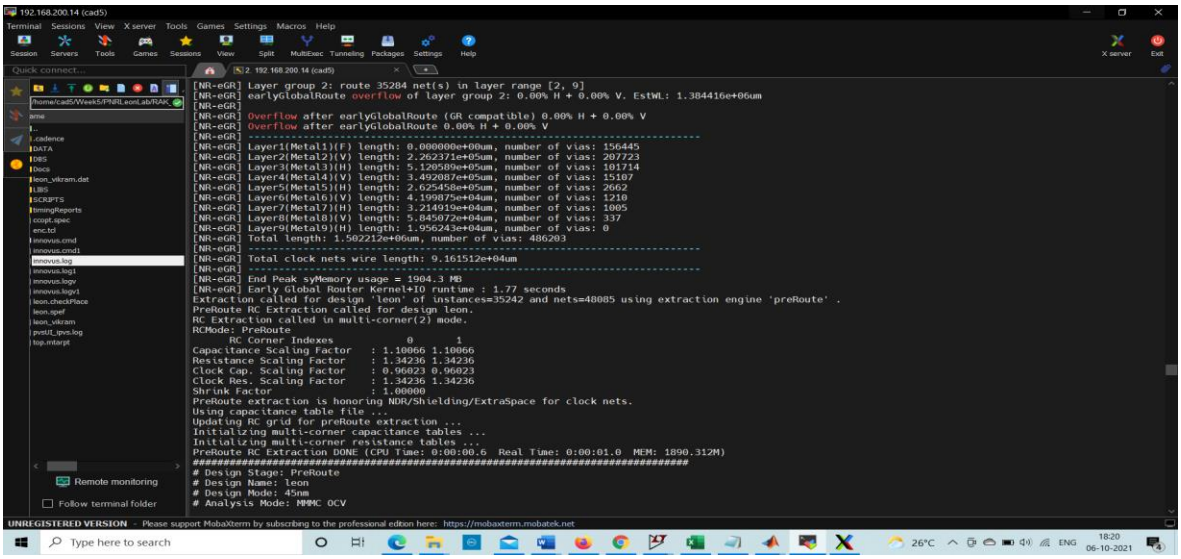
Layer1	Layer2	Layer3	Layer4	Layer5	Layer6	Layer7	Layer8	Layer9
158425	208632	107606	15700	2664	1223	1000	359	0



Fig(1.3.2): Number of Metal Layer and Vias

Metal Layer = 9
Number of vias = 495432

Layer1	Layer2	Layer3	Layer4	Layer5	Layer6	Layer7	Layer8	Layer9
158448	208705	107444	15627	2650	1220	981	357	0

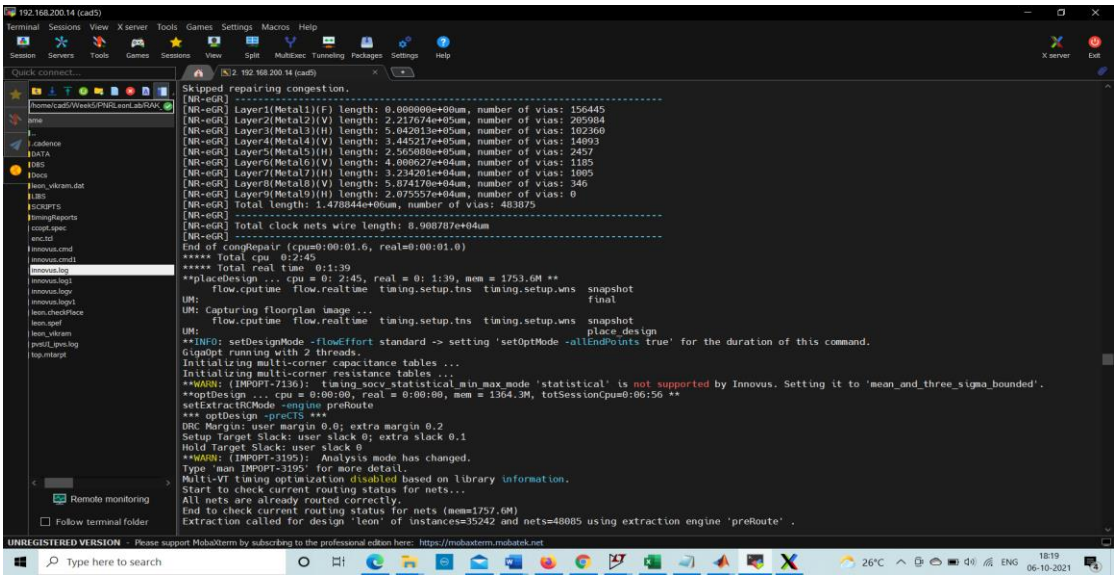


Fig(1.3.3): Number of Metal Layer and Vias

Metal Layer = 9

Number of vias = 486203

Layer1	Layer2	Layer3	Layer4	Layer5	Layer6	Layer7	Layer8	Layer9
156445	207723	101714	15107	2662	1210	1005	337	0



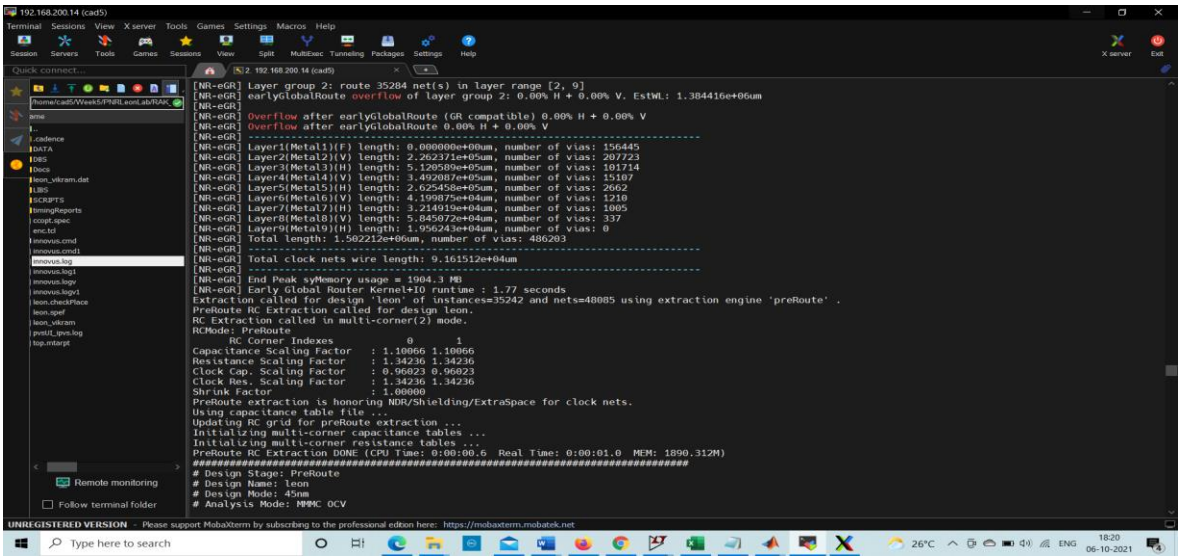
Fig(1.3.4): Number of Metal Layer and Vias

Metal Layer = 9

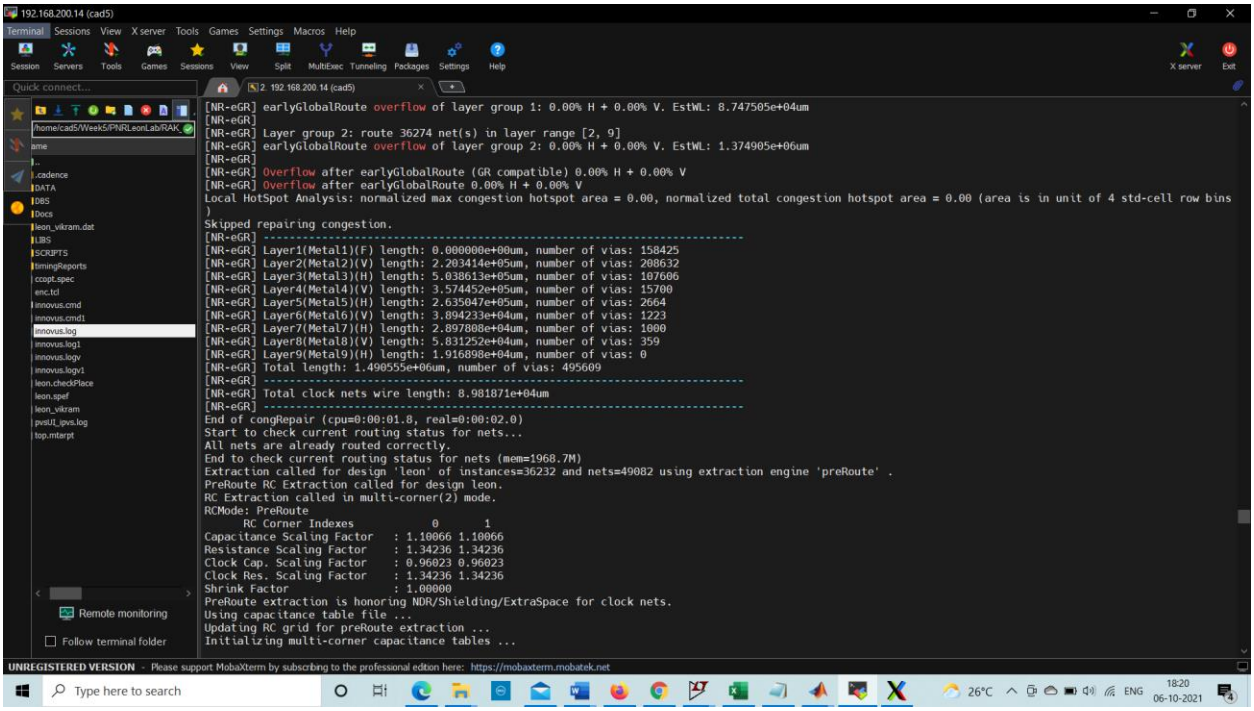
Number of vias = 483875

Layer1	Layer2	Layer3	Layer4	Layer5	Layer6	Layer7	Layer8	Layer9
156445	205984	102360	14093	2457	1185	1005	346	0

b. During preRoute, how many instances and nets exist in the Leon design during the "preRoute" stage



Fig(1.4): Instances = 35242 and Nets= 48085 (Leon Design) during PreRoute



Fig(1.5): Instances=36232and Nets=49082 (Leon Design) during PreRoute

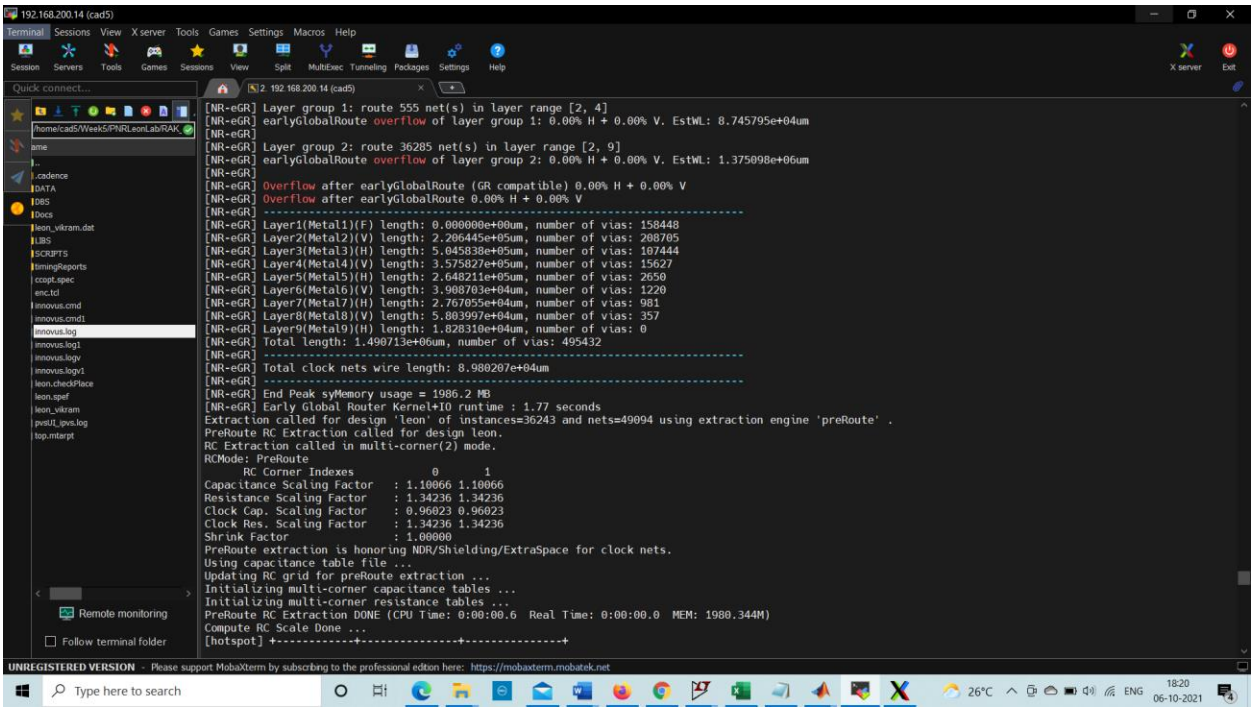
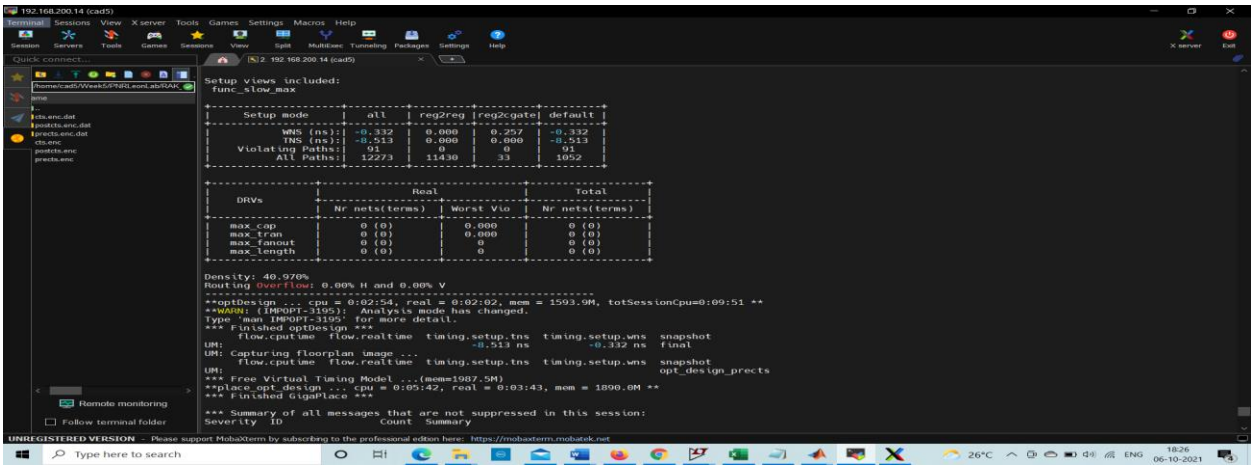


Fig (1.6): Instances=36243 and Nets=49094 (Leon Design) during PreRoute

2. After you run Check Placement, what is the Placement density? How many cells have been placed? (Take a screenshot)

Here we are showing the Timing summary , so that we can easily see timing results after optimization as well as standard cell utilization (density) and it give us the EarlyGlobalRoute overflow values.



Fig(2.1) :Placement Density=40.970%

The total number of cell which are placed after optimization

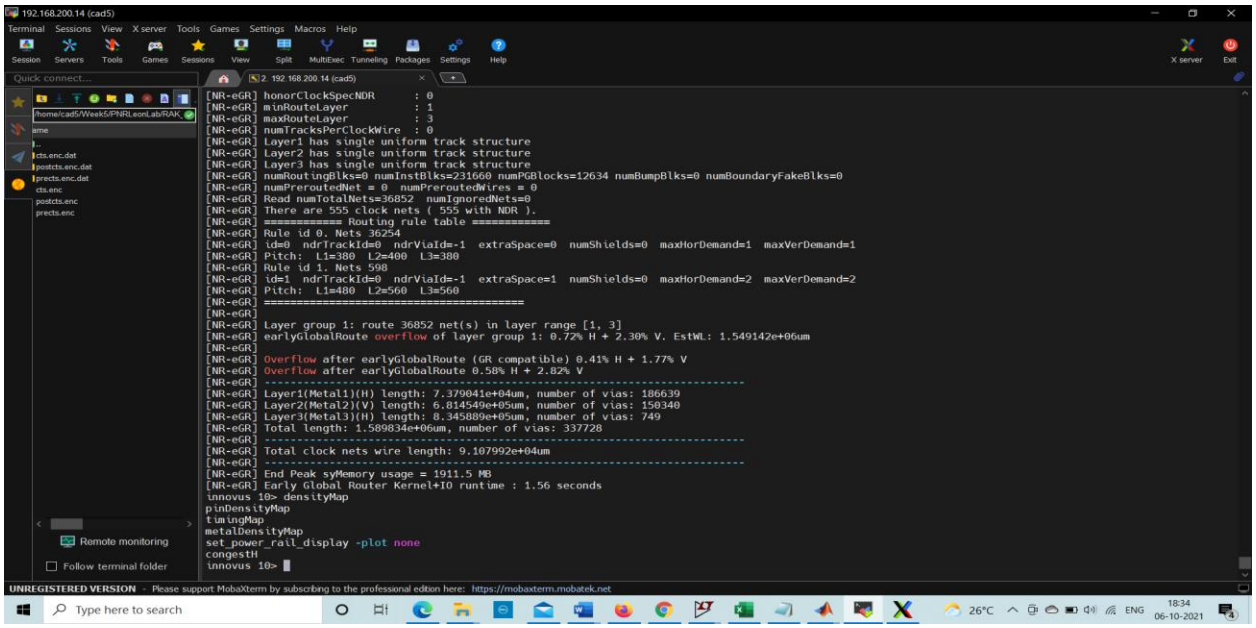
Number of Cells placed = 36339

Step: Running Early Global Route

Early Global Route defined as the group of global routing & track assignment which correlates well to detail route while running in a very small amount of the time. here we are demonstrating the route congestion by limiting the number of metal routing layers from 1 to 3

3. a. After you run Early Global Route with just 3 Metal Layers, what is the number of vias on each layer.

Layer1	Layer2	Layer3
186639	150340	749



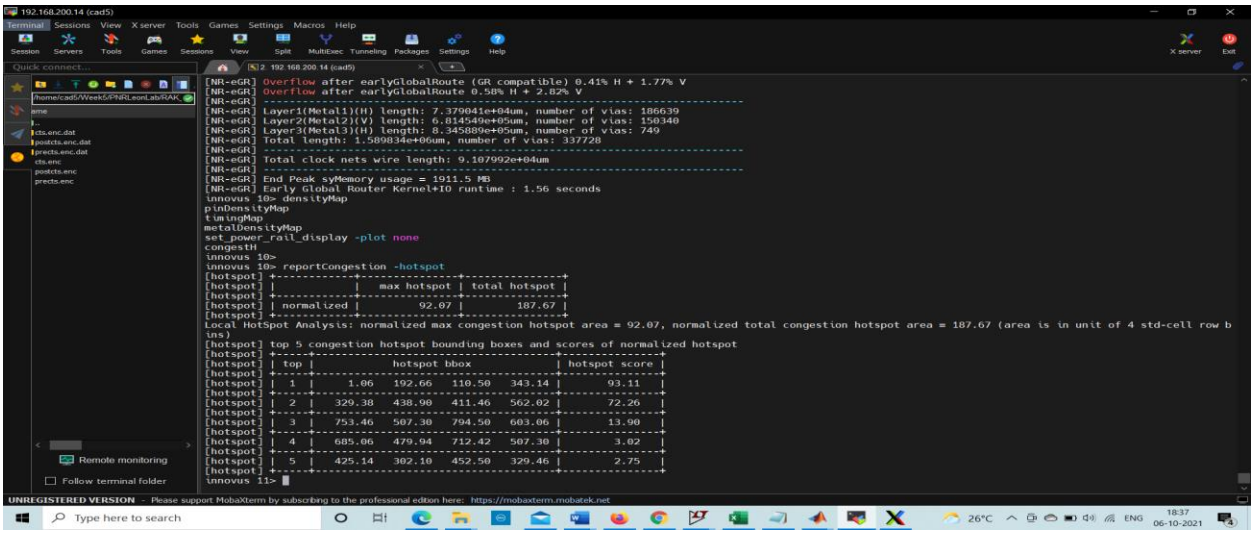
Fig(3.1):Number of Vias on each metal layer after EGR with 3Metal Layer

b. which is of these layers is Vertical?

Layer2(Metal2)=Vertical

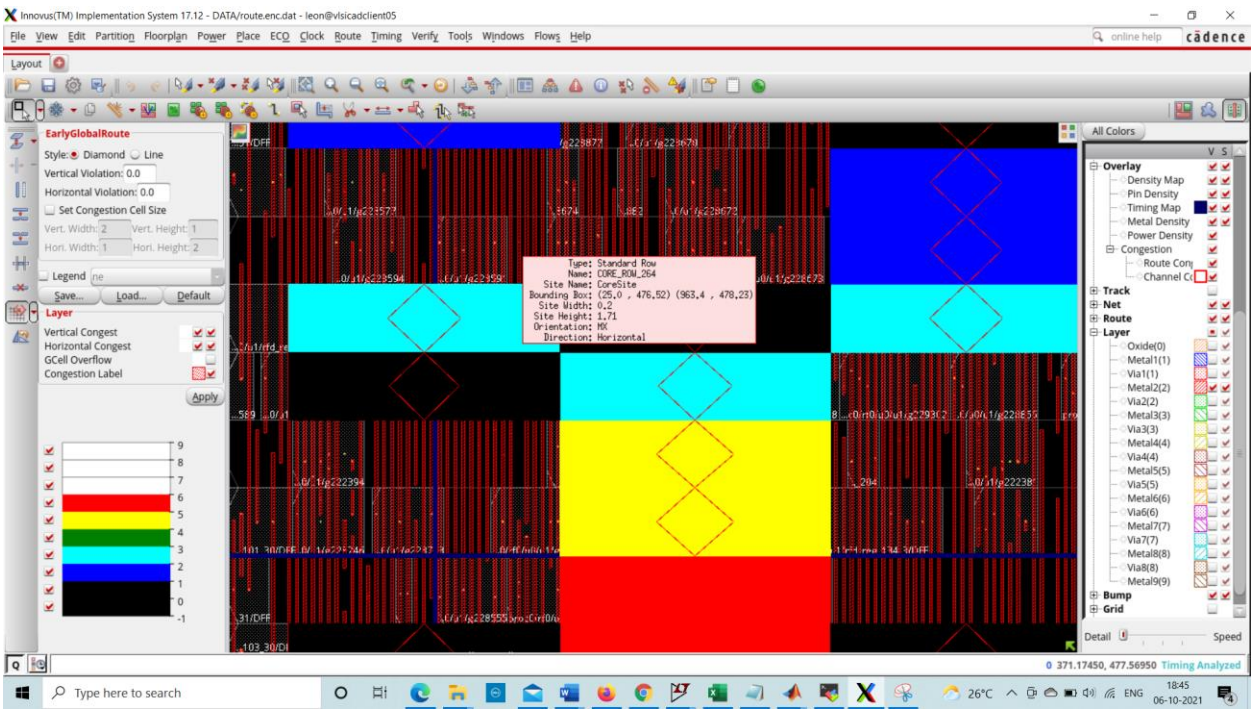
c. What is the Congestion Report after EarlyGlobal Route with just 3 layers

Here we can see the total number of Hotspots are 5 when we are using the 3layers.



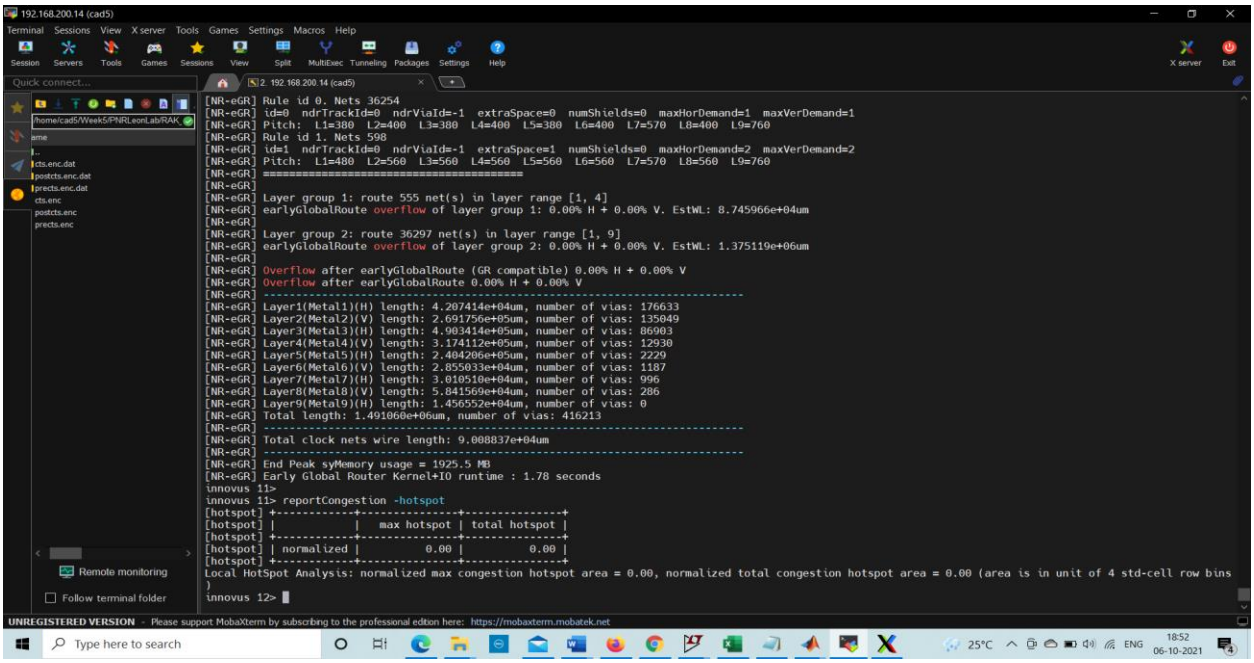
Fig(3.2):Congestion Report (for 3 Layers)

d. With Overlay and Net highlighted, only on Metal 2, Zoom into Core_Row_264. Now Zoom out and take a snapshot of the entire Innovus window which shows congestion marks.



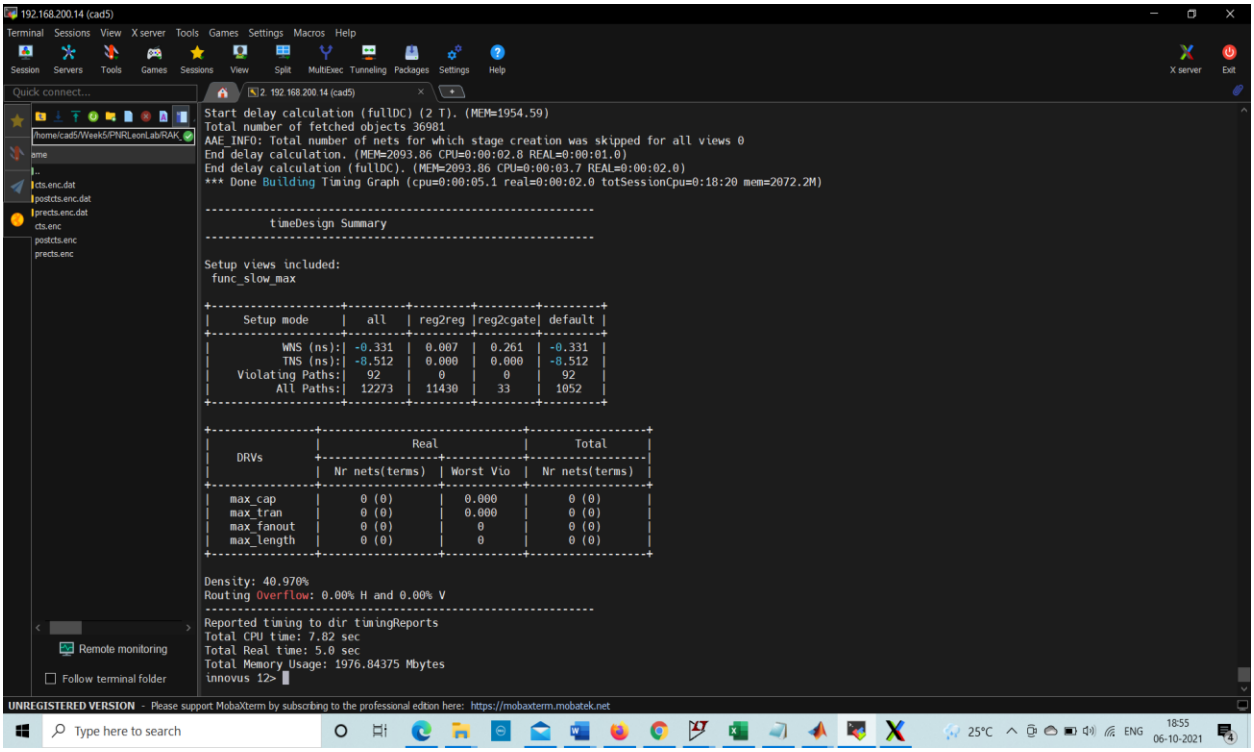
Fig(3.3): 2-D view of Early Global Congestion of Core_Row_264

4. Now, after you change the number of Layers to 9, report Congestion again. Provide a snapshot of how many hotspots exist now?



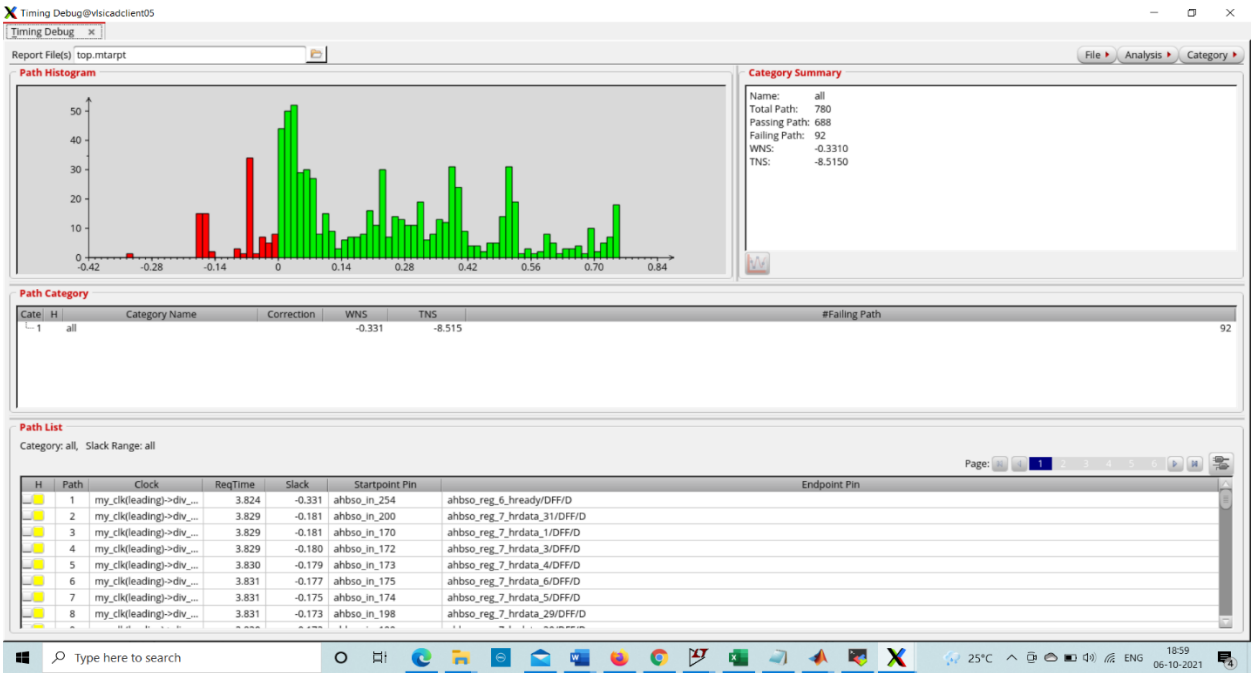
Fig(4.1):Number of Hotspots after giving range to 9 layers

5. After Pre-CTS timing, how many reg2reg paths have violated Setup timing?

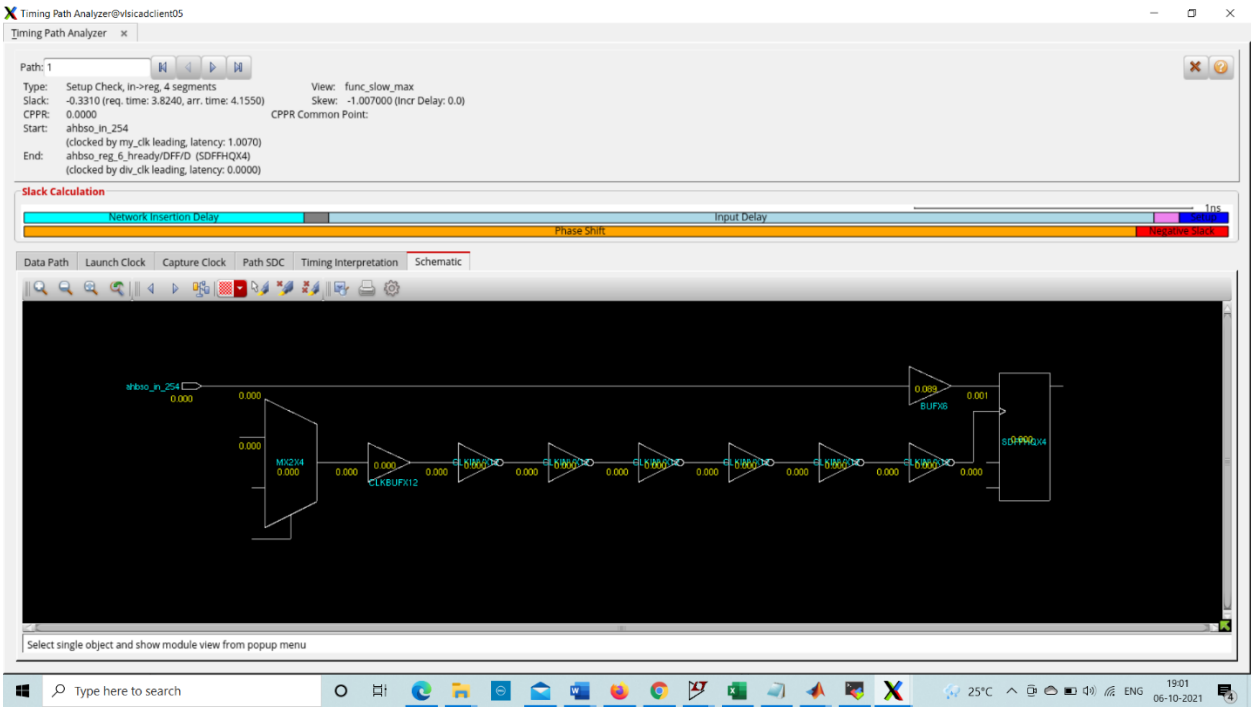


Fig(5.1):reg2reg paths have violated setup timing=92

6. Open global timing debug after the pre-cts timing and take a snapshot of the Schematic of the 1st path that violated timing



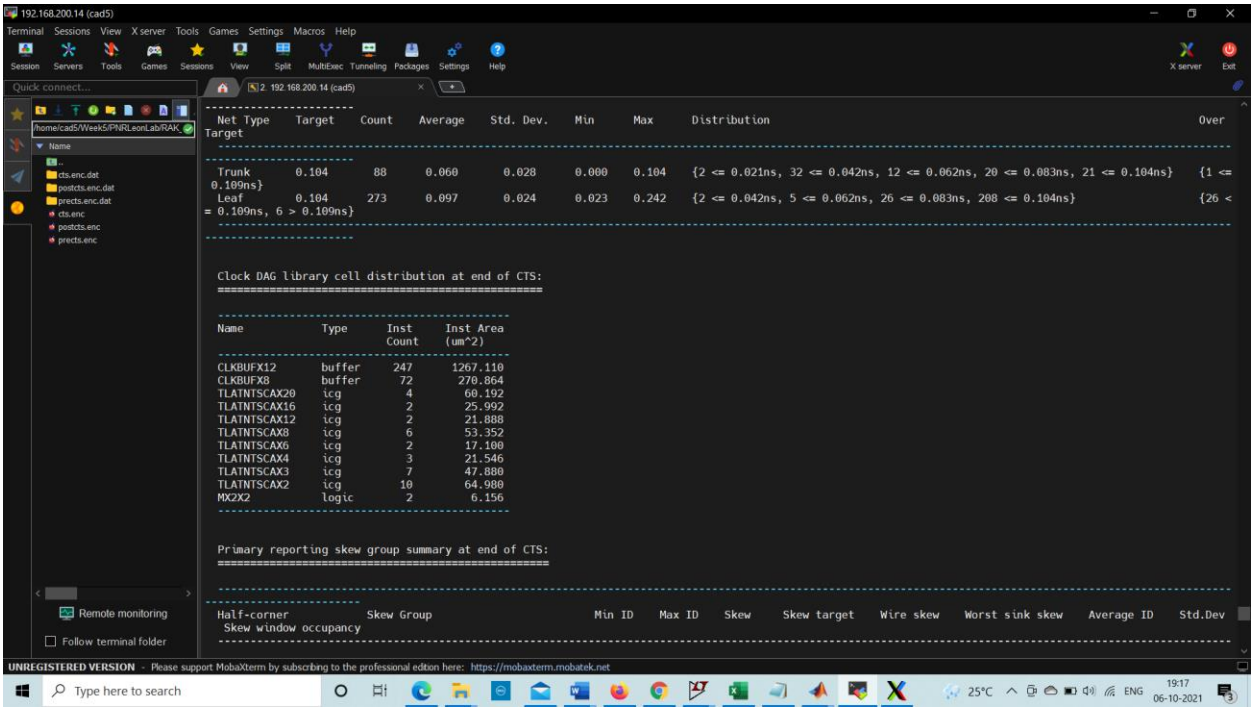
Fig(6.1):Global Timing Debug Interface



Fig(6.2): Schematic of the 1st path that violated timing

7. After running CTS, list the names and the number of the CLK Buffer cells and Clock Gating cells (ICG) used in the design

   Total= (319) CLKBUFFER+ (36) ICG were used in the design of different drive strengths



Fig(7.1): Number of the CLK Buffer cells and Clock Gating cells (ICG) used in the design

8. After running CTS, what is the total wire capacitance and gate capacitance reported by CCOPT

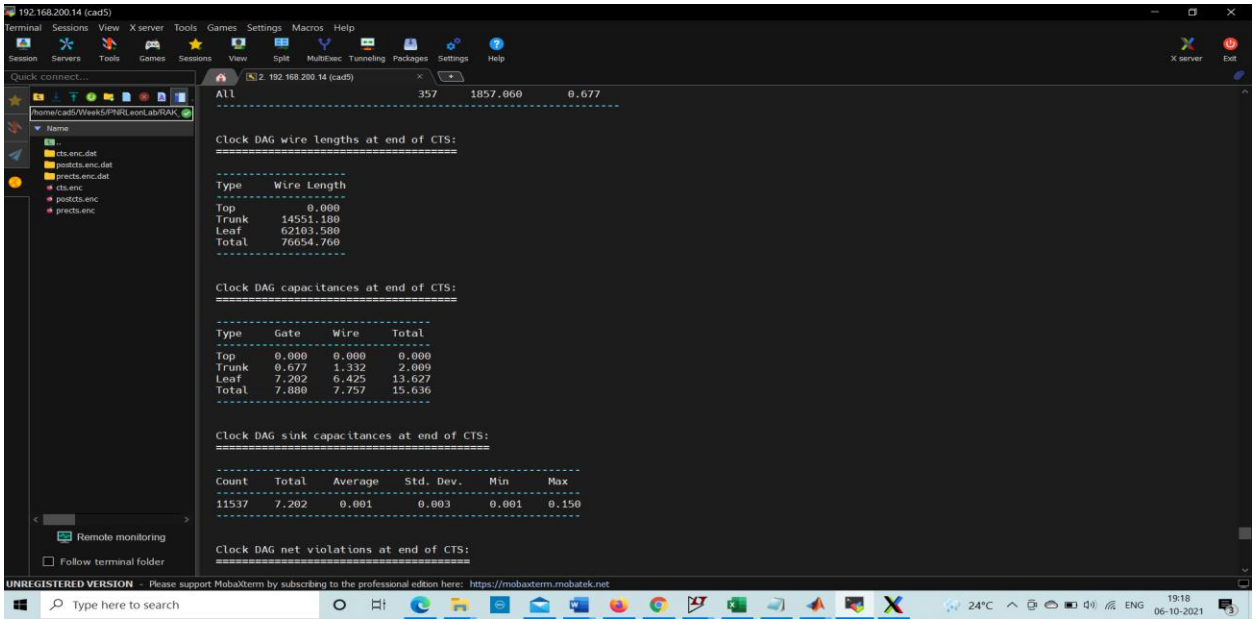


Fig (8.1): The total wire capacitance and gate capacitance reported by CCOPT

9. What are the different steps (or functions) the tool went through during CTS

Start the CCopt Design: Here the Process is Clock concurrent optimization merges physical optimization into clock tree synthesis and simultaneously optimizes clock delay and logic delay using a single unified cost metric

Routing table rules are specified, layers and vias details read

Updating RC grid for preRoute extraction.

Initializing multi-corner capacitance tables.

Initializing multi-corner resistance tables.

Pre-route RC extraction done

Slew time targets are specified

Delays of BUFFERS, INV and ICG'sare specified along with other specifications

Delay constrainst for Via's is reported

In resynthesis clock gate merging summary is created and reason of mering is also mentioned
New netlist is created and merged clocks are removed.

Then clock tree optimization is carry out using different type of methods clustering is one of them and after each step the innovus sees if the pre-reqisites are met if not it tries other methid of optimisation.

Verification done and after the final optimization the result for worst and total delay paths are reported.

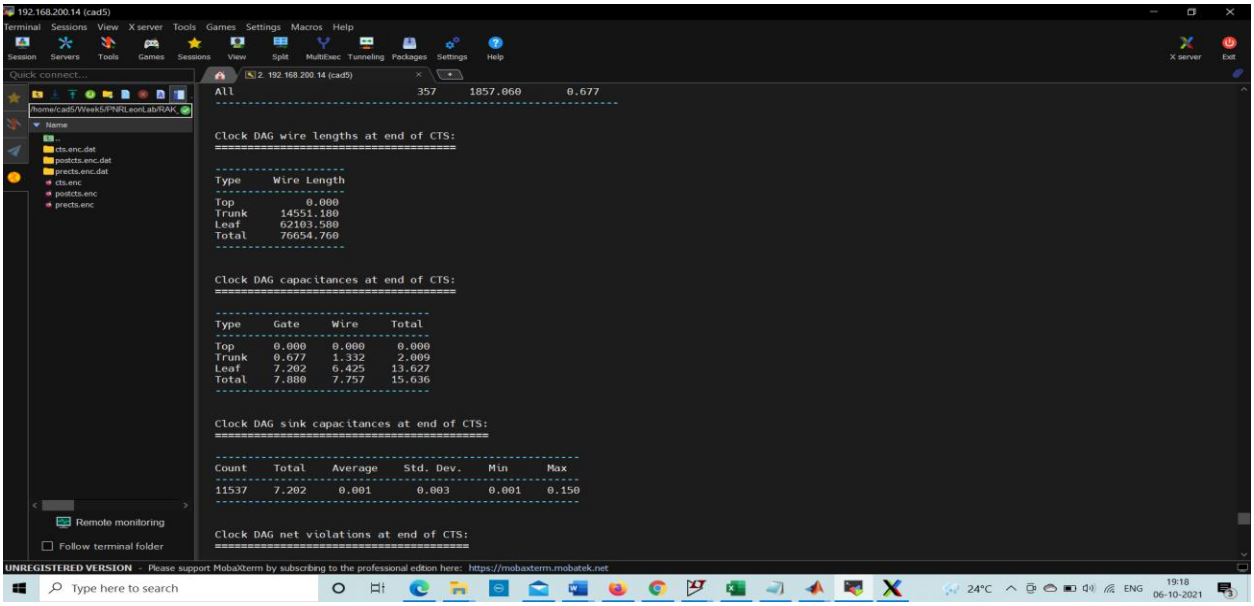
Total Wire and gate capacitances are reported

Total wire length is reported

Worst and total set-up and hold delays are reported

Also, all the timing violations are reported after the CTS and the cells or instances for timing violations are reported.

10. Provide a snapshot of the total wire length after Routing



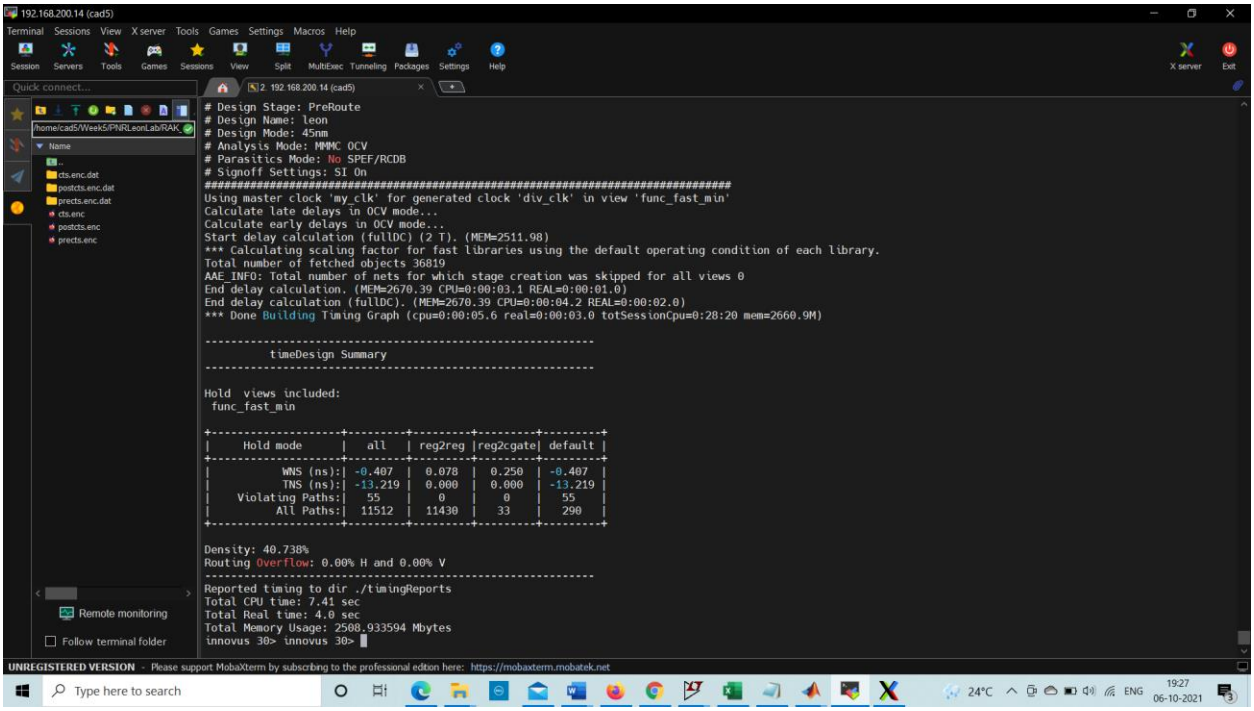
Fig(10.1): The total wire length after Routing

11. Provide a timing summary of post Route hold timing and mention the violating paths

We are getting the updated values of Violation Path and Density

Violation Path =55

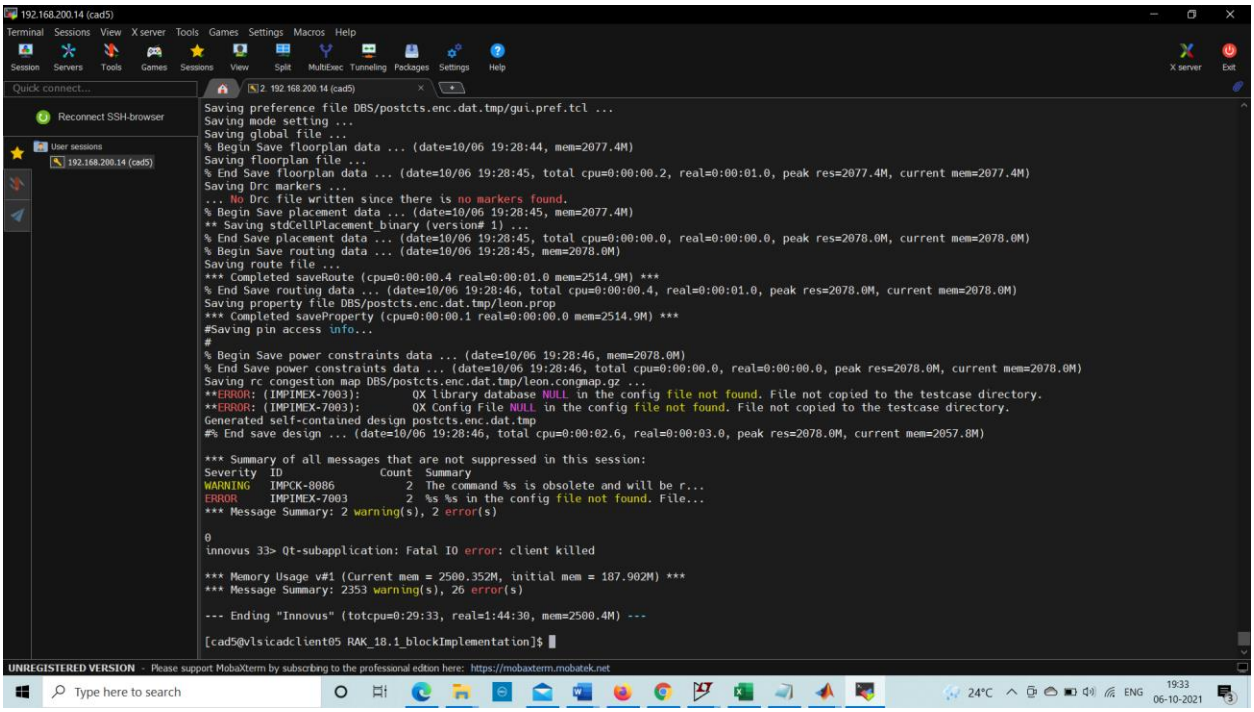
Density=40.738%

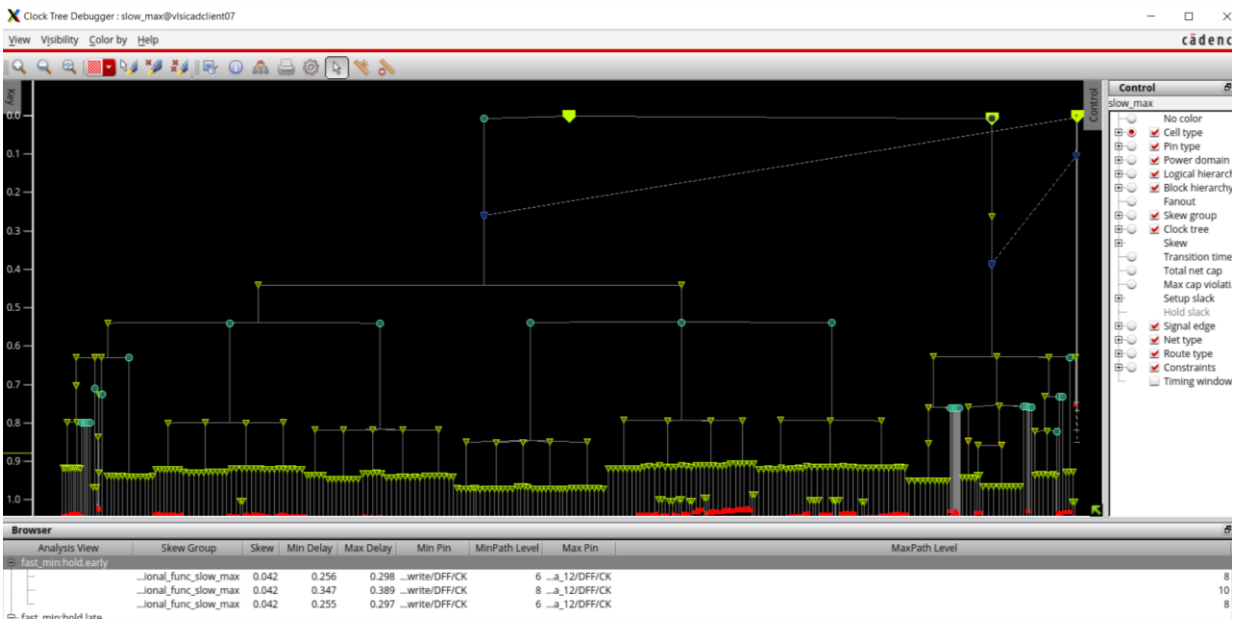


Fig(11.1): Timing summary of post Route hold timing

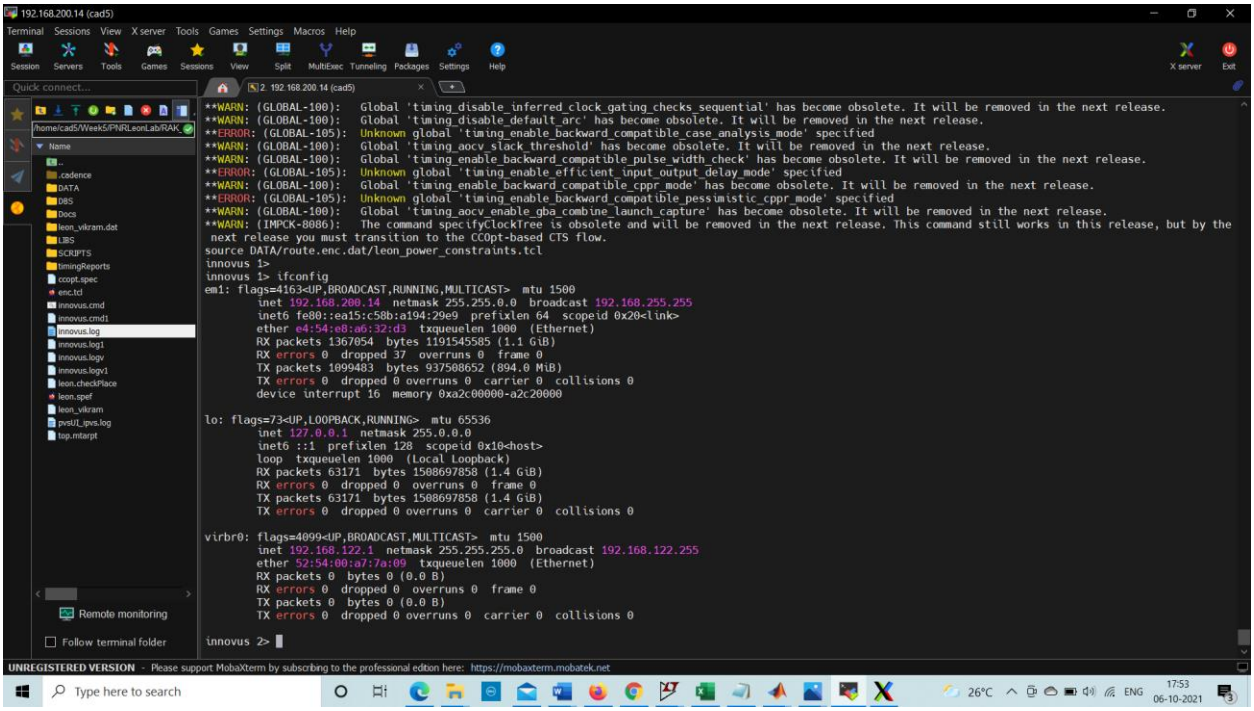
12) After you streamout GDS, what is the total instance count

After finishing post-route hold timing, we tried executing the further processes required to extract GDS. But we got exited from innovus multiple times (screenshots are attached) and we were unable to move ahead.





IP ADDRESS :



IP ADDRESS LOG FILE