Quadruple Cross-Coupled Latch-Based 10T and 12T SRAM Bit-Cell Designs

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PROBLEM STATEMENT

- As both Voltage and Cell Size are reduced with each new process node.

- The internal Capacitance is also reduced makes the critical charge needed to upset the logic state of circuit node much smaller , resulting in increase vulnerability of SEE.

- High Energy Cosmic rays and Solar particles react with the upper atmosphere generating high energy proton & neutron that showers to the ground.

- E-H Pair generated by interaction of an energetic charged particle with semiconductor atoms corrupts the stored data in memory cell.

LIMITATION OF SRAM

1): By applying near/ subthreshold voltage in SRAM Designs

- As Supply Voltage ⬇ Delay of SRAM ⬆ at higher rate than CMOS Logic Circuit Delay.
- Low Voltage READ operation lead to destruction of stored data in SRAM bitcells.
- Write Operation suffers from a higher rate of failure at Low Supply Voltages.

2): Due to the possibility of SRAM being affected by SEU.

IS THIS A NEW PROBLEM ?

NO!

In Late 1970's SOFT ERROR problem gained widespread attention when DRAM's circuit began to sign of apparently random failures.

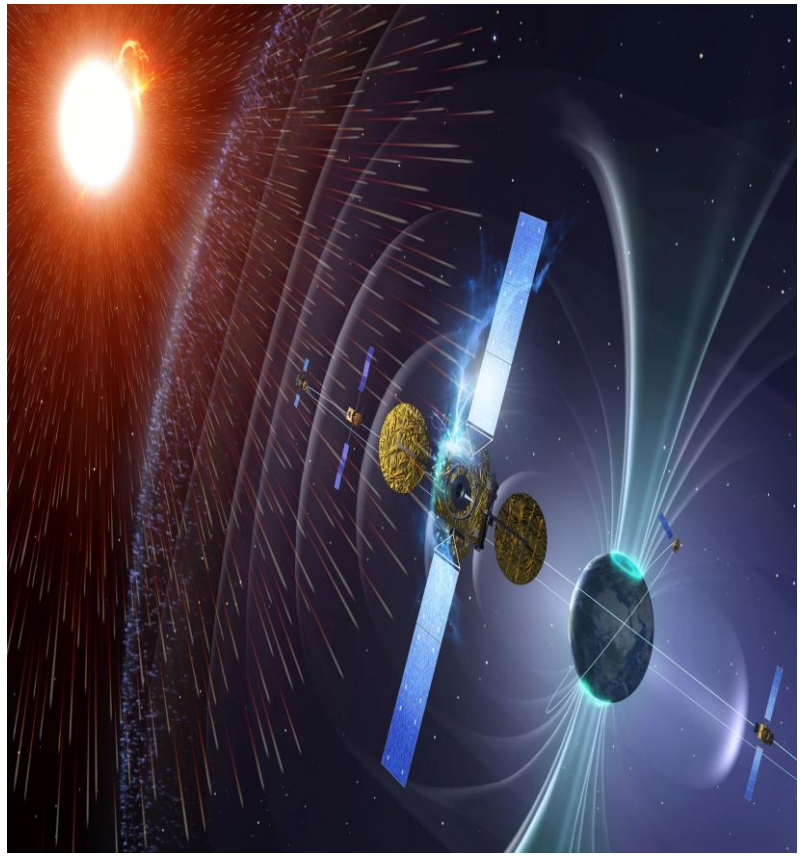
Predictably induce bit flips


FORGET SOFTWARE—NOW HACKERS ARE EXPLOITING PHYSICS

- Unlike DRAM's , SRAM memories and SRAM-based programmable logic devices are also subject to the same effects.
- SRAM's are constructed of cross coupled devices , far less CAPACITANCE in each cell. SRAM cell capacitance continues to decrease, making the cell even more vulnerable to more types of (lower energy) particles.

OVERVIEW

- IBM demonstrated that at an altitude as low as 10,000 feet, SEU effects were already 14 times higher than at sea.
- In 2000, Sun's UltraSPARC II workstations were crashing at an alarming rate.
- The April 2002 (IRPS), held in Dallas, had a special focused session discussing, "Radiation Induced Soft Errors in Silicon Components and Computer Systems.
- This problem will continue to worsen as devices increase in density and geometries continue to shrink. 130 nanometer and smaller SRAM geometries are particularly sensitive to these problems.



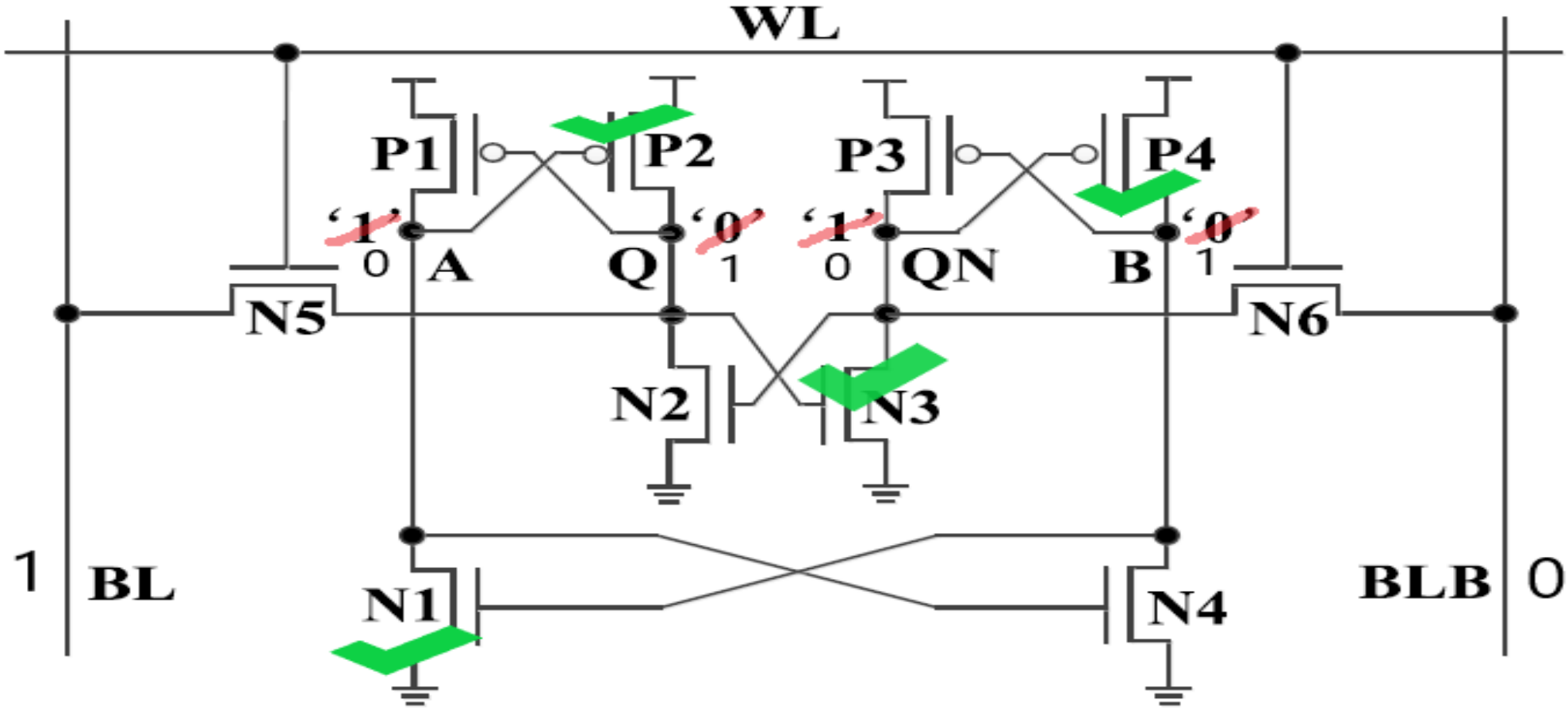
https://www.esa.int/var/esa/storage/images/esa_multimedia/images/2018/11/space_situational_awareness_space_weather/18246476-2-eng-GB/Space_Situational_Awareness_Space_Weather.jpg

PROPOSED DESIGN

- Utilizing two p-type and two n-type latch structures, quadruple cross-coupled storage cells (QUCCE) 10-T and 12-T are proposed.
- QUCCE 10-T and 12-T have better soft error tolerance, time performance, read static noise margins, and hold static noise margins.
- QUCCE 10-T also has lower costs in terms of area and leakage power.
- QUCCE 12-T saves more than 50% the read access time compared with most of the referential cells including the 6T, making it suitable for high speed SRAM designs.

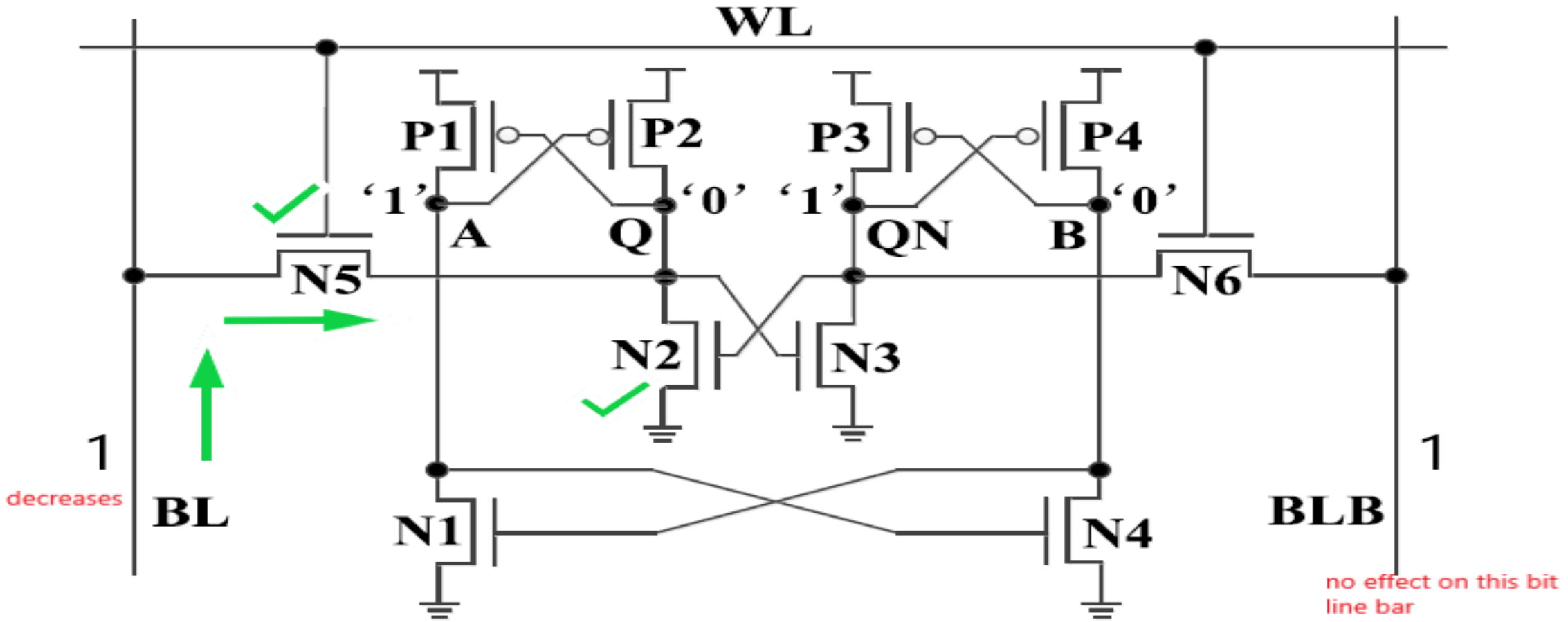
10-T SRAM CELL

WRITE 1



10-T SRAM CELL

READ 0



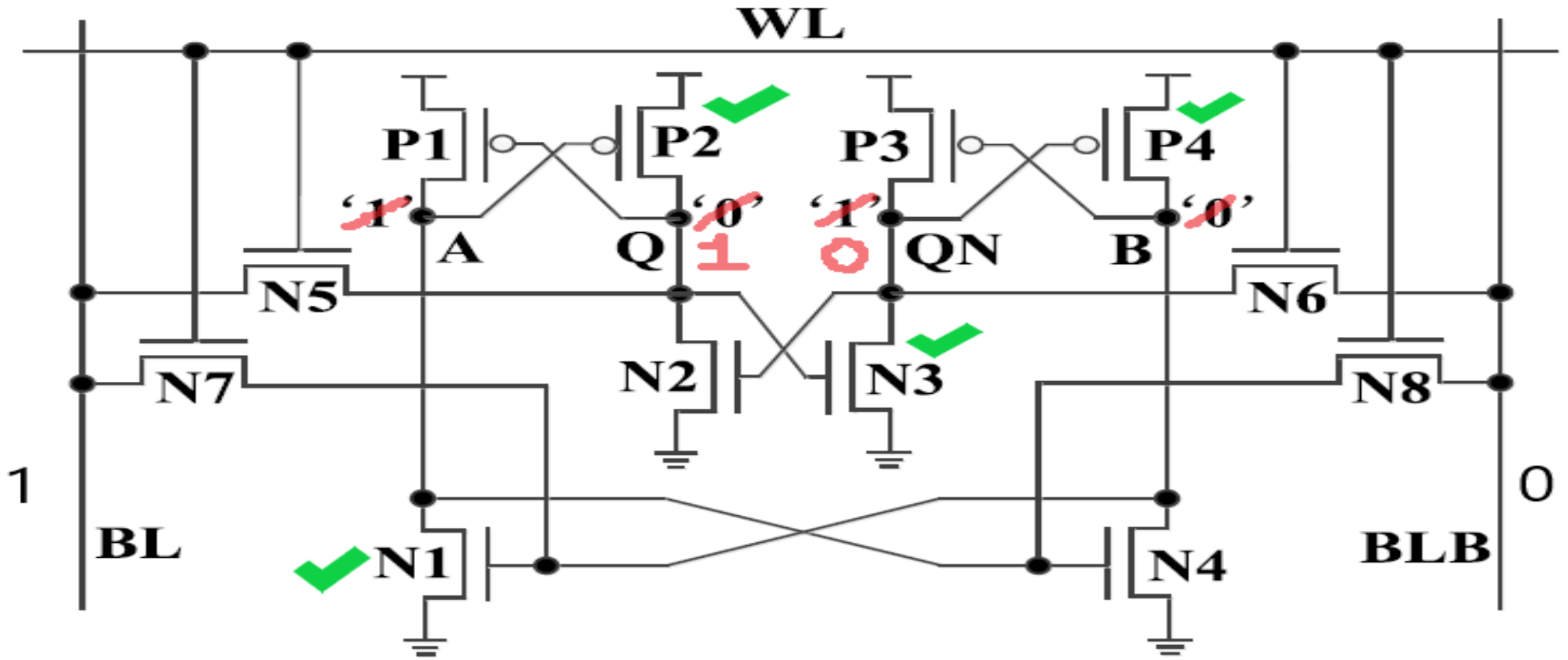
10T-SRAM WIDTH SPECIFICATION

NMOS	Width(nm)	PMOS	Width(nm)
N1	120	P1	265
N2	250	P2	140
N3	250	P3	140
N4	120	P4	265
N5	140		
N6	140		

- CR, the cell ratio defined as (WN2/LN2)/(WN5/LN5) or (WN3/LN3)/(WN6/LN6) for read stability, is set to be 1.8.
- PR1, defined as (WP2/LP2)/(WN5/LN5) or (WP3/LP3)/(WN6/LN6) for write-ability, is set to be 1
- PR2, defined as (WP4/LP4)/(WN4/LN4) or (WP1/LP1)/(WN1/LN1), is set to be 2.2.

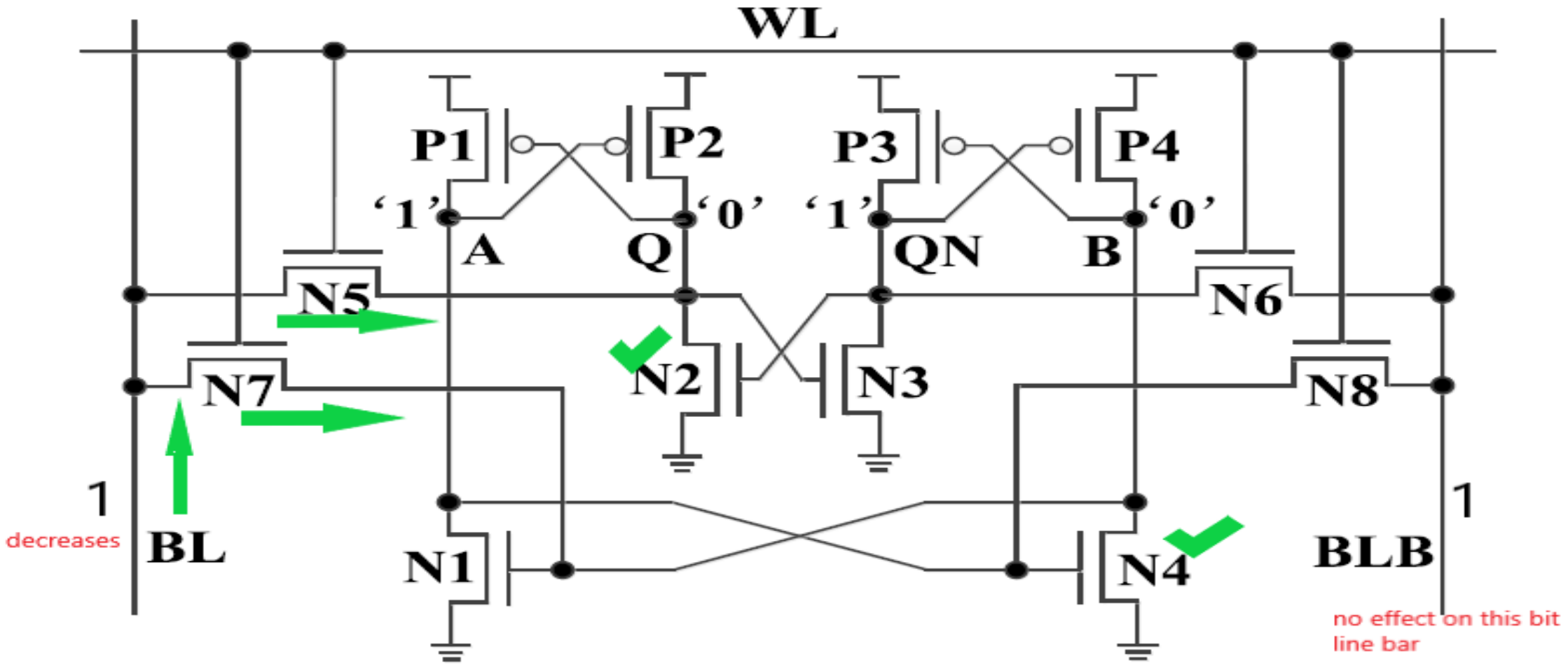
Schematic of QUCCE 12T

WRITE-1



Schematic of QUCCE 12T

READ-0



12T-SRAM WIDTH SPECIFICATION

NMOS	Width(nm)	PMOS	Width(nm)
N1	510	P1	280
N2	510	P2	280
N3	510	P3	280
N4	510	P4	280
N5	280		
N6	280		
N7	280		
N8	280		

- CR, defined as (WN2/LN2)/(WN5/LN5), (WN4/LN4)/(WN7/LN7), (WN3/LN3)/(WN6/LN6), or (WN1/ LN1)/(WN8/LN8) for read stability, is set to be 1.8.
- PR, defined as (WP3/LP3)/(WN6/LN6), (WP1/LP1)/(WN8/LN8), (WP2/LP2)/(WN5/LN5), or (WP4/LP4)/(WN7/LN7) for write ability, is set to be 1.

SET(SINGLE EVENT TRANSIENT)

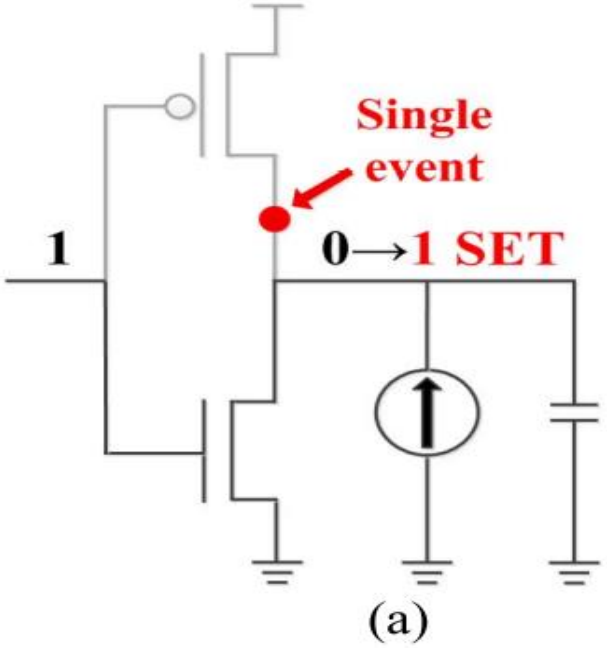
- Single Event Transients (SETs) are caused by a single energetic particle.
- If a SET propagates through digital circuitry and results in an incorrect value being latched in a sequential logic unit, it is then considered an SEU.

Condition for SET to occur:

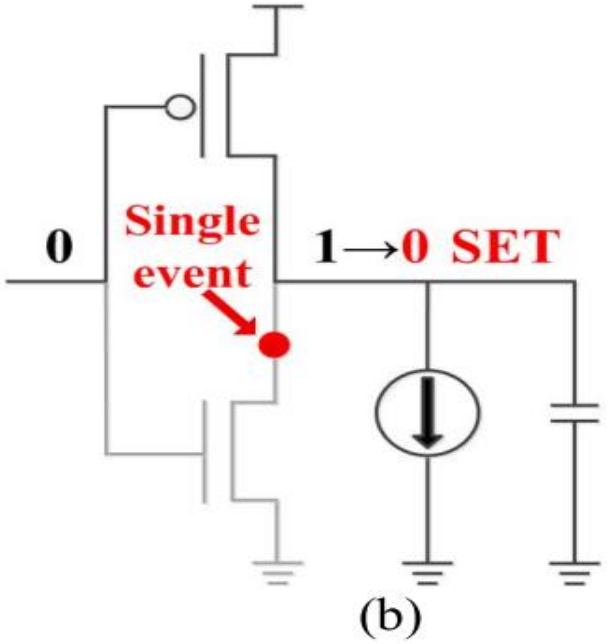
- An energetic particle strikes drain terminal of MOSFET.
- The MOSFET should be OFF.
- The MOSFET should be in reverse biased (reverse biased junctions collect charge due to the influence of the electric potential gradient).

MODELLING SINGLE EVENT TRANSIENT

We have to inject transient fault through double exponential current source as described in literatures

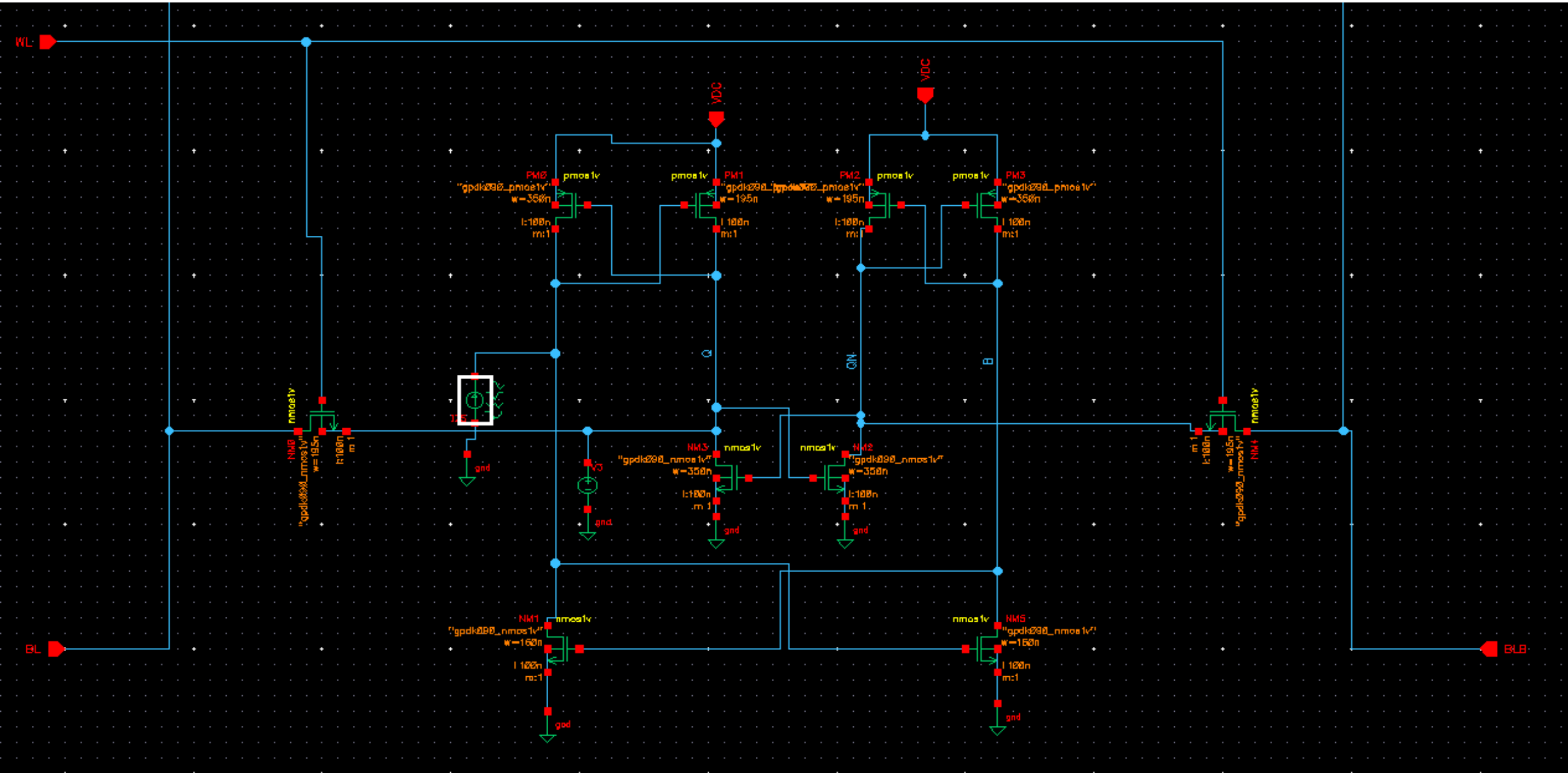


(a) generation of a positive transient pulse

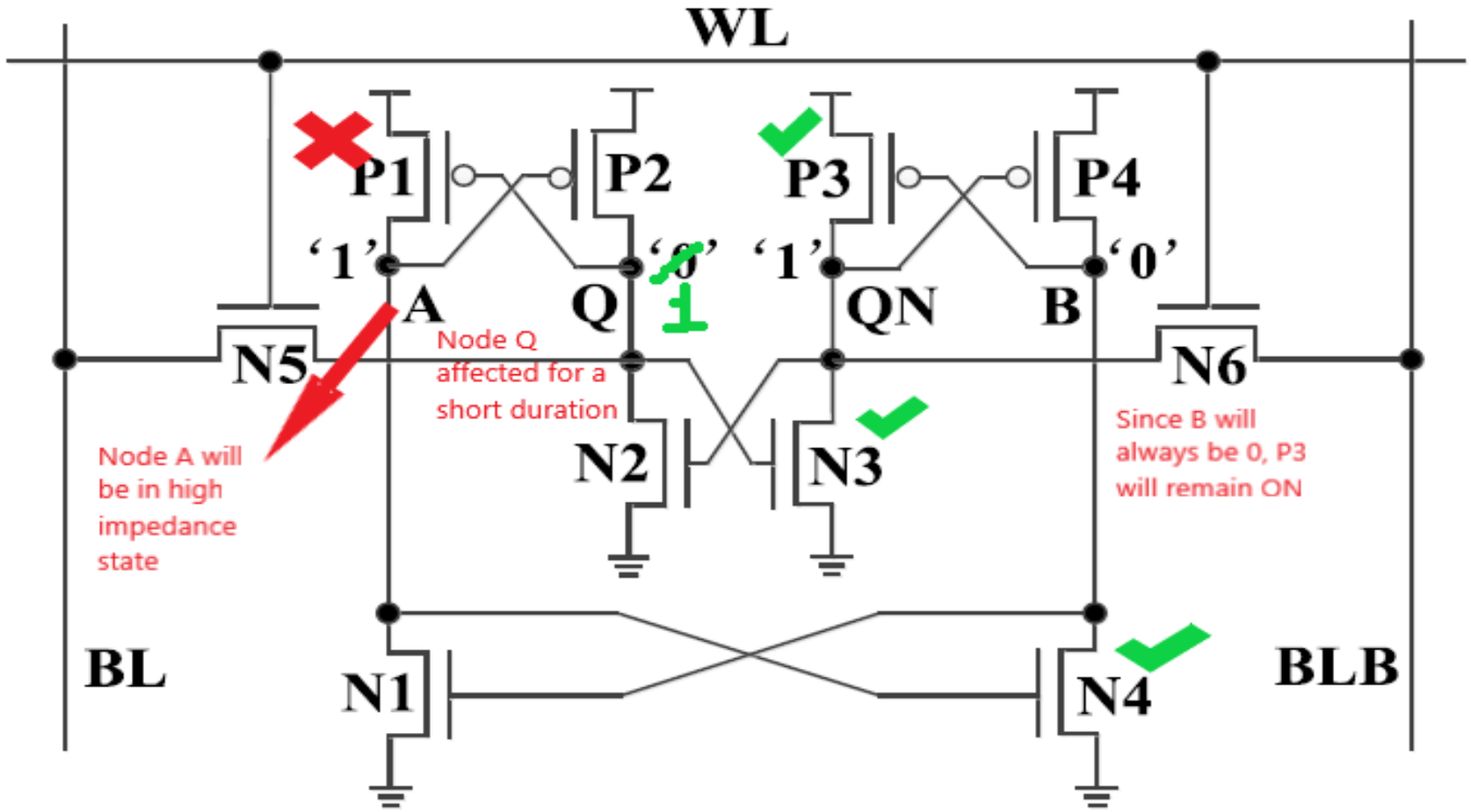


(b) generation of a negative transient pulse

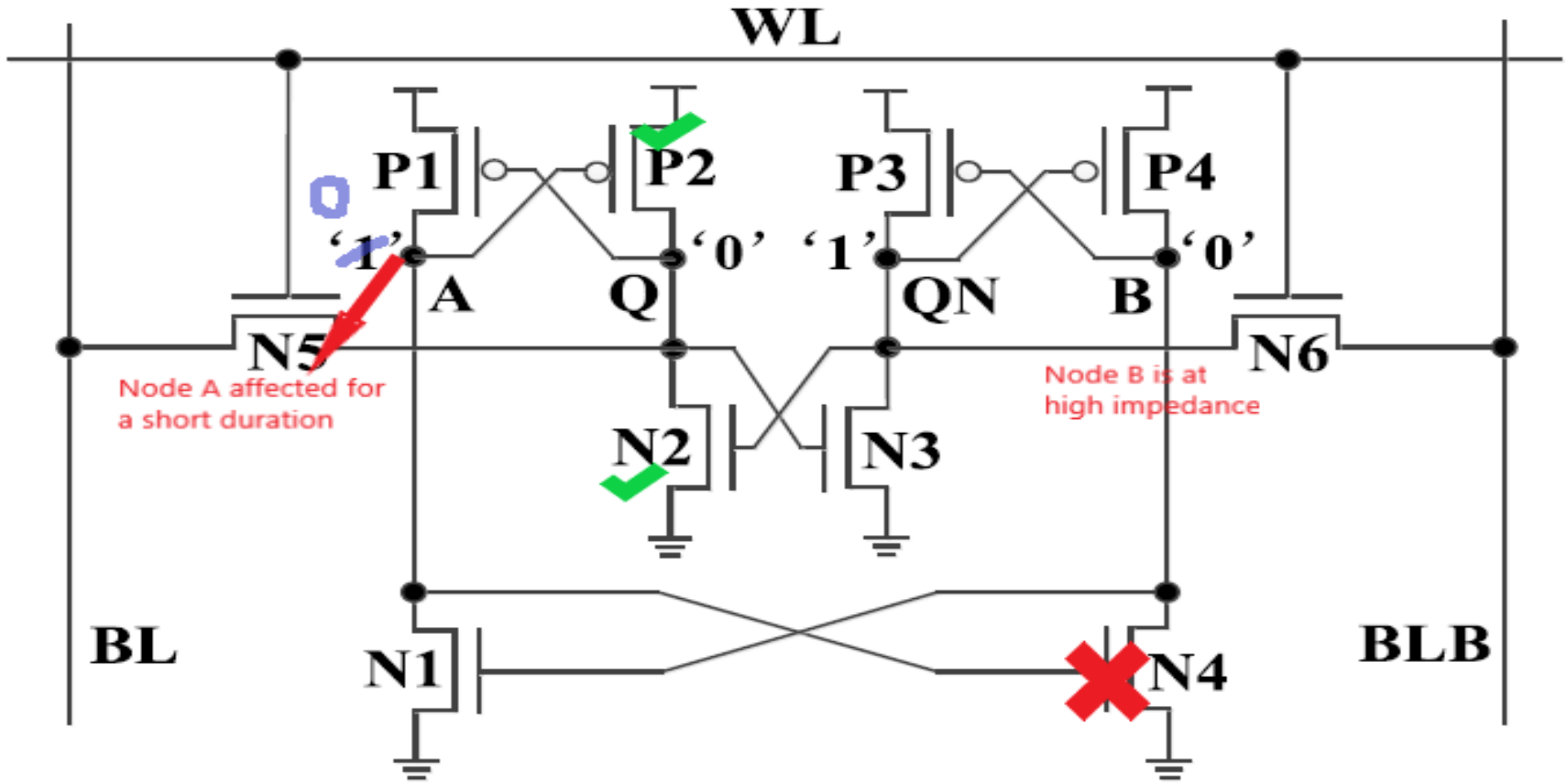
SCHEMATIC WITH SEU



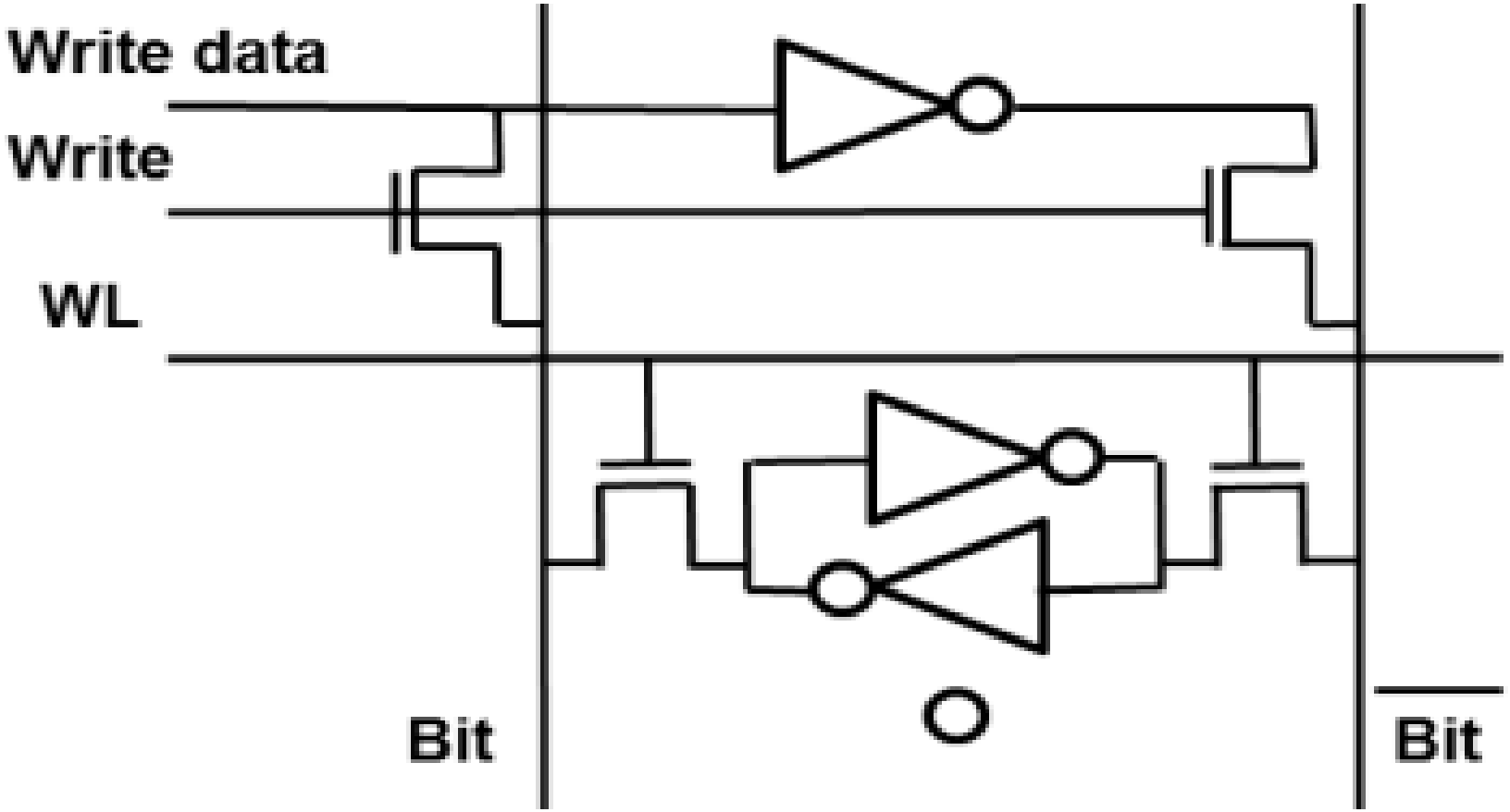
10-T (SEU AT Q)


WL
P1
P2
P3
P4
'1'
'0'
'1'
'0'
A
Q
QN
B
N5
N6
Node Q affected for a short duration
Node A will be in high impedance state
Since B will always be 0, P3 will remain ON
N2
N3
BL
N1
N4
BLB

10-T (SEU AT A)

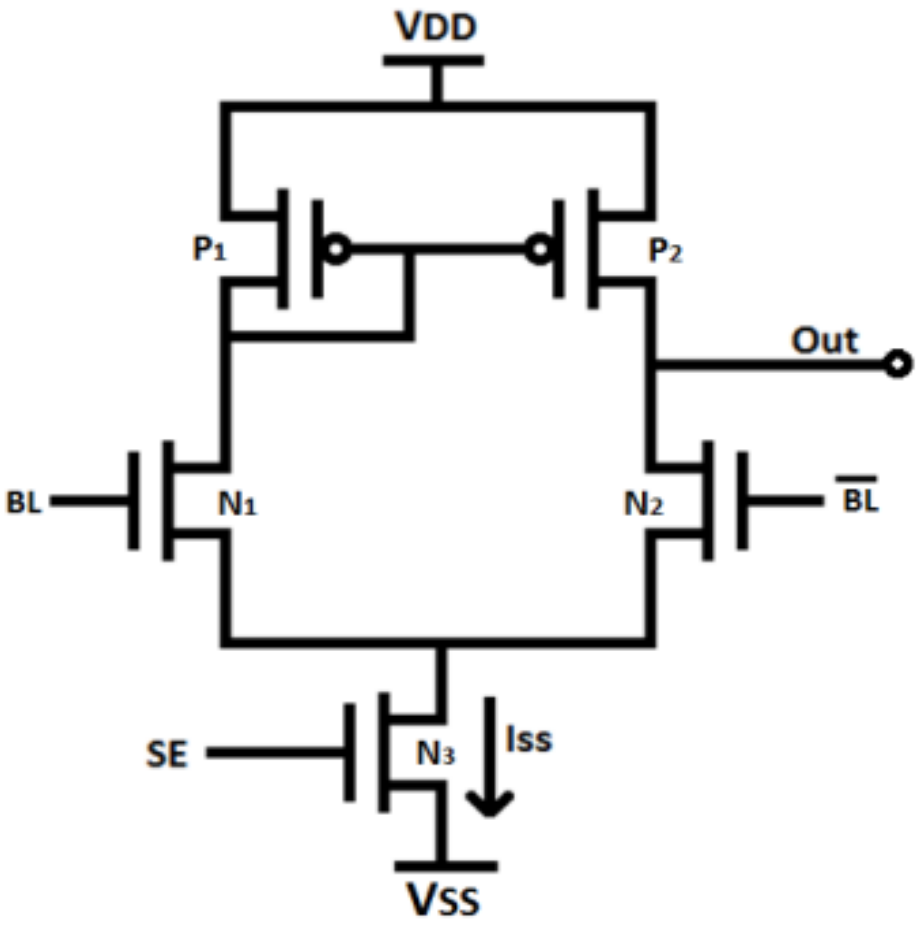

WL
P1
P2
P3
P4
'1'
'0'
'1'
'0'
A
Q
QN
B
N5
N6
Node A affected for
a short duration
Node B is at
high impedance
N2
N3
BL
N1
N4
BLB

Write Circuitry

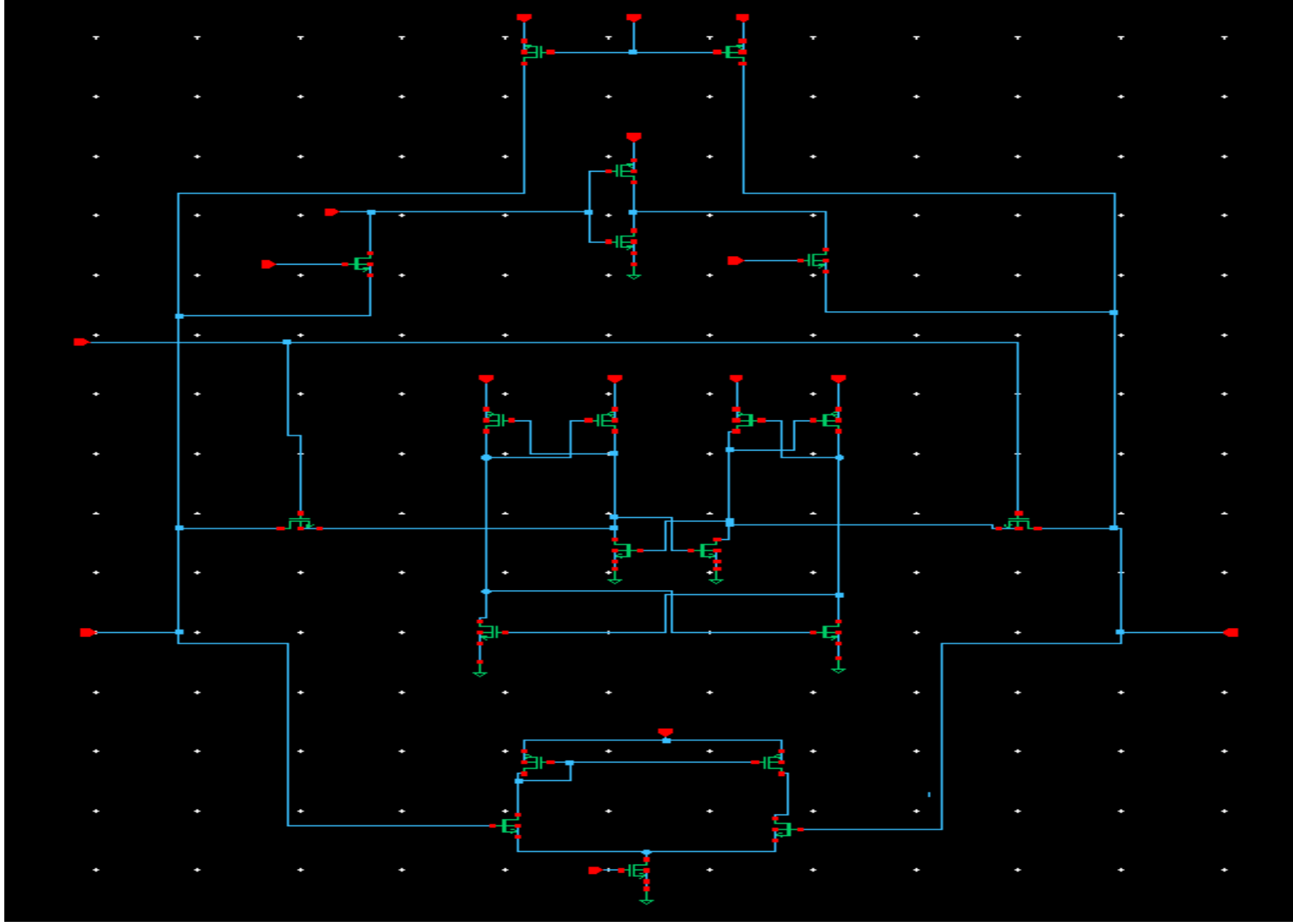


Sense Amplifier Design

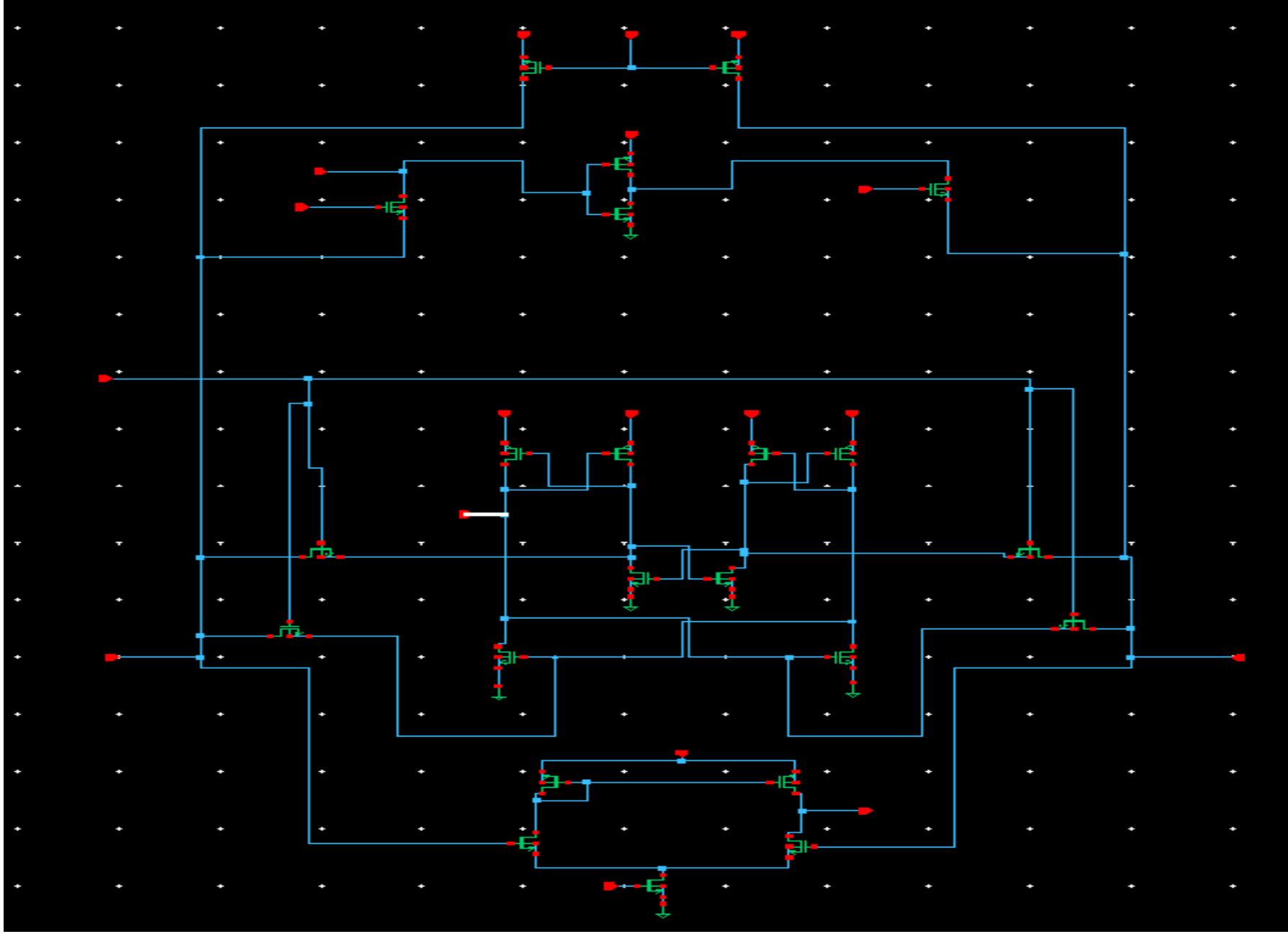
- The sense amplifier may be enabled at the same time as the wordline during a read cycle, making timing requirements for this amplifier very easy.
- The differential amplifier is resistant to supply noise variations due to its ability to reject common mode voltages; only differences between the inputs are amplified.
- Any noise that appears on both inputs of the amplifier will not affect the output.



10-T FULL CIRCUITARY



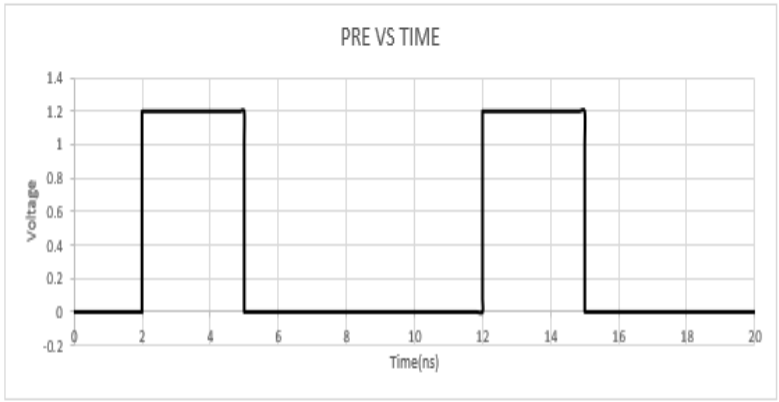
12-T FULL CIRCUITARY

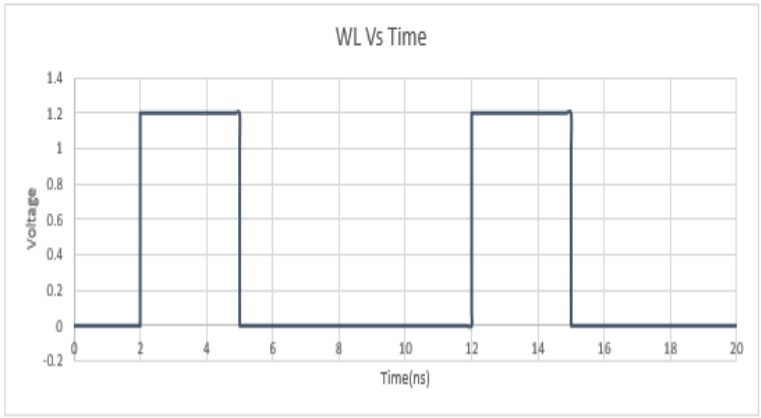


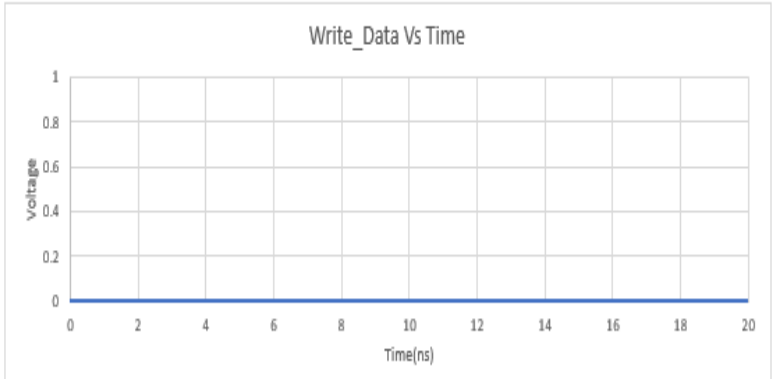
RESULTS

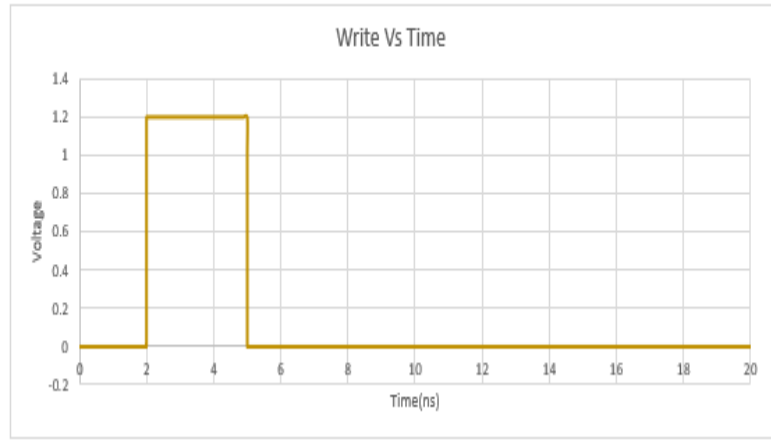
SIMULATION RESULTS OF QUCCE 10T:

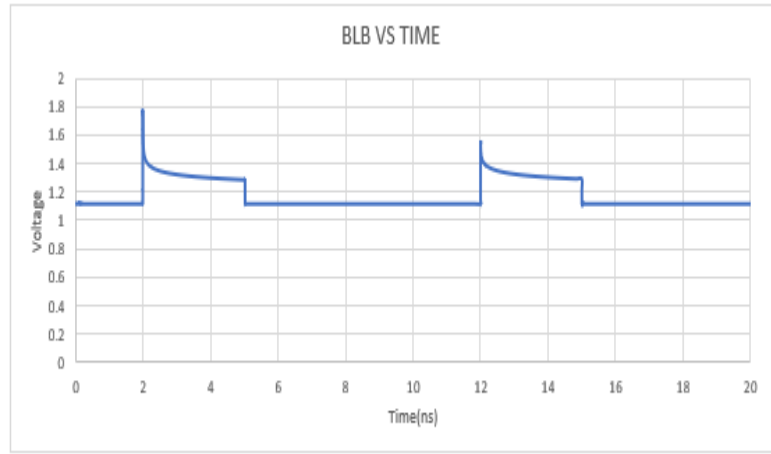
WRITE and READ 0 operation:

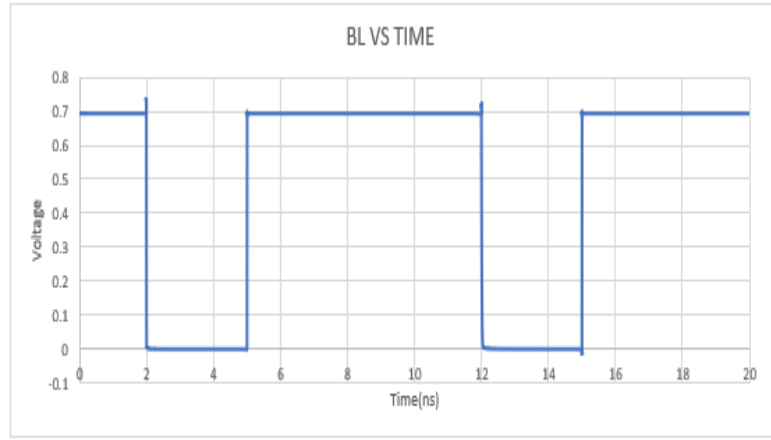


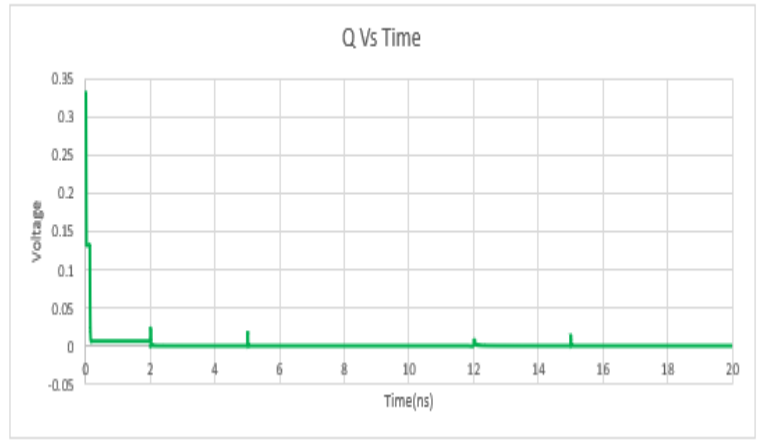


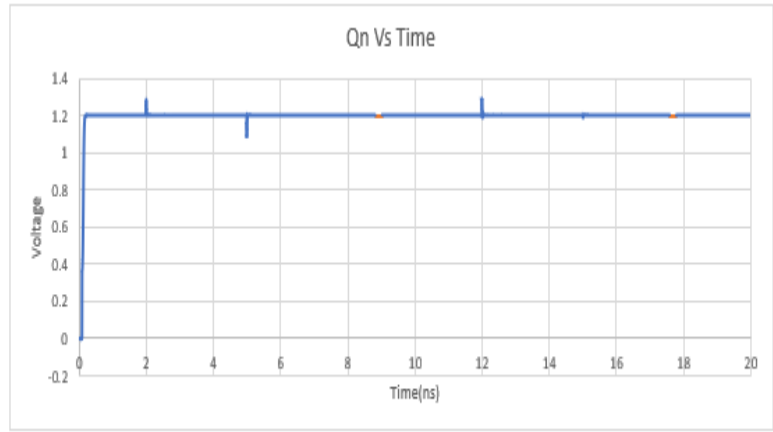


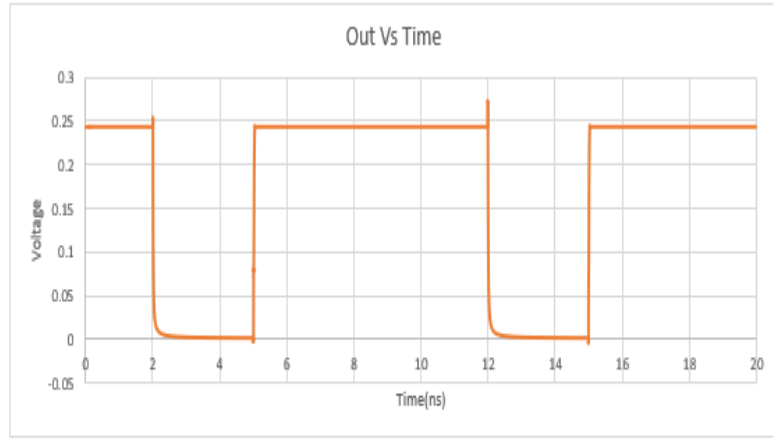




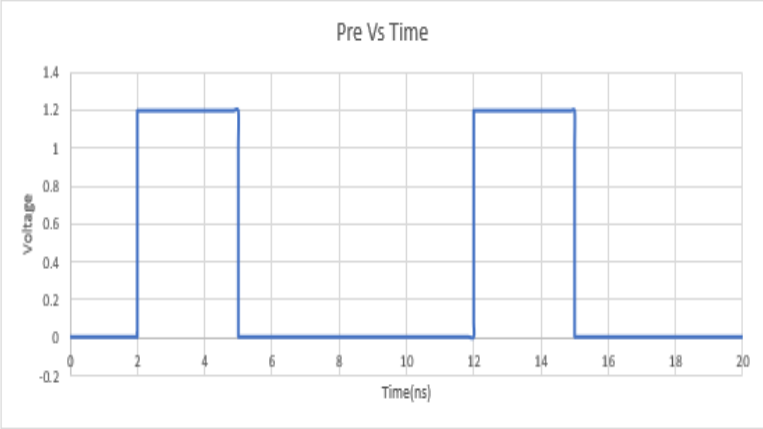


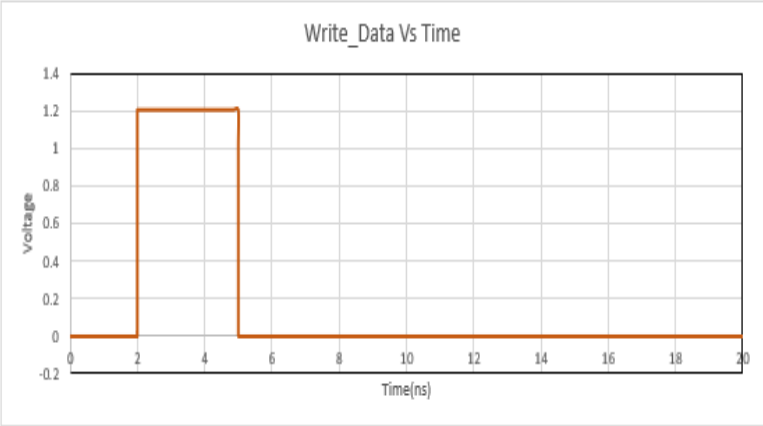


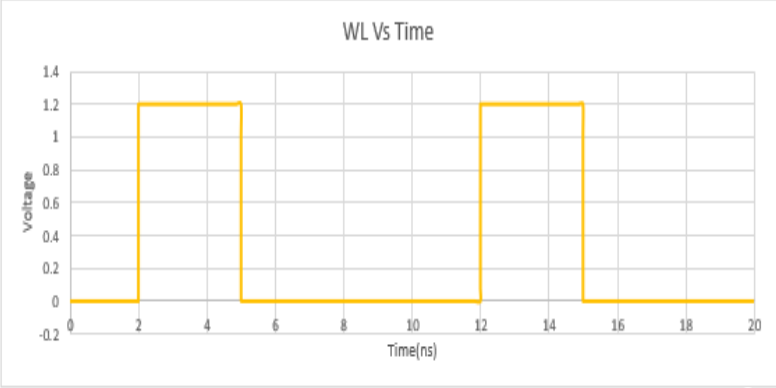


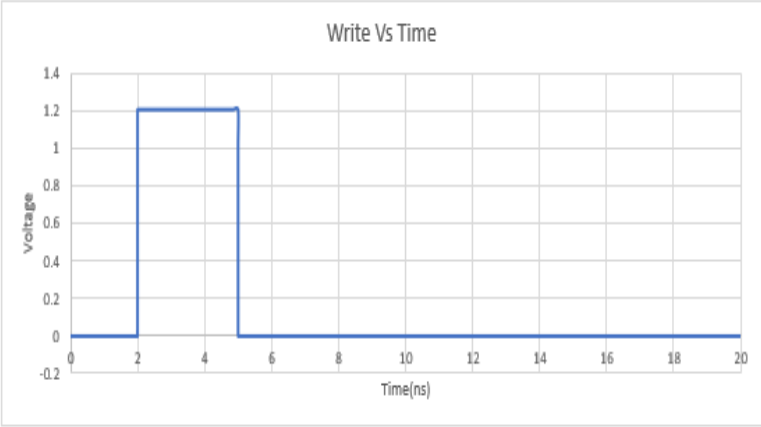


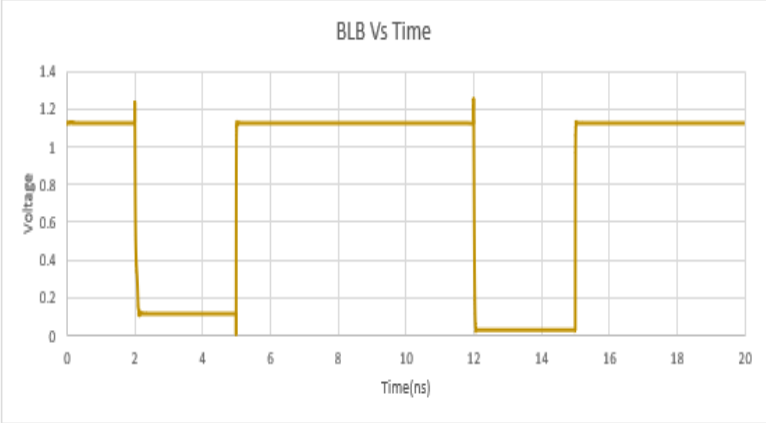
WRITE and READ 1 operation:

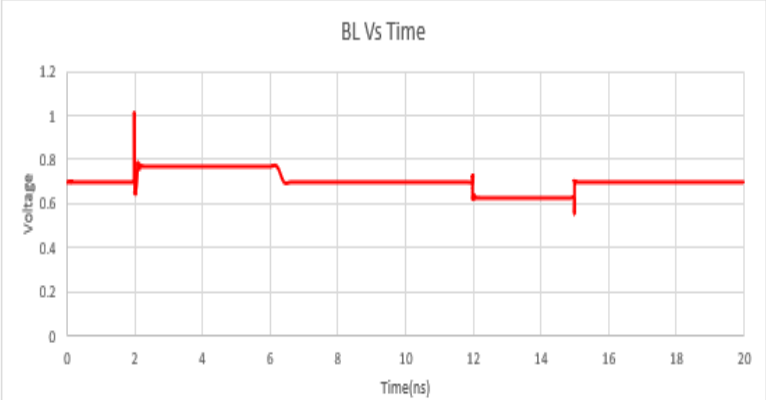


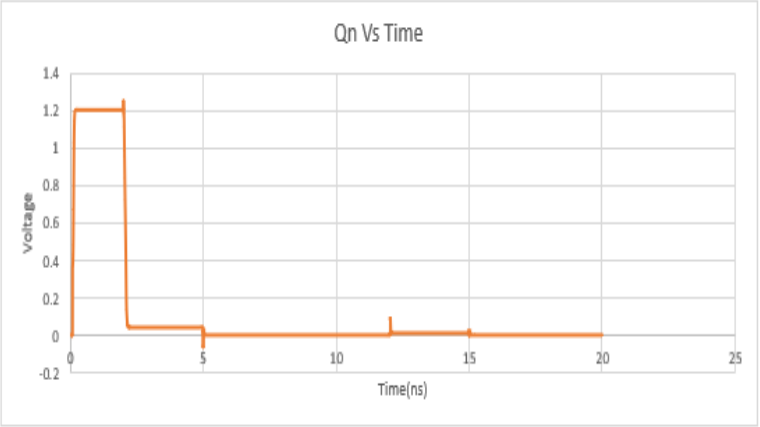


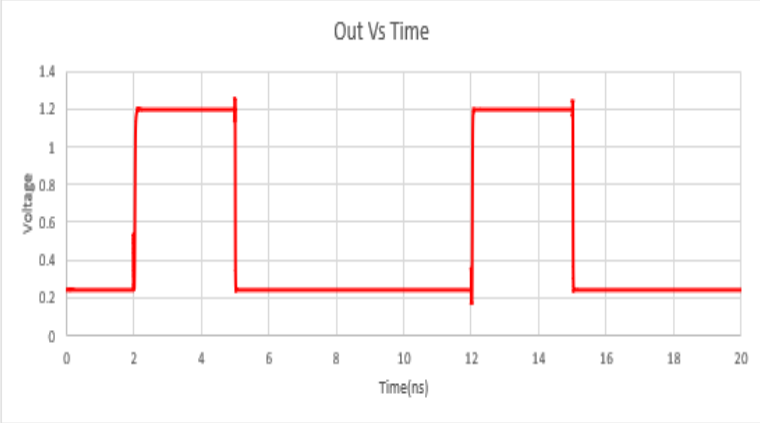




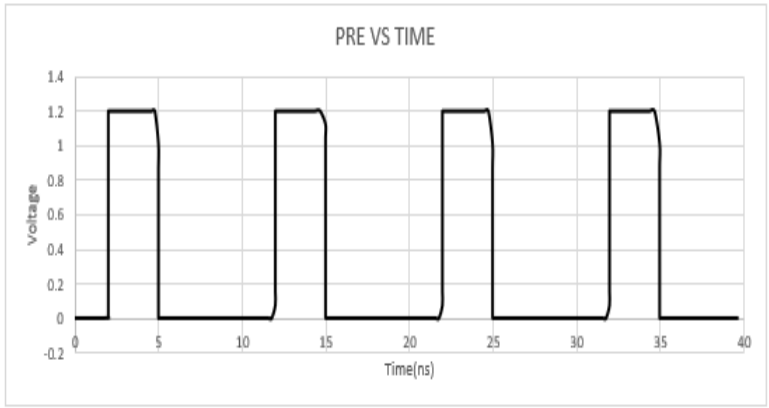


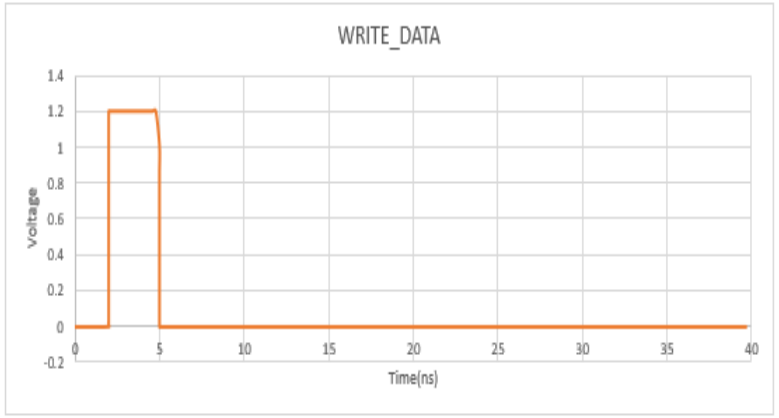


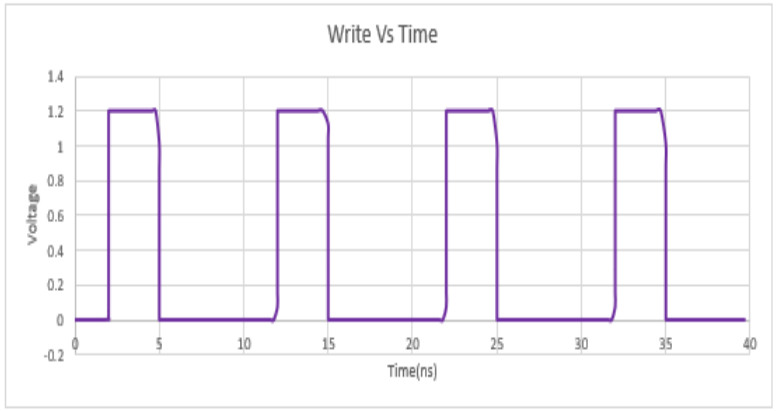


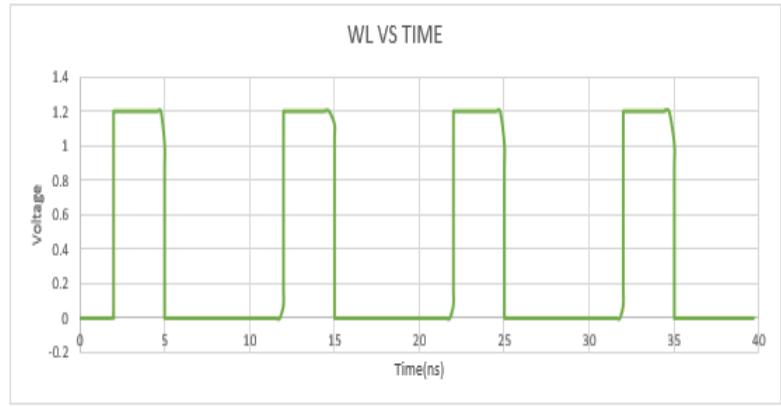


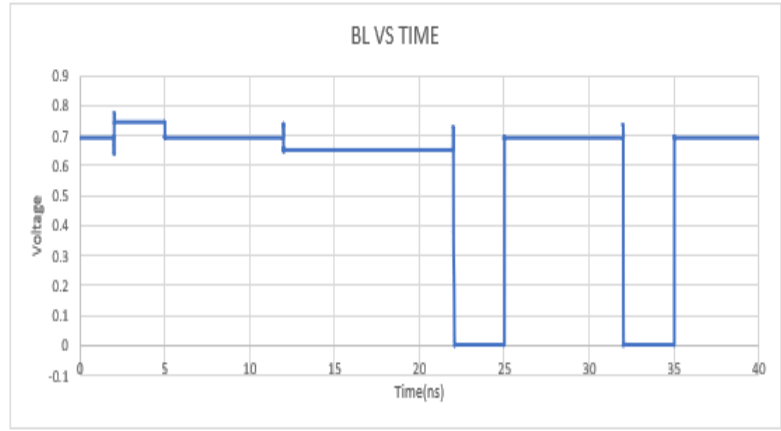
SIMULATION RESULTS OF QUCCE 12T:

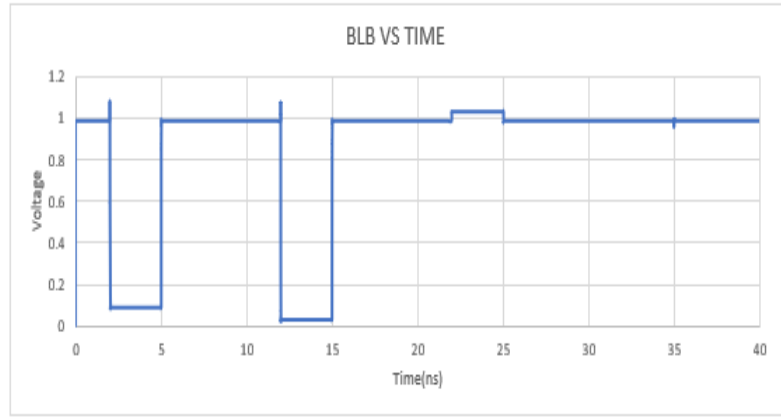


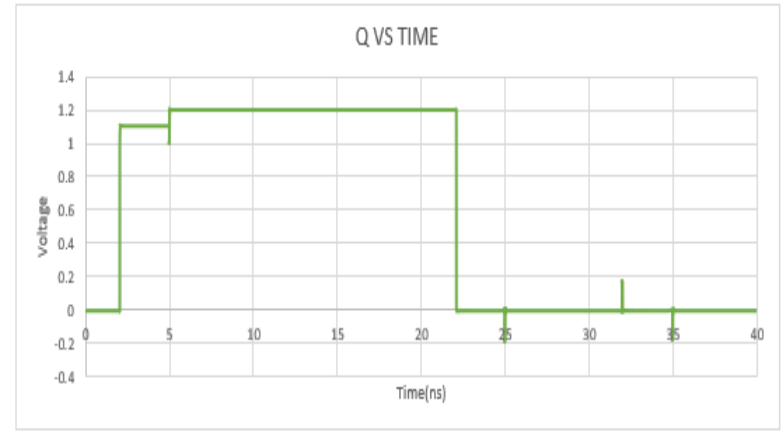


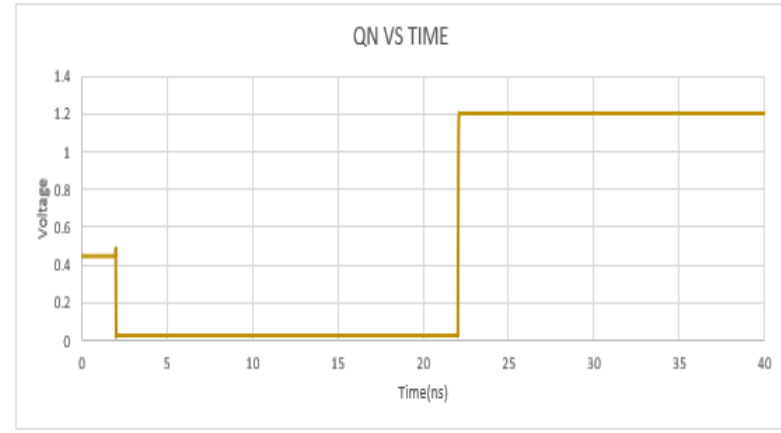


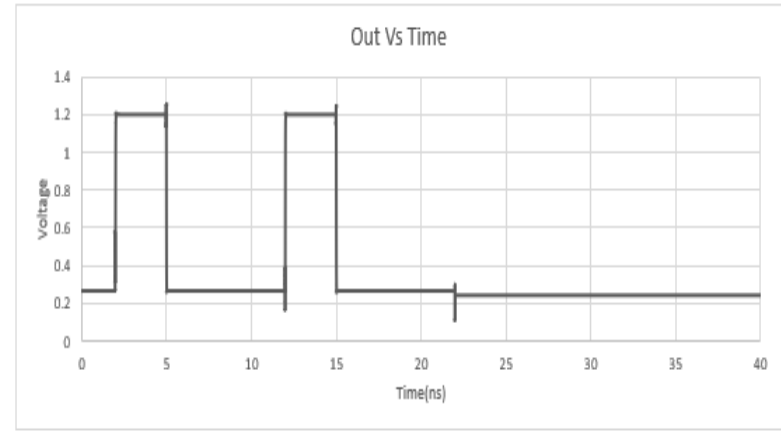






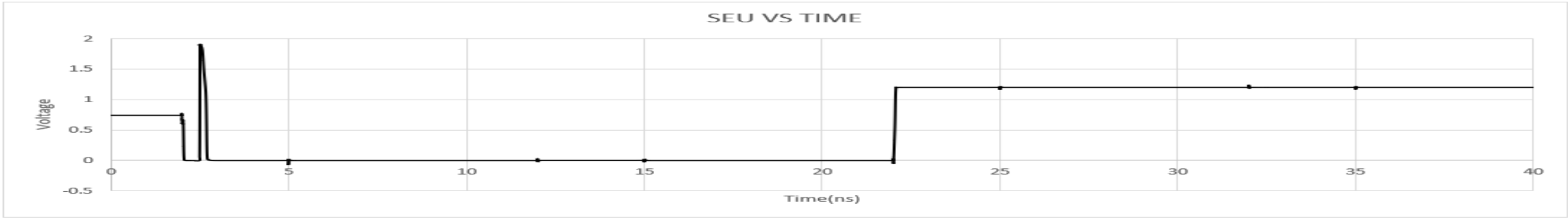


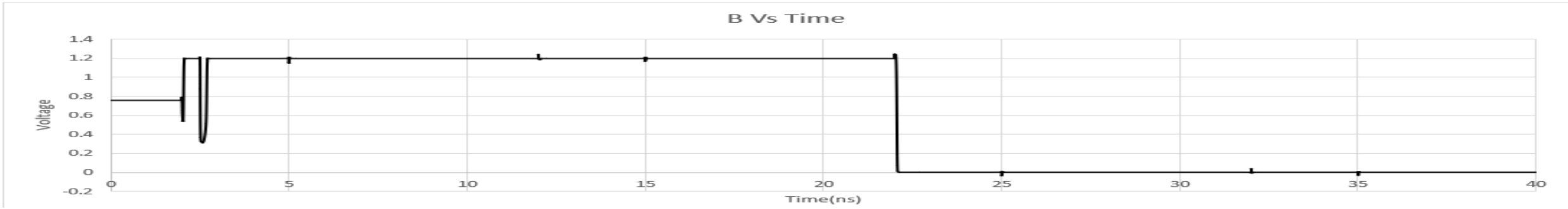


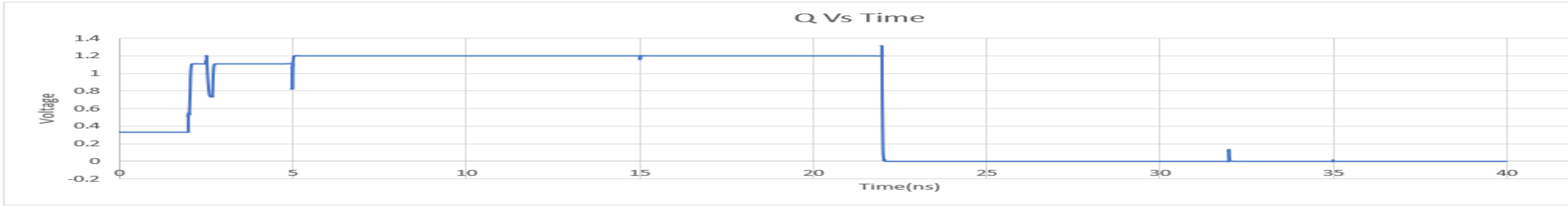


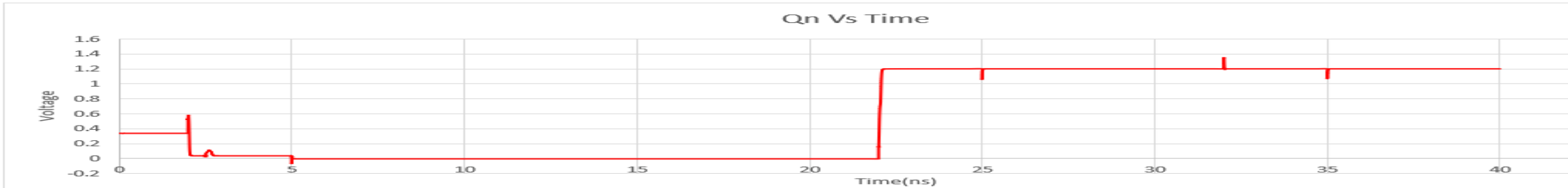
SEU RECOVERY ANALYSIS:

SEU on A:

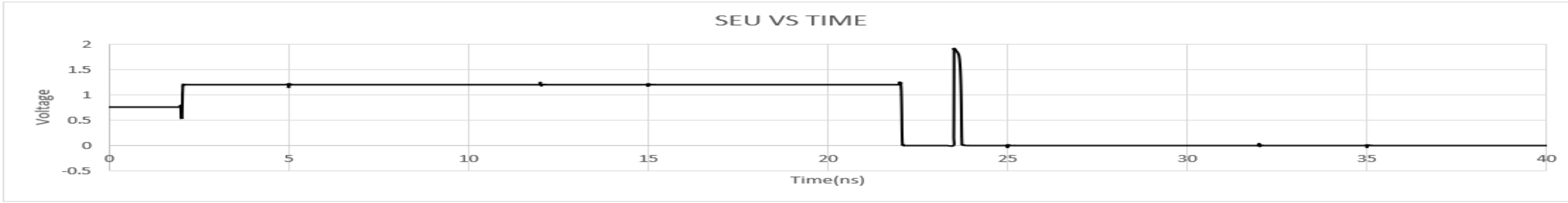


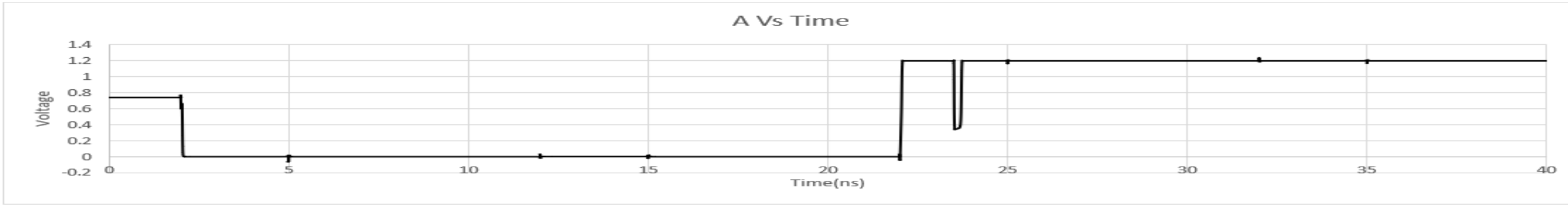


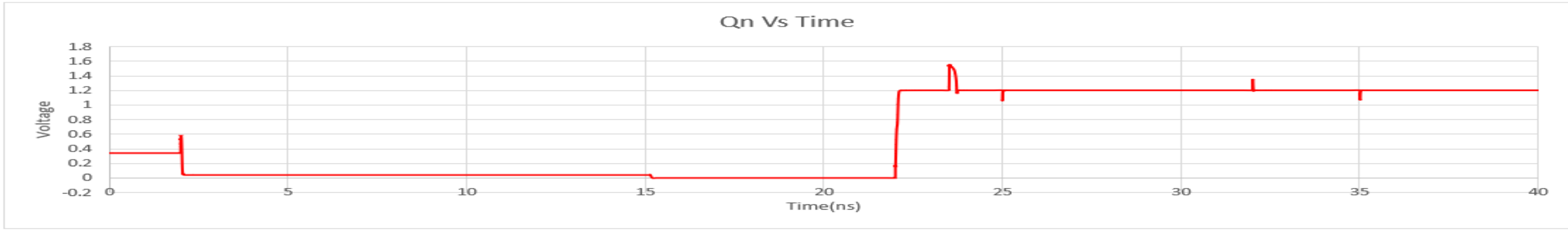


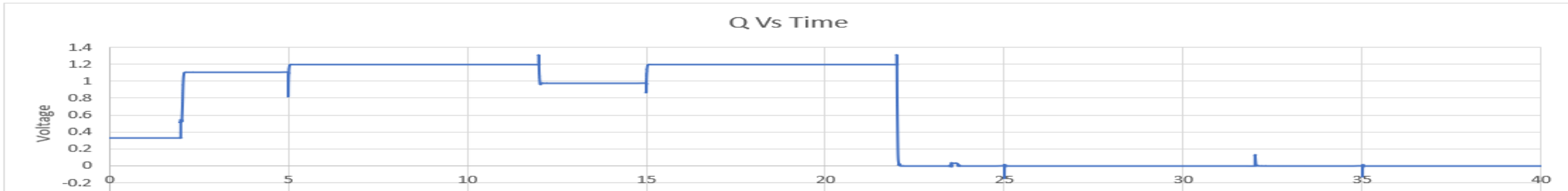


SEU on B:

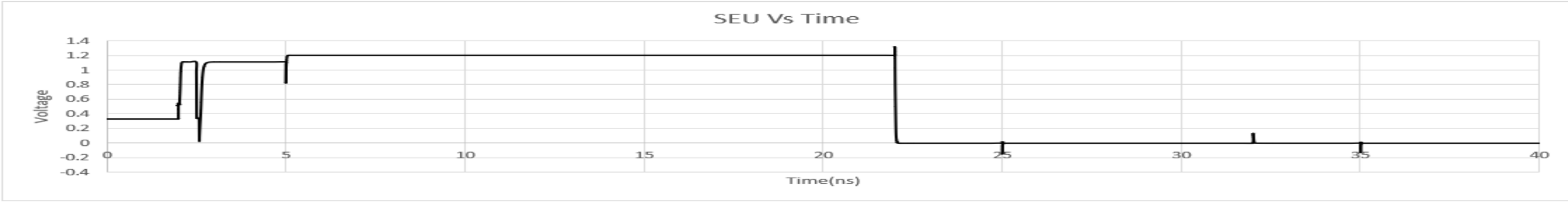

SEU VS TIME
Voltage
2
1.5
1
0.5
0
-0.5
0
5
10
15
20
25
30
35
40
Time(ns)

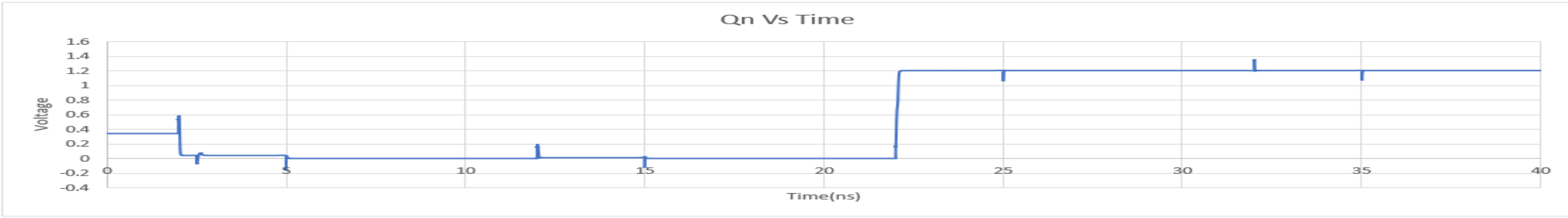

A Vs Time
Voltage
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
5
10
15
20
25
30
35
40
Time(ns)

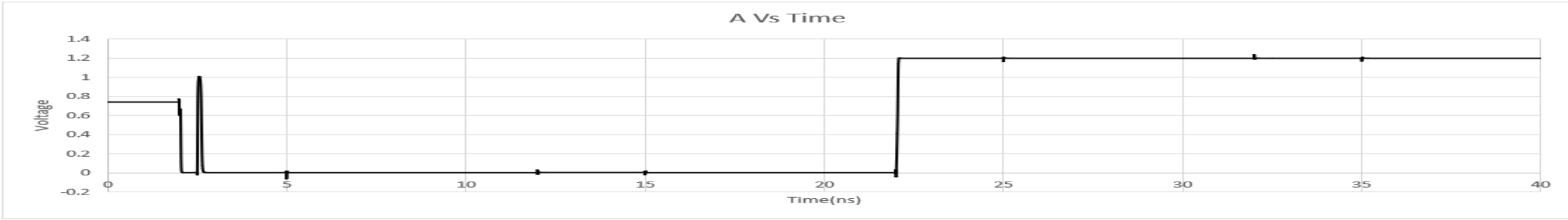

Qn Vs Time
Voltage
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
5
10
15
20
25
30
35
40
Time(ns)

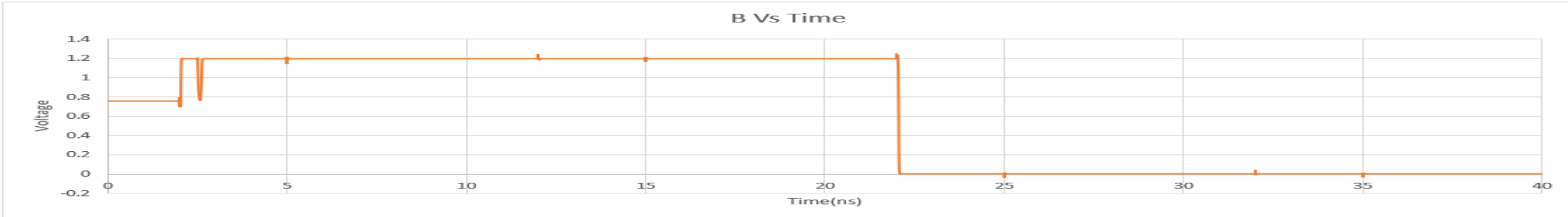

Q Vs Time
Voltage
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
5
10
15
20
25
30
35
40

SEU on Q:

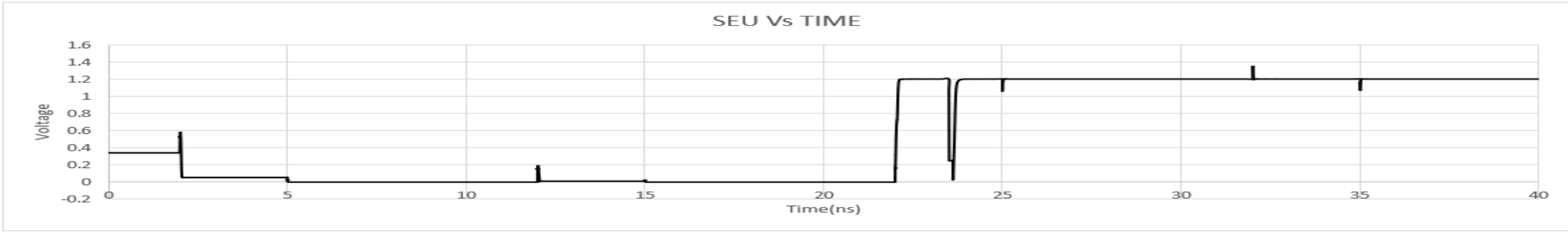

SEU Vs Time
Voltage
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
0
5
10
15
20
25
30
35
40
Time(ns)

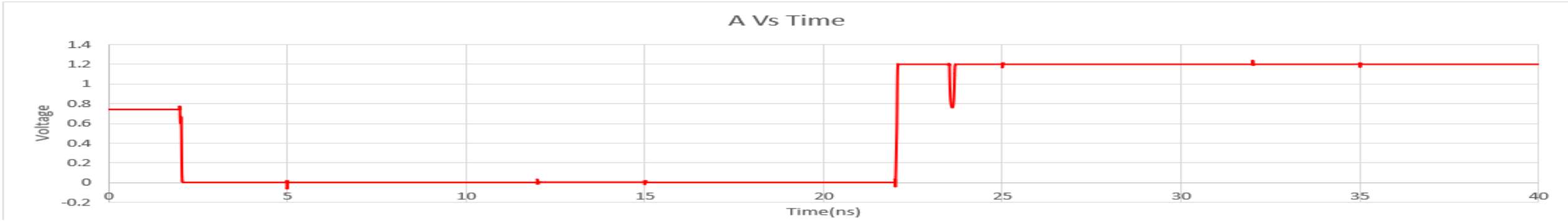

Qn Vs Time
Voltage
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
0
5
10
15
20
25
30
35
40
Time(ns)

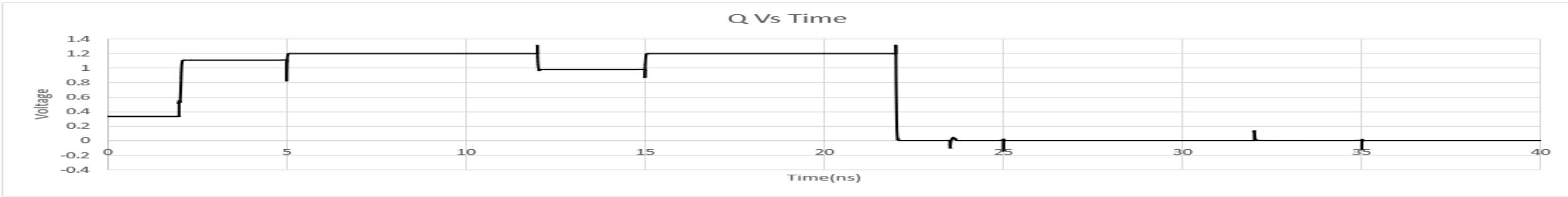

A Vs Time
Voltage
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
5
10
15
20
25
30
35
40
Time(ns)

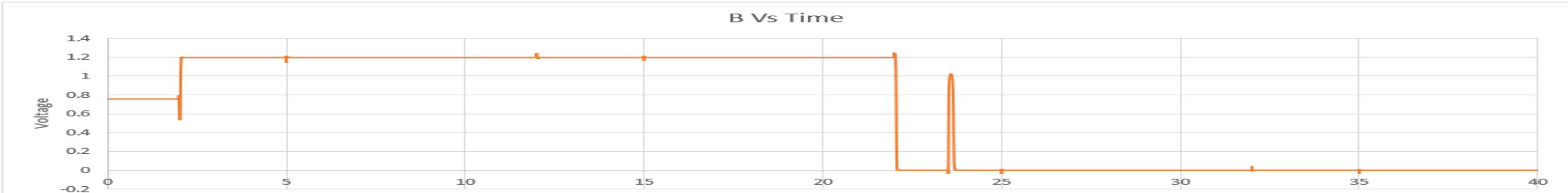

B Vs Time
Voltage
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
5
10
15
20
25
30
35
40
Time(ns)

SEU on QN:

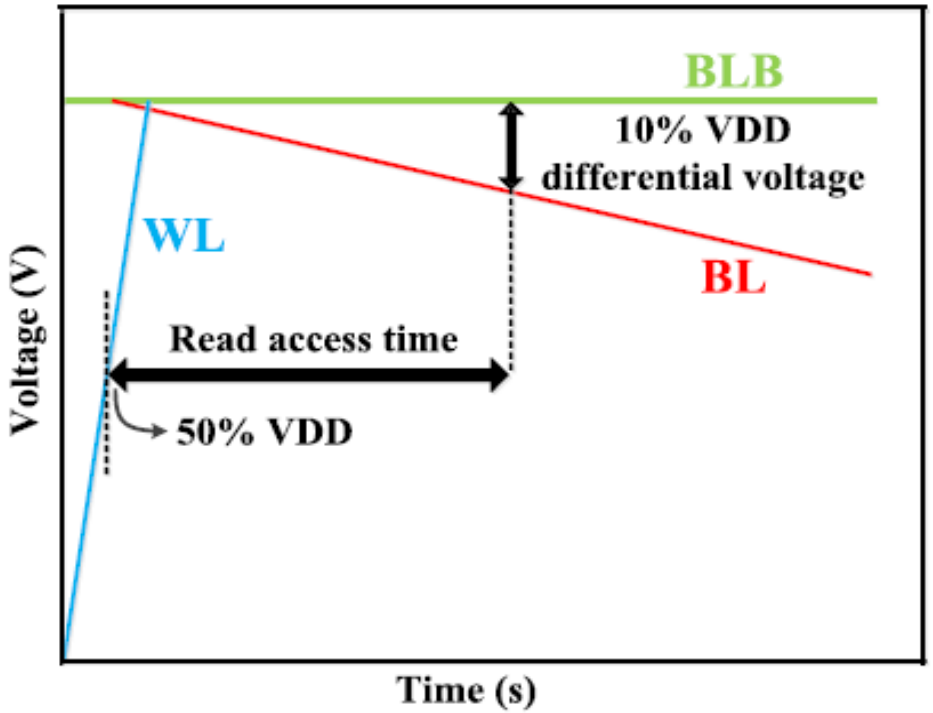

SEU Vs TIME
Voltage
Time(ns)

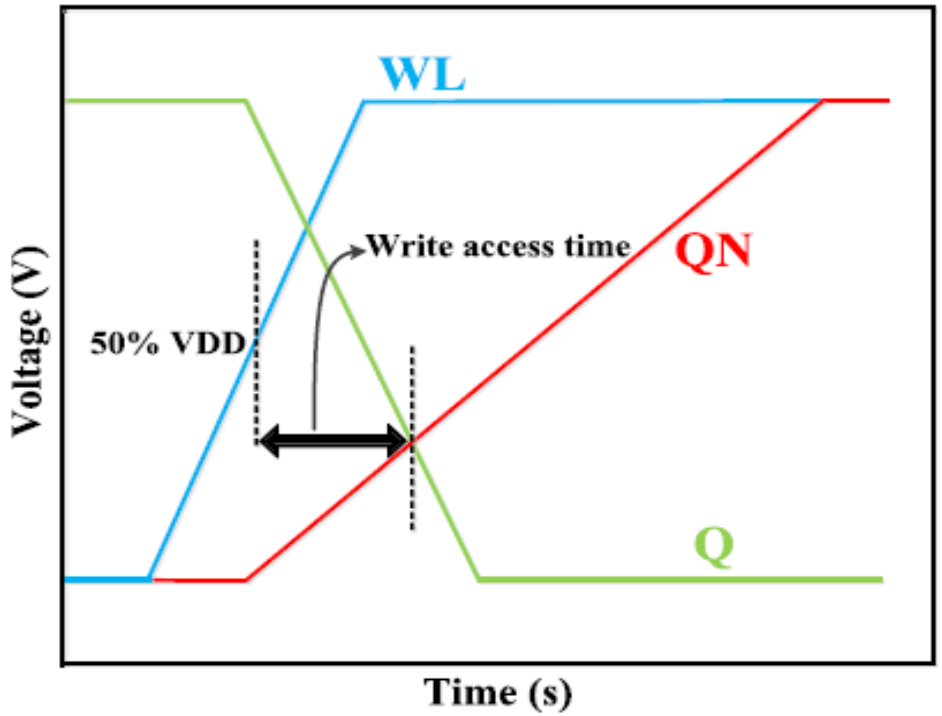

A Vs Time
Voltage
Time(ns)


Q Vs Time
Voltage
Time(ns)

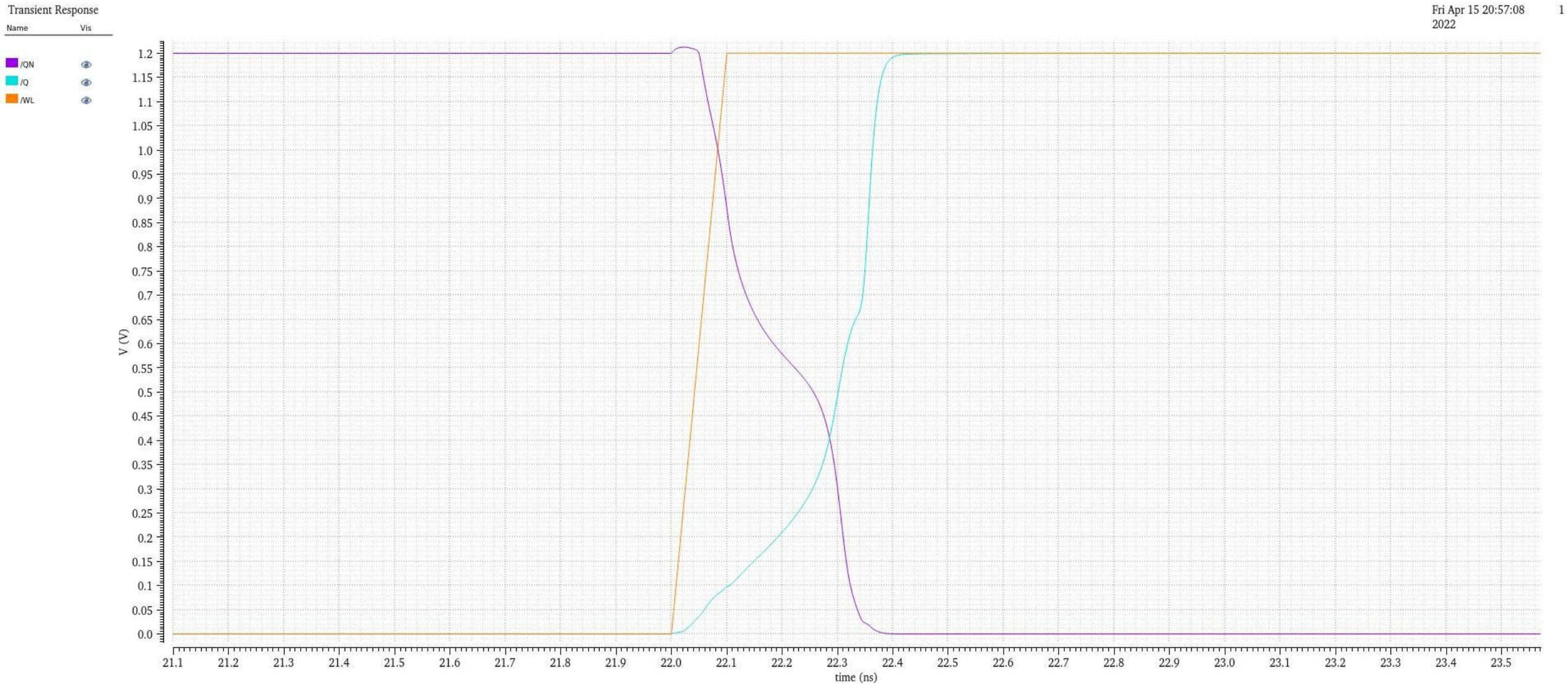

B Vs Time
Voltage

READ & WRITE ACCESS TIME

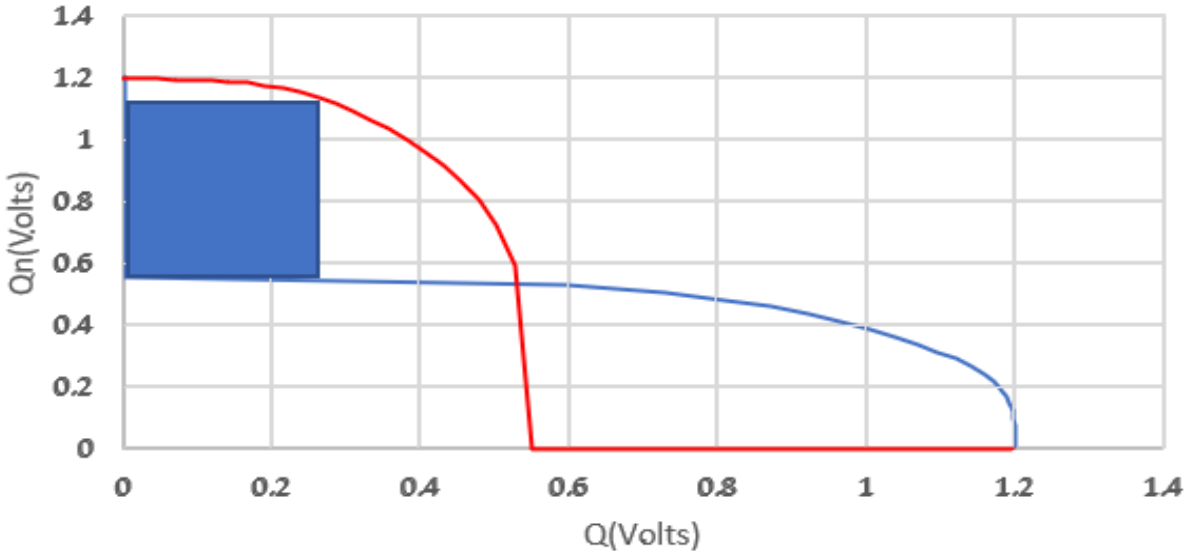




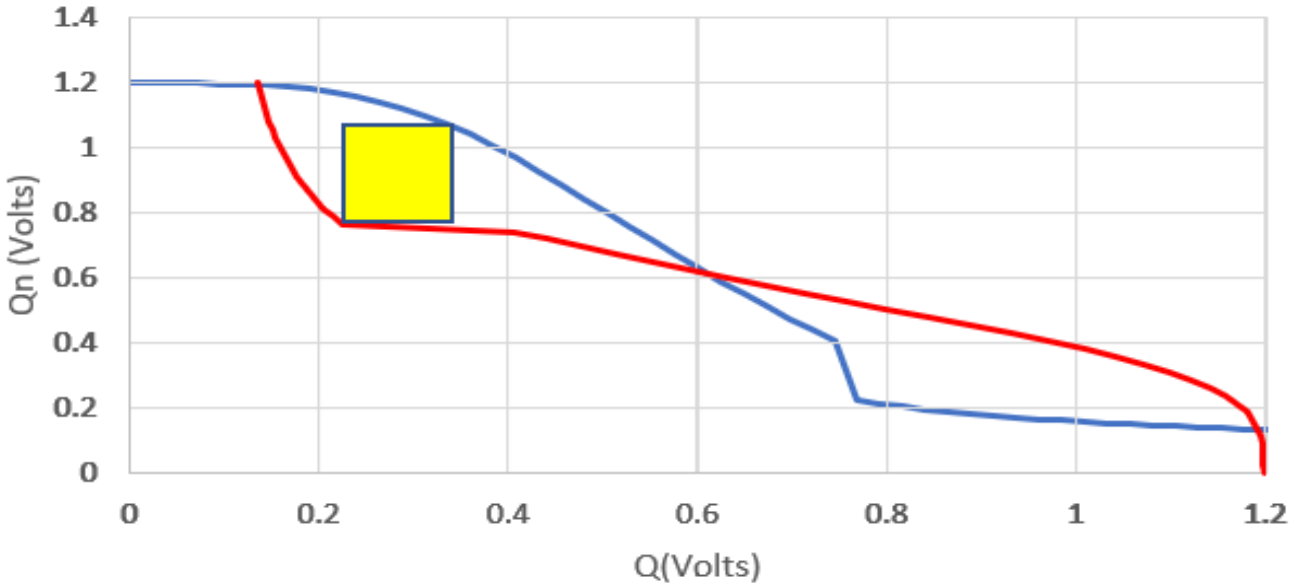
WRITE ACCESS TIME

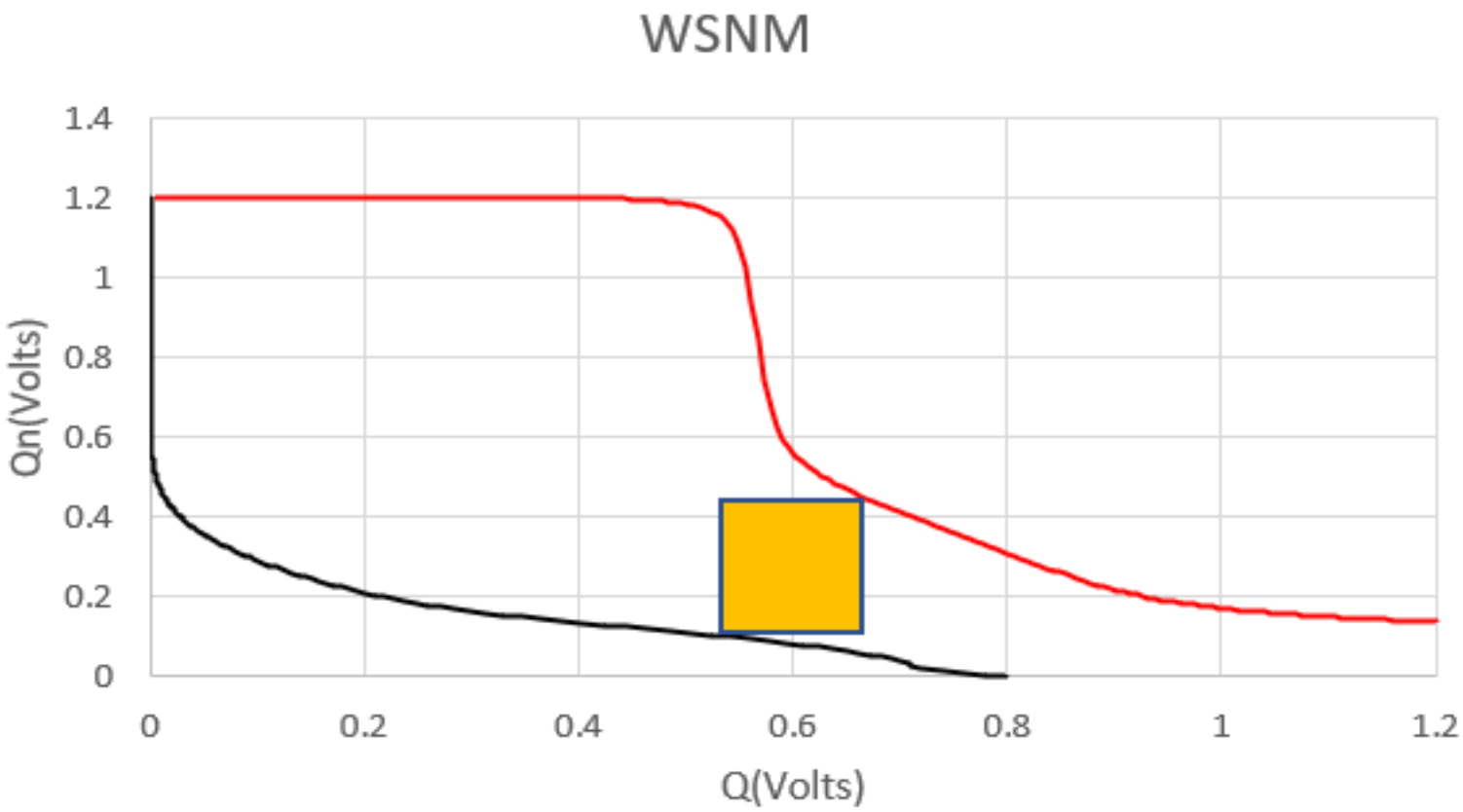


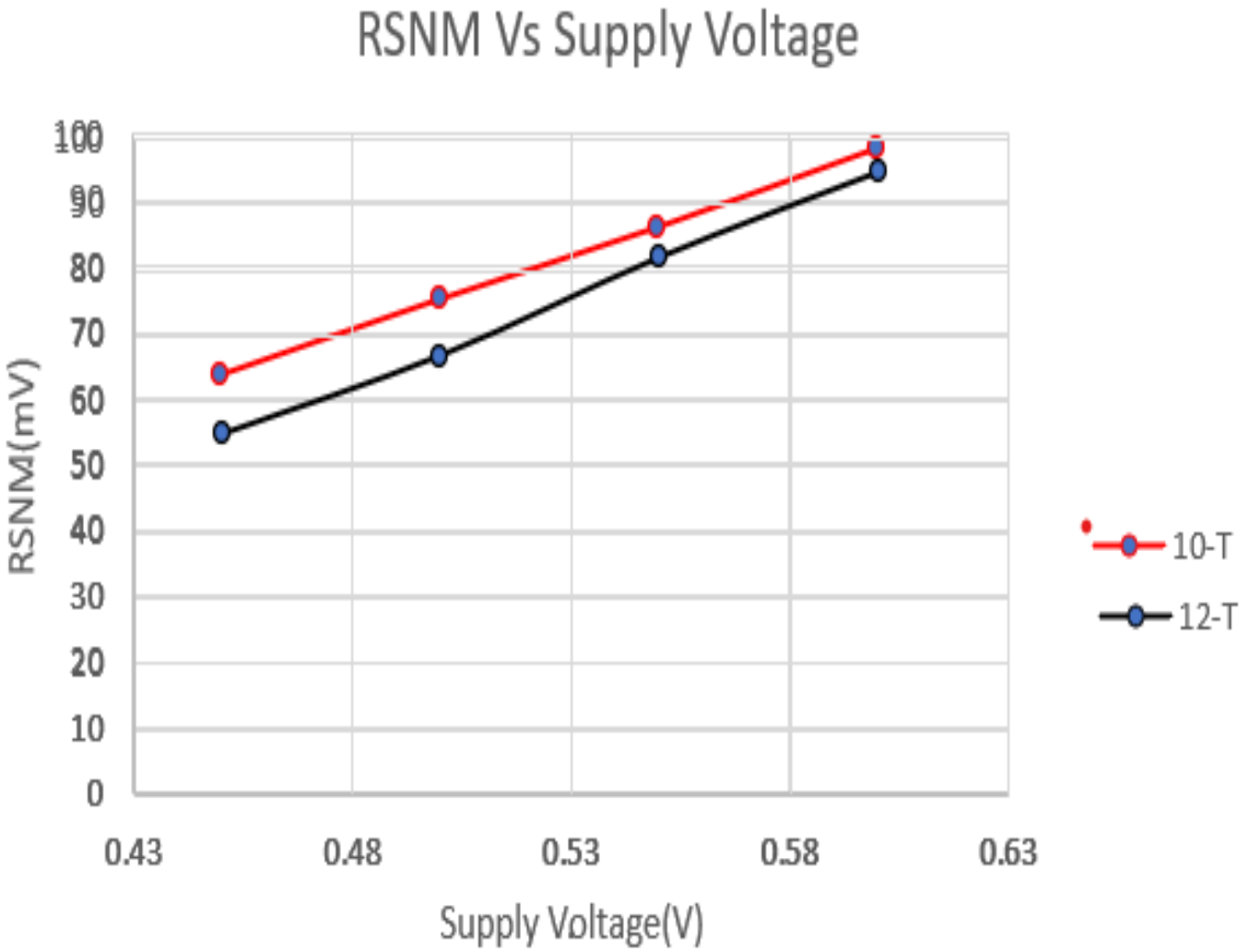
HOLD STATIC NOISE MARGIN

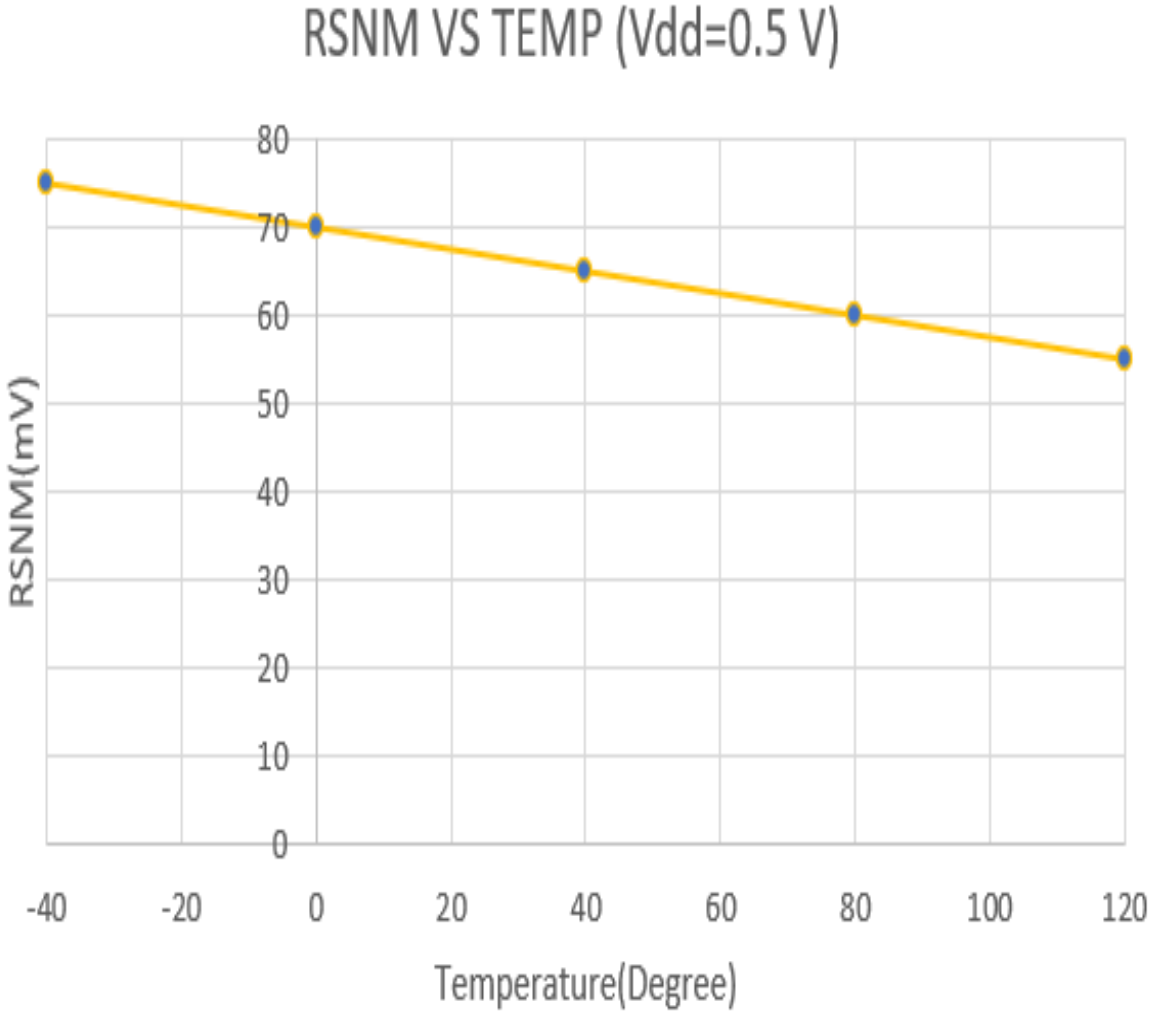


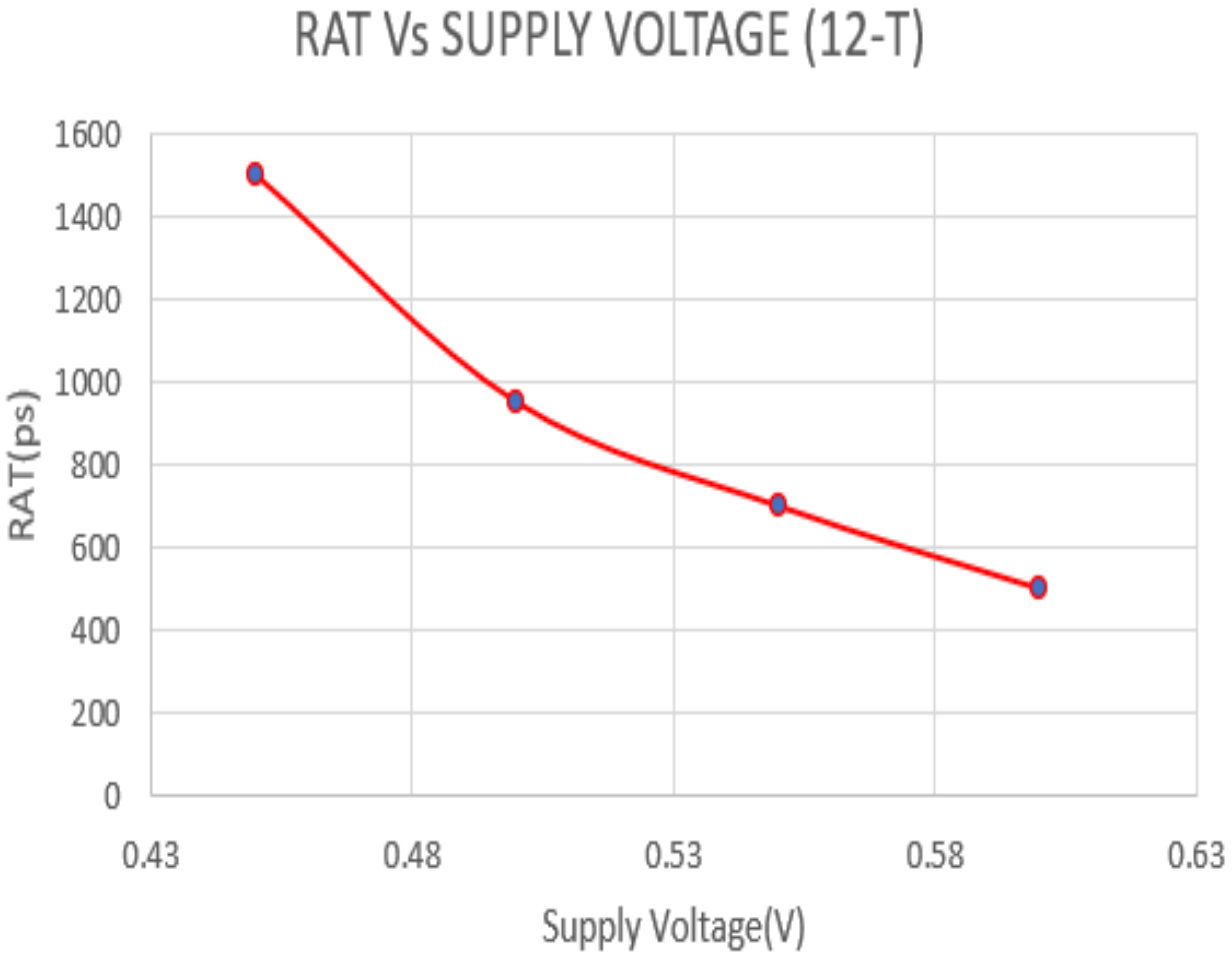
READ STATIC NOISE MARGIN

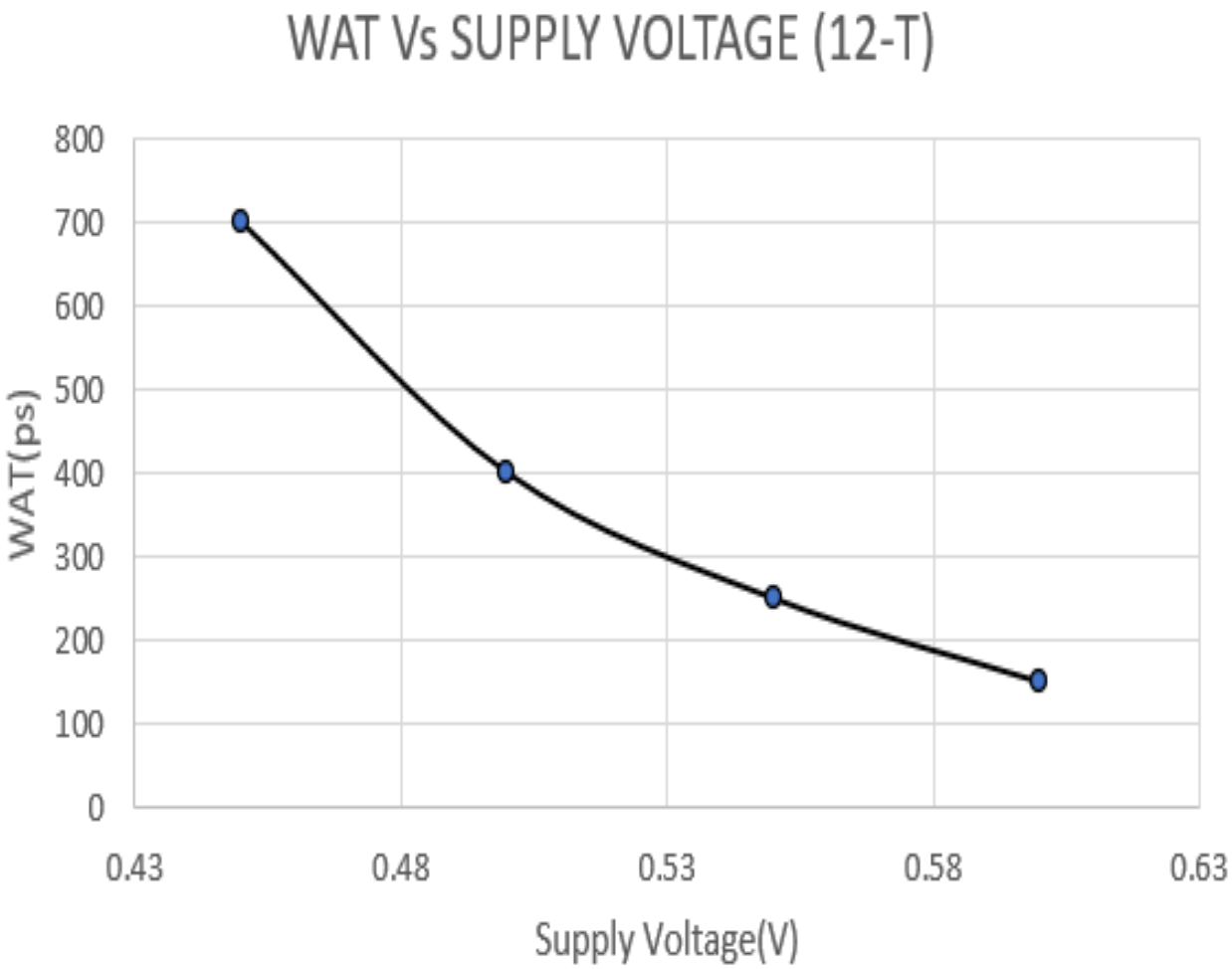



WSNM
1.4
1.2
1
0.8
0.6
0.4
0.2
0
Qn(Volts)
0
0.2
0.4
0.6
0.8
1
1.2
Q(Volts)

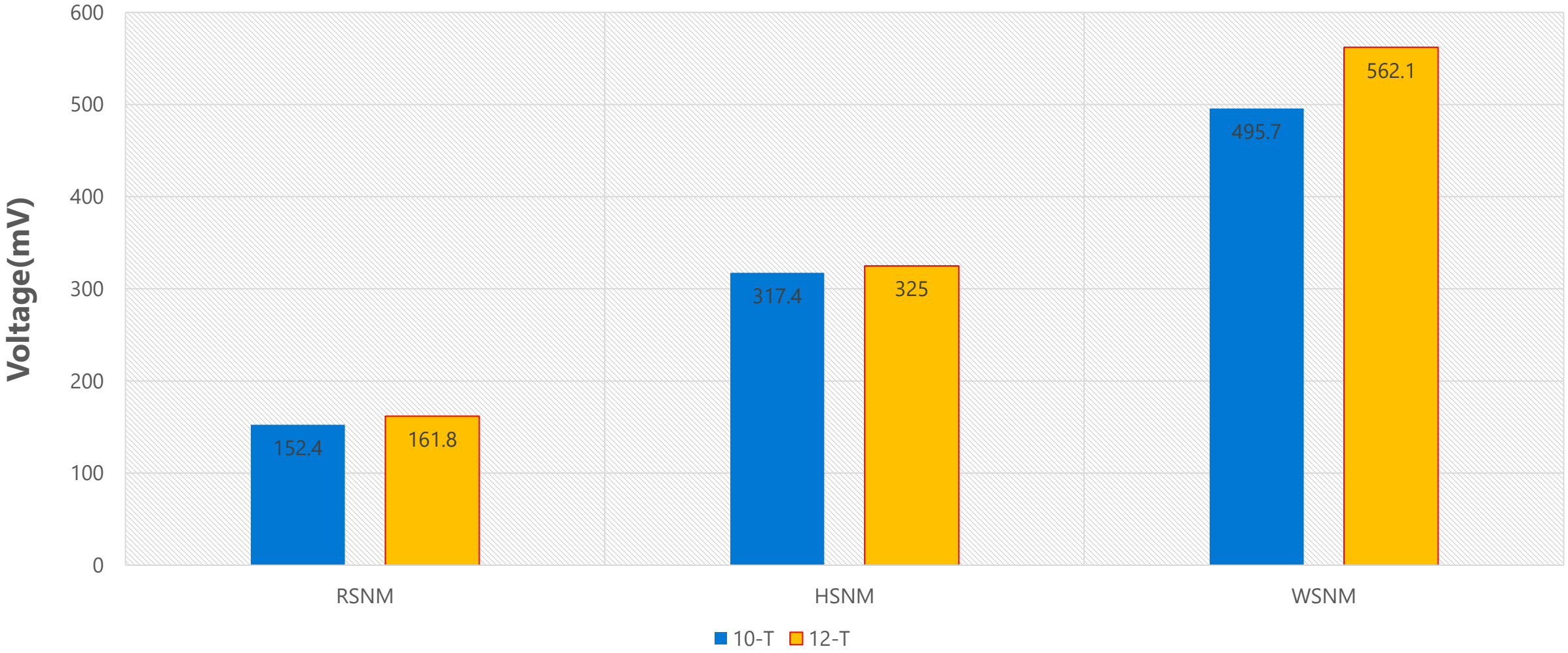

RSNM Vs Supply Voltage
RSNM(mV)
100
90
80
70
60
50
40
30
20
10
0
0.43
0.48
0.53
0.58
0.63
Supply Voltage(V)
10-T
12-T


RSNM VS TEMP (Vdd=0.5 V)
RSNM(mV)
80
70
60
50
40
30
20
10
0
-40
-20
0
20
40
60
80
100
120
Temperature(Degree)

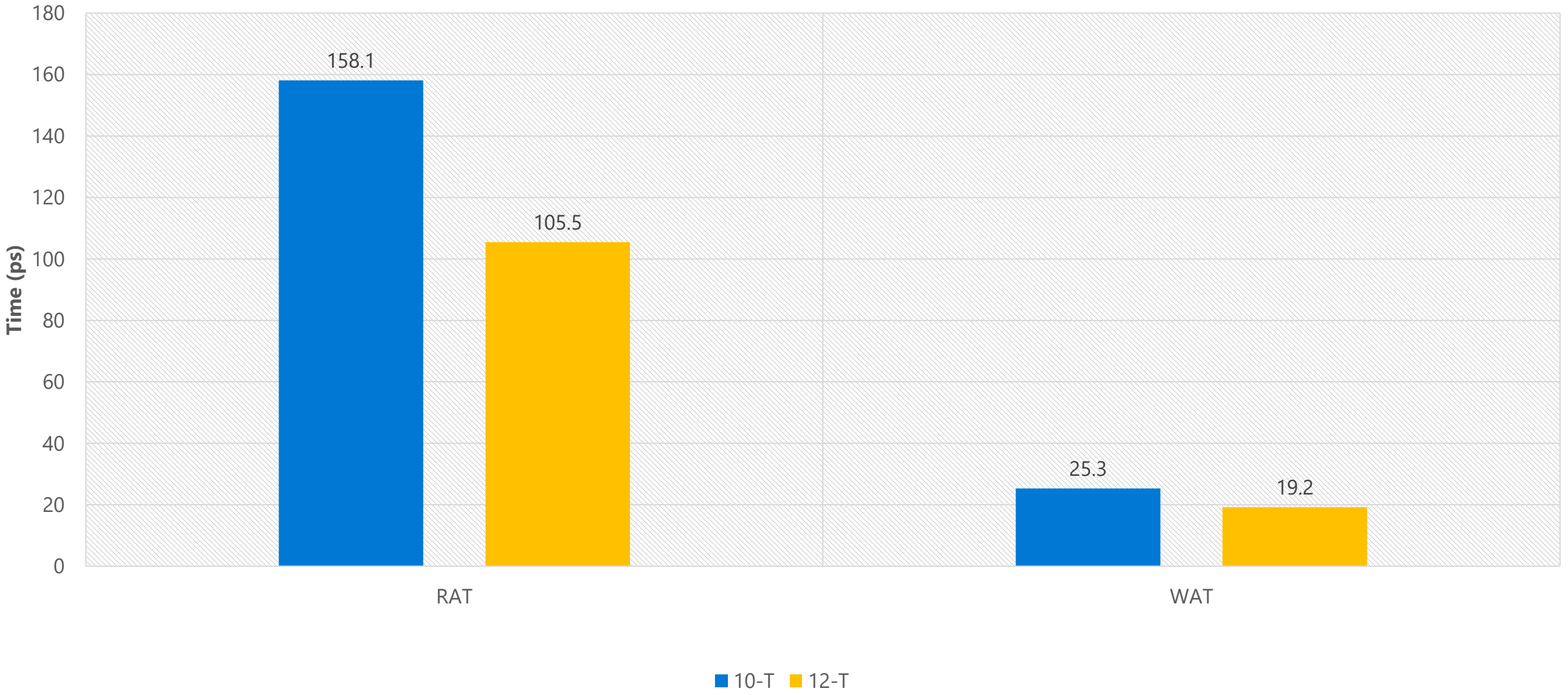

RAT Vs SUPPLY VOLTAGE (12-T)
1600
1400
1200
1000
800
600
400
200
0
RAT(ps)
0.43
0.48
0.53
0.58
0.63
Supply Voltage(V)


WAT Vs SUPPLY VOLTAGE (12-T)
800
700
600
500
400
300
200
100
0
WAT(ps)
0.43
0.48
0.53
0.58
0.63
Supply Voltage(V)

COMPARISON REPORT
NOISE MARGIN



COMPARISON OF WRITE ACCESS TIME (WAT)& READ ACCESS TIME(RAT)



RSNM Vs PROCESS CORNER VARIATION

PROCESS CORNER	RSNM(12-T)(mV)
SS	70.53
SF	103.61
FS	24.94
FF	42.89
NN	68.25

REPORT

	RSNM (mV)	HSNM (mV)	WSNM (mV)	RAT (ps)	WAT (ps)	LEAKAGE POWER (nW)	AREA (μm^2)
10-T	152.4	317.4	495.7	158.1	25.3	23.25	6.25
12-T	161.8	325.0	562.1	105.5	19.2	29.73	7.84

Resources

- M. Alioto, “Ultra-low power VLSI circuit design demystified and explained: A tutorial,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012.
- A. T. Do et al., “0.2 V 8T SRAM with PVT-aware bitline sensing and column-based data randomization,” IEEE J. Solid-State Circuits, vol. 51, no. 6, pp. 1487–1498, Jun. 2016.
- M. T. Bohr and I. A. Young, “CMOS scaling trends and beyond,” IEEE Micro, vol. 37, no. 6, pp. 20–29, Dec. 2017.
- J. Jiang et al., “Low-cost single event double-upset tolerant latch design,” Electron. Lett., vol. 54, no. 9, pp. 554–556, May 2018.

- A. T. Do et al., “0.2 V 8T SRAM with PVT-aware bitline sensing and column-based data randomization,” IEEE J. Solid-State Circuits, vol. 51, no. 6, pp. 1487–1498, Jun. 2016.

- I.-S. Jung, Y.-B. Kim, and F. Lombardi, “A novel sort error hardened 10T SRAM cells for low voltage operation,” in Proc. IEEE 55th Int. MWSCAS, Aug. 2012, pp. 714–717.

Questions & answers