VL 502 Analog CMOS VLSI Design
Spice Assignment – 3: Telescopic Cascode Differential Amplifier Design

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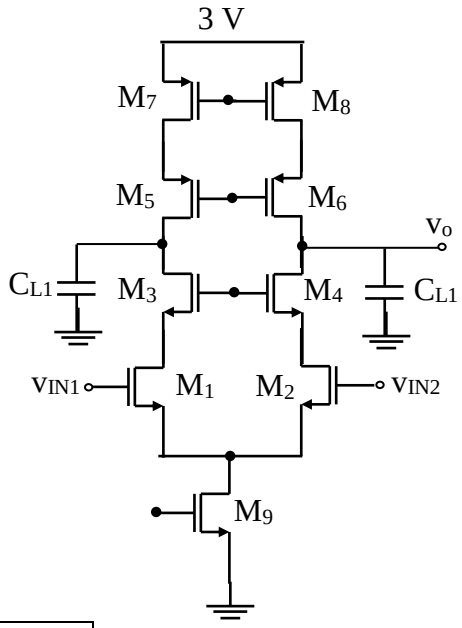
Due: 9 am, Wednesday, 17 November, 2021

Design the CMOS differential amplifier with a single-ended output shown in the figure.



Use the Spice model parameters you used for the first two assignments.

You will use this differential amplifier in the fourth Spice assignment to design a 2-stage operational amplifier, by connecting the common-source amplifier of Assignment 2 to its output.

Make sure to include AD, AS, PD, PS in the description of each MOSFET. Connect the body terminals of all NMOS transistors to ground, and the body terminals of all PMOS transistors to V_{DD}.

The specifications you have to meet are as follows:

Differential-mode voltage gain, A_{dm} (≥)	As specified in Table 1 below
C_{L1}	A_{dm} * C_C (C_C is of your Assignment 2)
CMRR (≥)	35 dB
-3dB frequency	Highest possible
dc power consumption (≤)	As specified in Table 1 below
Output voltage swing (≥)	2.3 V to 2.6 V

Table 1 Group-wise specifications

Group	Power (µW)	Gain
1	510	2000
2	600	2500
3	720	3000
4	810	3500
5	900	4000
6	1020	4500
7	1110	5000
8	1200	5500
9	1320	6000
10	1410	6500

Group	Power (µW)	Gain
11	1500	7000
12	1620	7500
13	1710	8000
14	1800	8500
15	1920	9000
16	2010	9500
17	2100	10000
18	2220	10500
19	2310	11000
20	2400	11500
21	2520	12000

The submission will be your (.cir) Spice file, ready to perform an ac simulation for a differential input. Please write the differential-mode gain, CMRR, -3 dB frequency, and the dc power consumption your circuit achieves, as comments at the top of your Spice file.

Upload your final design values in the Excel file at this link: https://iiitbac-my.sharepoint.com/:x:/g/personal/chetan_parikh_iiitb_ac_in/EdkH5ypqG2FIsagTAcm7OSUBEO1Alvji1j5SEzSaGiVKnQ?e=1WpaMc

Steps to design a telescopic cascode differential amplifier

The following steps will assist you in designing the amplifier. Please also watch the video lecture 32: https://youtu.be/hVX2jP56R4A

Step 1

It is best to begin by designing a single-input telescopic cascode (M_1-M_3-M_5-M_7) :

- The dc power consumption decides the dc current (I_{D9} = power/V_{DD} = $2I_{D1}$).
- Start with the voltage swing specification:
  - The output voltage needs to be between 2.3 V and 2.6 V. This requirement comes from the CS second stage which has a PMOS input (look up your Assignment-2) which needs a dc bias of around 2.5 V.
  - Given this output voltage range, the PMOS transistors will need small overdrive voltages.
  - The NMOS transistors *can* have large overdrive voltages.
  - But $V_{OV1\text{-}2}$ need to be small to meet the gain specification.
  - Making $V_{OV3\text{-}4}$ large will allow their sizes to be small. But this is not of great importance because the load capacitance is large, and therefore MOSFET sizes will not play a significant role in determining the frequency response. Instead, $V_{G3\text{-}4}$ can be made large (while keeping V_{OV3} not large). This will make the source voltages of M_3 (which are the drain voltages of M_1) large, and thus the λ of M_1 large, which is good.
- Write the equation for the voltage gain, and decide values of the lengths and the overdrive voltages (keeping in mind the constraints you have already decided above), to meet the gain specification.
- Perhaps simultaneously, consider the -3dB frequency (f_{-3dB}). f_{-3dB} can be written approximately as the reciprocal of the time-constant at the output node:

$$f_{-3dB} = \frac{1}{R_{out}(C_L + C_1)}$$

  where R_{out} = (g_{m3} r_{o3} r_{o1} || g_{m5} r_{o5} r_{o7}), and C_1 is the sum of all MOSFET capacitances at the output node. To maximize f_{-3dB}, R_{out} has to be minimum, but for a high voltage gain, R_{out} has to be high. So you will have to optimize R_{out} so as to meet the gain specification and then make f_{-3dB} as high as you can.
- The dc gate voltages of M_1 and M_7 must be carefully matched so that their saturation currents are exactly equal. This you will do along with designing for the voltage gain, as I had discussed for Assignment-2 (see the recorded Lecture-17, at about 48:00 in the video).
- Then do a .ac analysis: Make sure that the low frequency voltage gain is 60 dB. Measure the -3dB frequency, and see if you can make it any higher.

Step 2

Now build the complete differential amplifier.

- M_2-M_4-M_6-M_8 will simply be replicas of M_1-M_3-M_5-M_7. If you are lucky, you will not have to change the dc gate voltages of M_3-M_5-M_7.
- The gate voltages of M_1-M_2 will be the input voltages. As long as they are kept larger than some minimum, and smaller than some maximum, their value will not matter (why?).

- M_9 will have to be designed to provide the dc tail current, and to meet the CMRR specification. Its saturation current will have to be exactly twice the saturation current of M_7. This will require specifying this voltage to a high accuracy (many decimal places).

- Once you have built the circuit, do a .dc simulation keeping V_{IN2} constant and varying V_{IN1} from 0 to 3 V and observe the differential-mode transfer characteristics you get (plot both the output voltages and make sure that they have the same value at the dc bias point you decide). The slope will be the differential mode gain – A_{dm} (or will it be twice of A_{dm}?!).

- If you do a .dc simulation with V_{IN1} and V_{IN2} shorted together and varying that voltage, you will get the common-mode transfer characteristics.

- The above two dc transfer characteristics are very rich in information, and you will be able to understand which transistors are in triode and which in saturation, by plotting various node voltages. If the circuit is poorly designed, these characteristics will show strange behaviours!

- Once the dc transfer characteristics are satisfactory, do .ac analyses:
    - Append "ac 0.5" and "ac -0.5" to the two input voltage source and do the .ac analysis. This will directly give you the differential mode again, and the -3dB frequency.
    - Append "ac 1" to both the input voltage sources and do the .ac analysis. This will give you the common-mode gain, from which you can calculate CMRR.