EE6320 RF Integrated Circuits
Project: PA Design

PA Performance Summary Table

Design Parameter	Design Metric	Performance	Specification
Output P1dB	f_o = 5.17 GHz	10.2609	$\geqslant$ +10 dBm
	f_o = 5.245 GHz	10.2793	$\geqslant$ +10 dBm
	f_o = 5.32 GHz	10.2963	$\geqslant$ +10 dBm
AM-PM Deviation (at P1dB)	f_o = 5.17 GHz	1.3 deg	$\leqslant$ 5 degrees
	f_o = 5.245 GHz	1.3 deg	$\leqslant$ 5 degrees
	f_o = 5.32 GHz	1.3 deg	$\leqslant$ 5 degrees
Voltage Gain (from Gate to Drain)	f_o = 5.17 GHz	10.65	$\geqslant$ 2
	f_o = 5.245 GHz	10.61	$\geqslant$ 2
	f_o = 5.32 GHz	10.58	$\geqslant$ 2
Power (at 5.245 GHz)	PA Average Consumption (excluding bias)	27.156 mW	Minimize
	Bias Circuit Consumption	27.1 uW	Minimize
Other	Sum of all Capacitances (including ac coupling)	20.838p	-
	Inductance Used	3.7	-
	Device Width	1.4mm	-

	Simulator Used	Virtuoso	-

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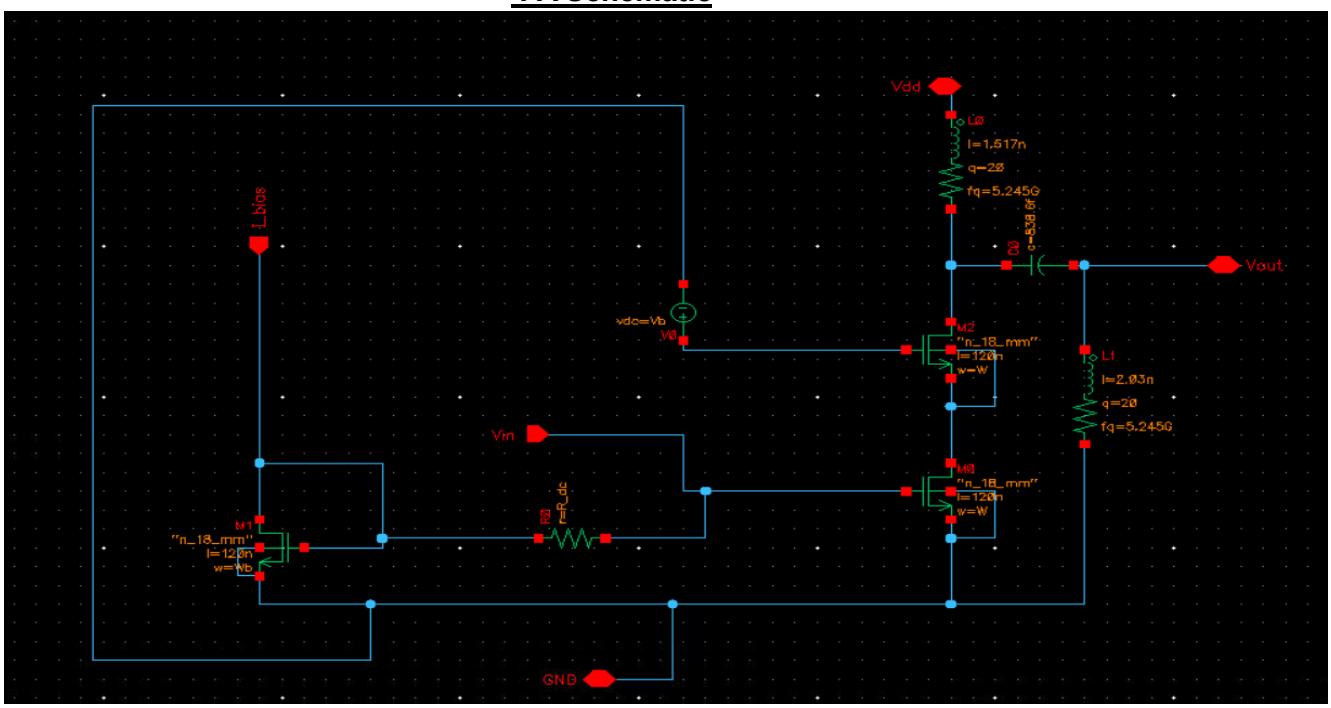
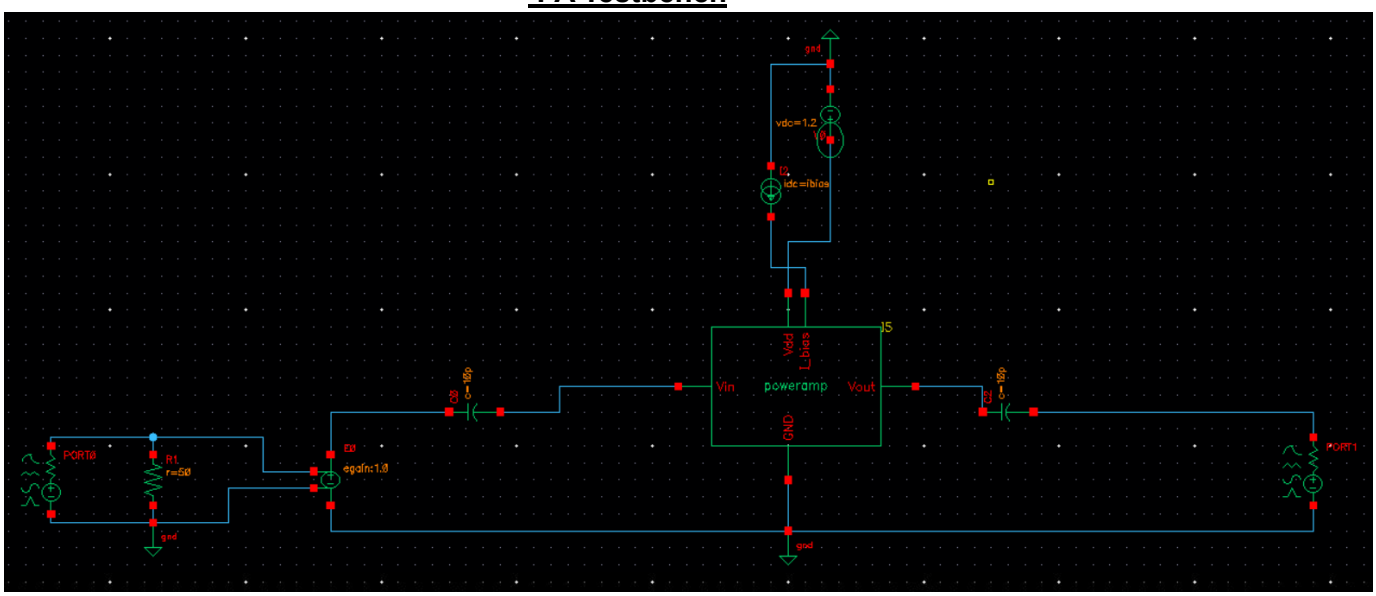
Roll No: EE21B103

PA Schematic



PA Testbench

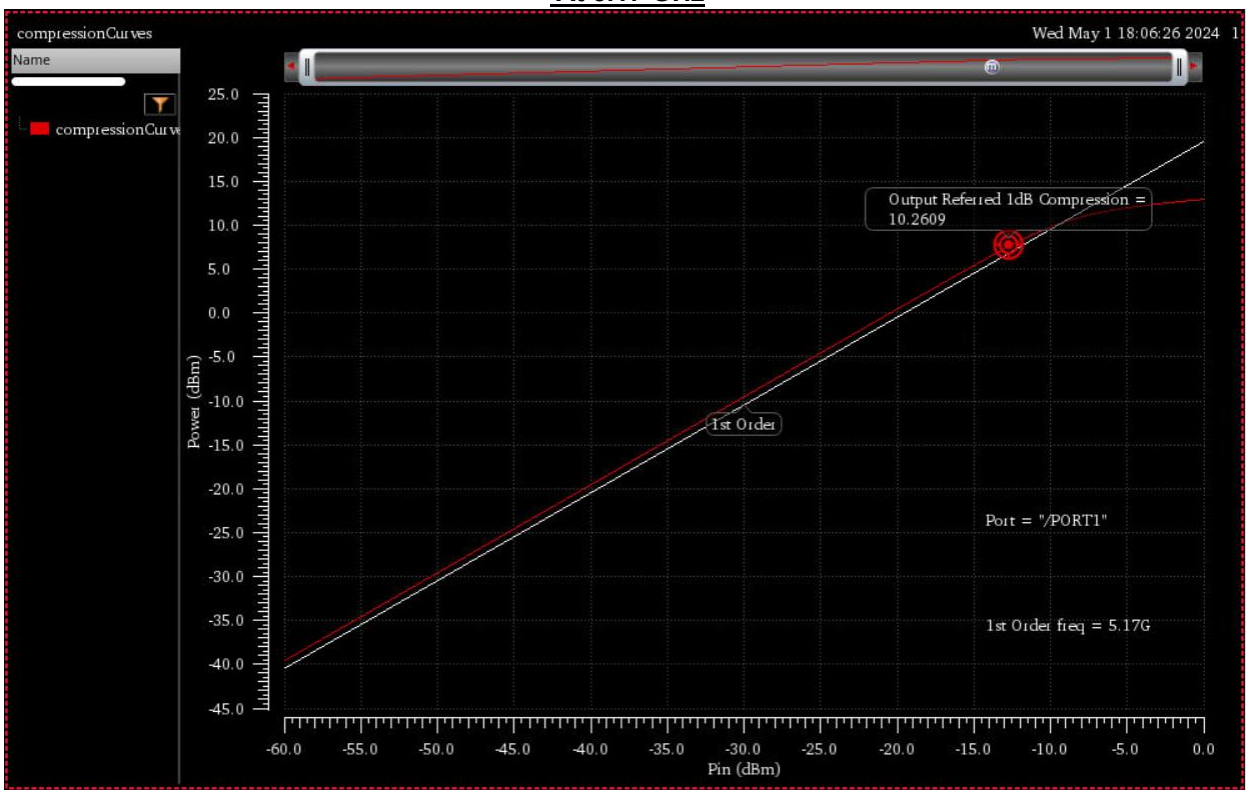


Component Values Table

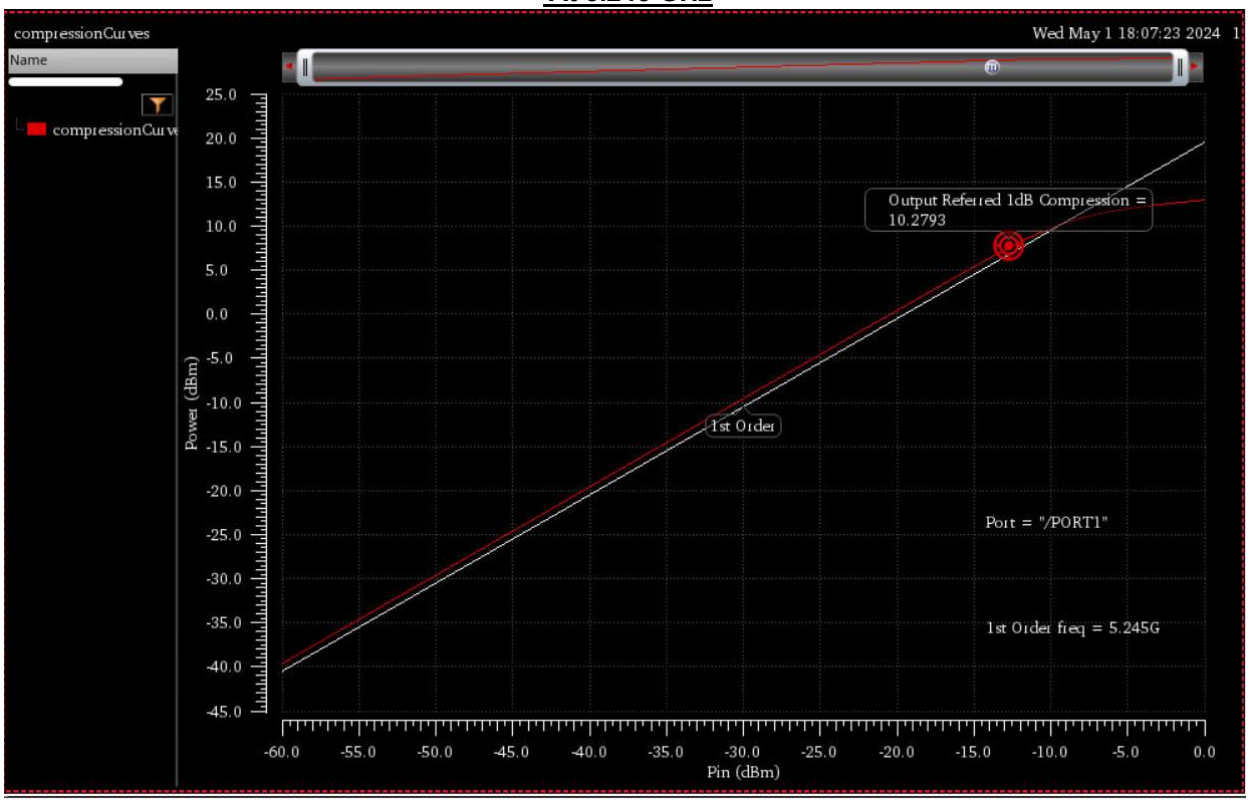
(W, L) MOS Amplifier = 1.4 mm, 120nm	(L, C, L2) Drain Tank = 1.517n, 868.3f, 2.03n
(W, L) Current Mirror MOS = 2.7um, 120nm	Bias Current = 50u
R_bias = 1 MΩ, C_coupling = 10p	V_DD = 1.2V , R_load = 50 ohms

Output 1dB Compression Point Plots

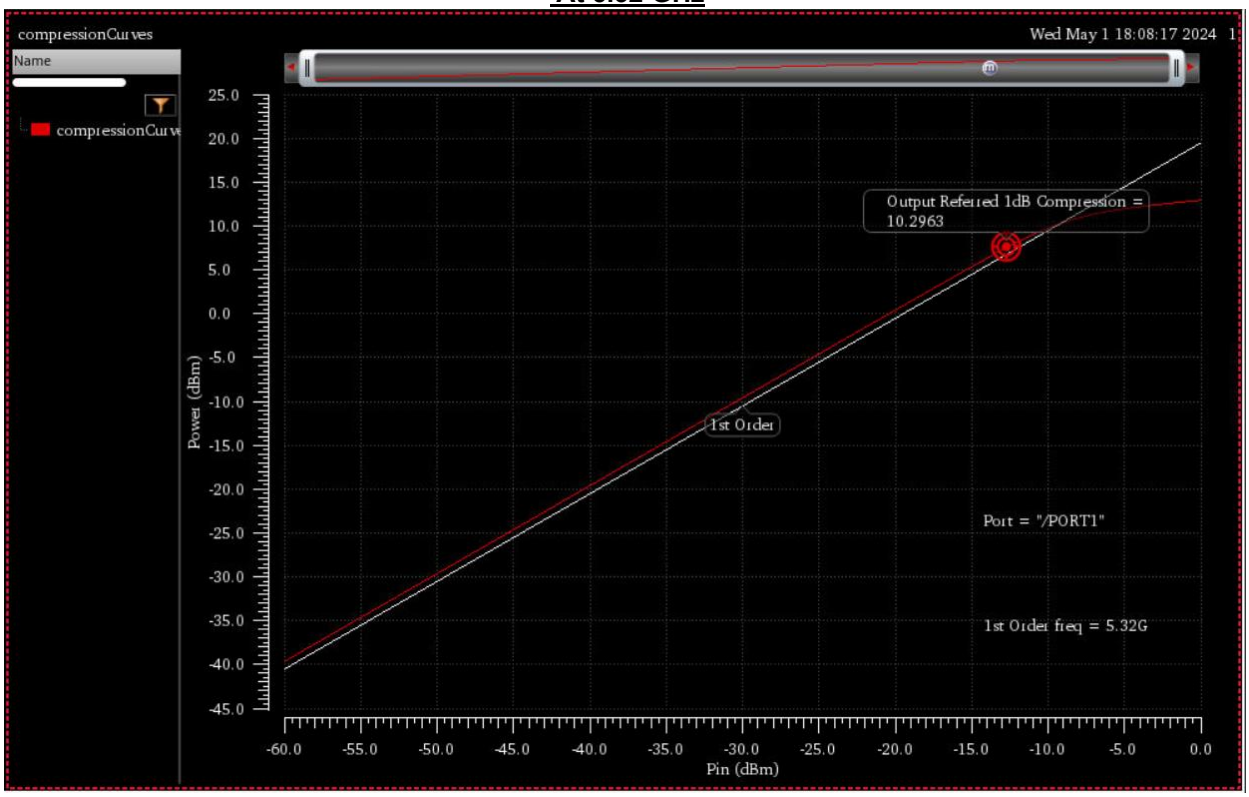
At 5.17 GHz



At 5.245 GHz

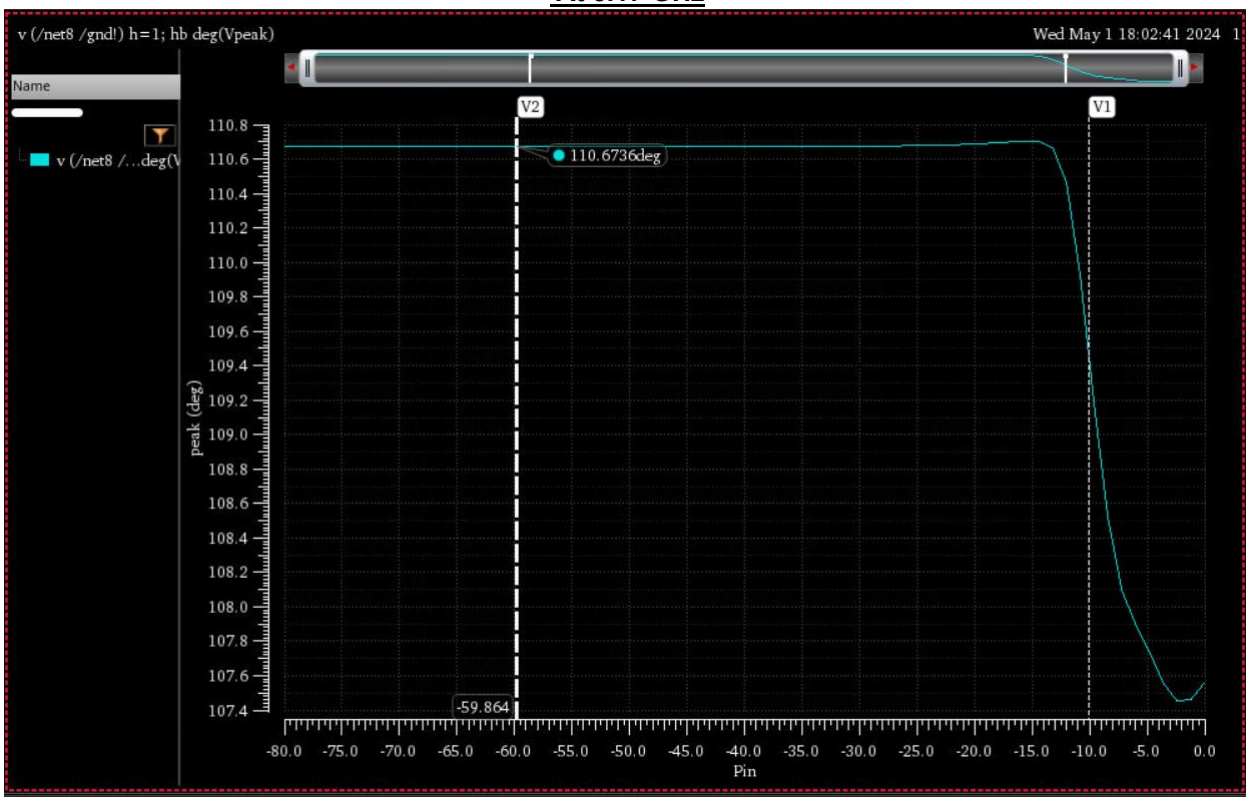


At 5.32 GHz

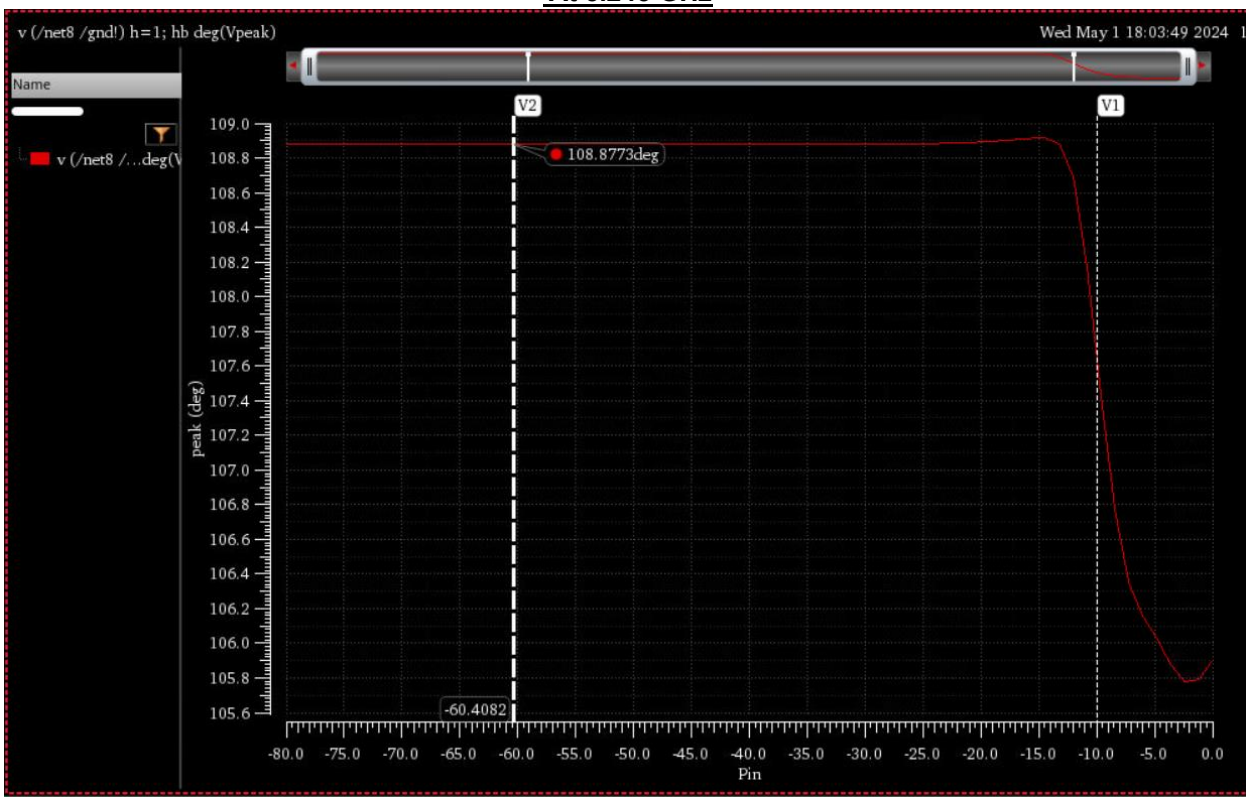


AM-PM Deviation Plots

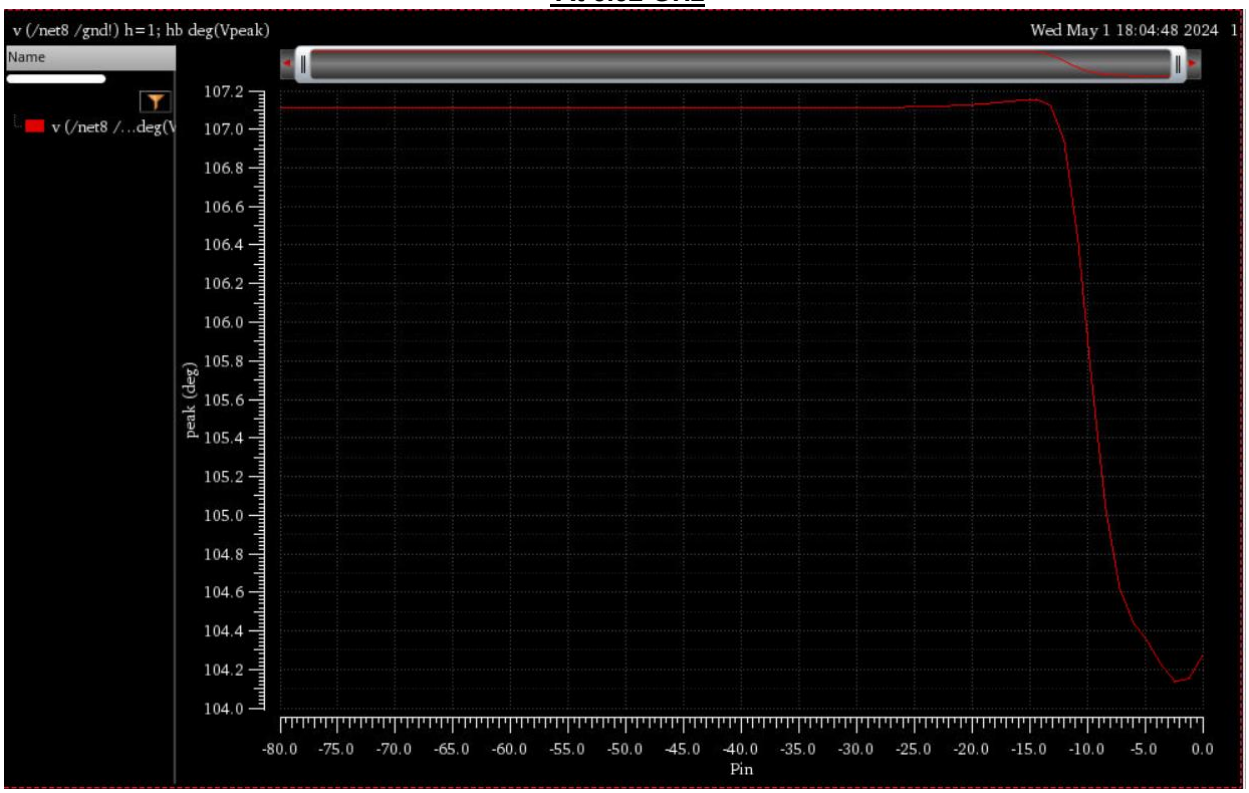
At 5.17 GHz



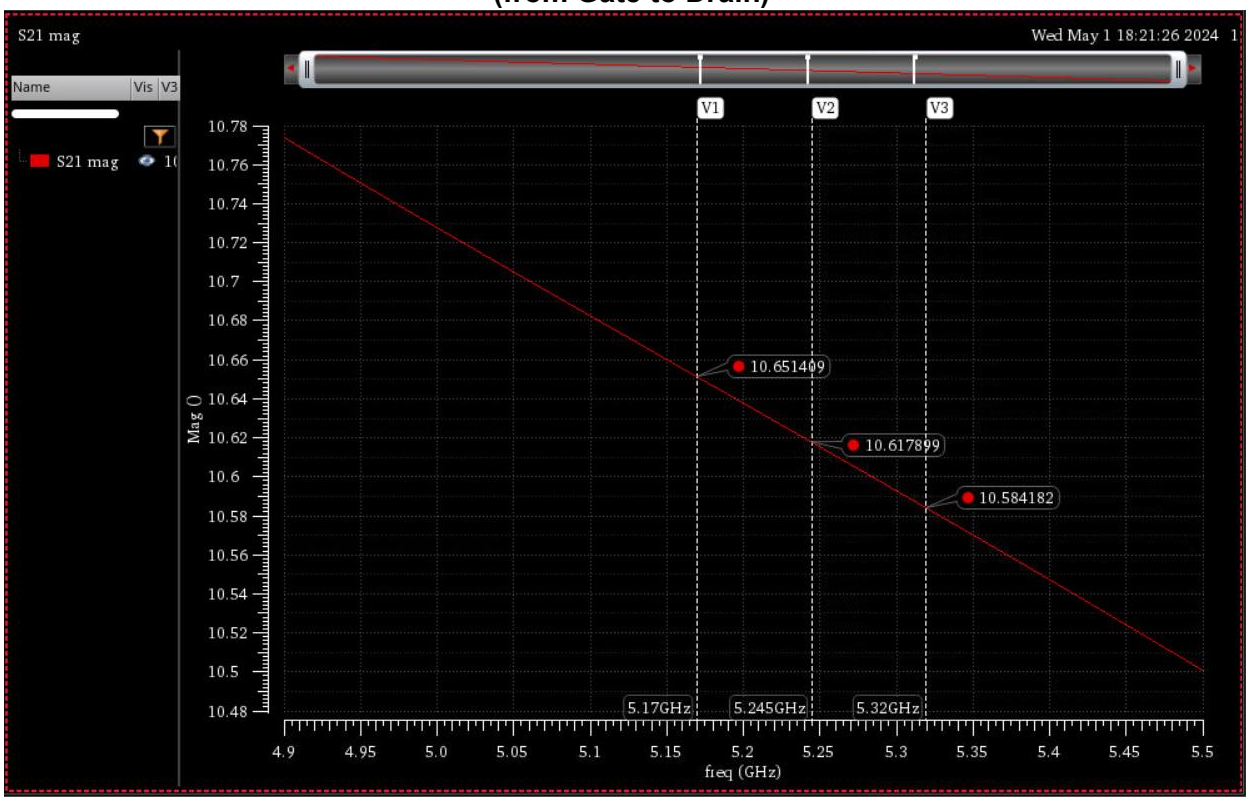
At 5.245 GHz



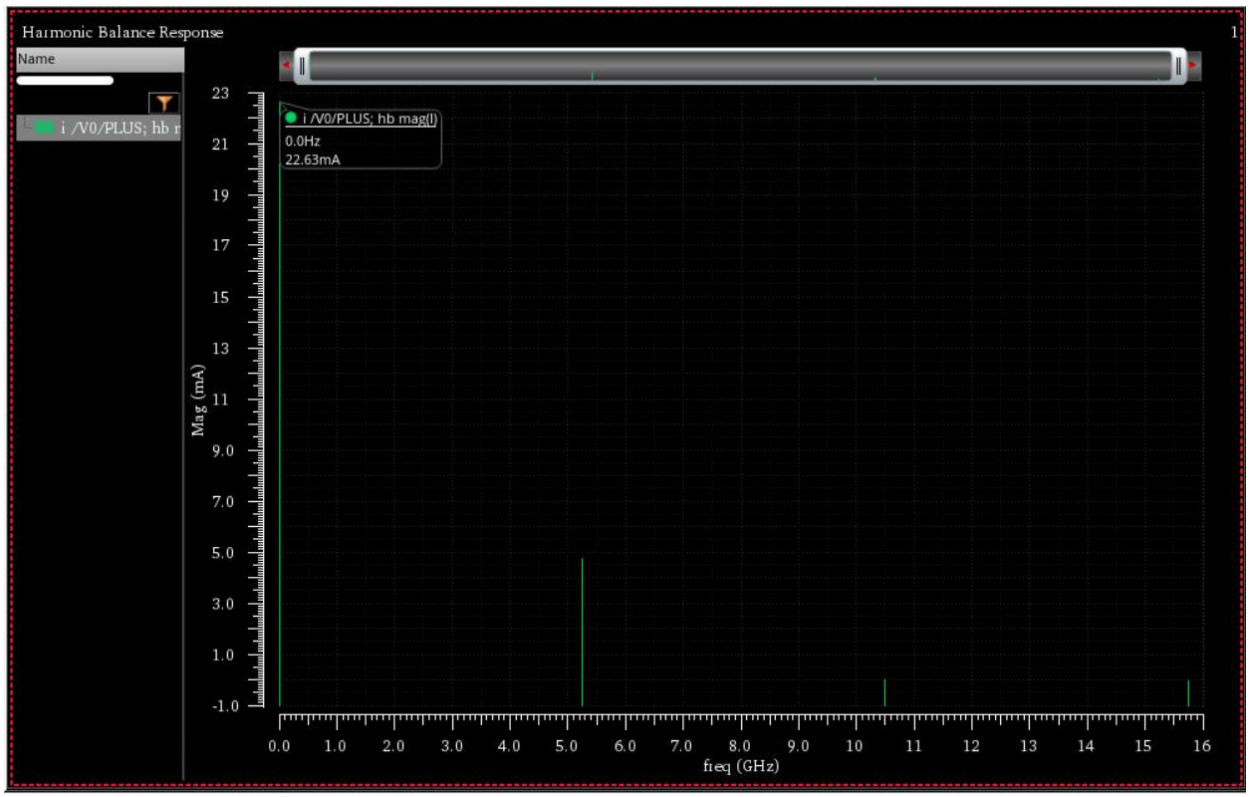
At 5.32 GHz



PA Volatge Gain Plot
(from Gate to Drain)



Current through VDD Plot
(at 5.245 GHz)



Design Procedure

1) Down converted the R_load to a lower value of 20 ohms to increase the swing limits at the drain. The Q of the matching network is 1.
2) The current through the amplifier mosfet has to be at least more than 20mAs based on the specs given.
3) An appropriate bias current of 50uA was chose, the W parameters of the mosfets were decided on that.
4) Based on the DC parameters of the cascode mosfet, the value of bias voltage of the cascode mosfet was chosen.
5) Then I made slight adjustments to both inductances, as the AM-PM plots were little off.

Path to Project Files

Amplifier : home/ee21b103/cadence_project/RFIC_2024/poweramp
Testbench : home/ee21b103/cadence_project/RFIC_2024/pa_testbench

Note: All the schematic/plots put up here are for reference only. Please replace them with the respective plots/schematic used or obtained by you.