EE6320 RF Integrated Circuits Project: VCO Design

VCO Performance Summary Table

Design Parameter	Design Metric	Performance	Specification
Output Amplitude (Vpp/2)	freq = 5.17 GHz	0.82	≥ 0.8V
	freq = 5.245 GHz	0.82	≥ 0.8V
	freq = 5.32 GHz	0.82	≥ 0.8V
Phase Noise (1 MHz Offset)	freq = 5.17 GHz	-121.9	≤ -118 dBc/Hz
	freq = 5.245 GHz	-121.9	≤ -118 dBc/Hz
	freq = 5.32 GHz	-121.9	≤ -118 dBc/Hz
Phase Noise (20 MHz Offset)	freq = 5.17 GHz	-150.6	≤ -150 dBc/Hz
	freq = 5.245 GHz	-150.6	≤ -150 dBc/Hz
	freq = 5.32 GHz	-150.6	≤ -150 dBc/Hz
Tuning Range	Total Tuning Range	170MHz	≥ 150 MHz
	Nunber of bits in coarse tuning	<only if cap. bank is used>	-
	Voltage range in fine tuning	<only if cap. bank is used>	-
	Average KVCO	154.7	150 MHz/V
	% variation in KVCO	300%	minimal
Power Consumption (5.245 GHz)	VCO average power consumption (excluding bias)	1.1157 mW	minimal

	Bias circuit	55uw	**minimal**
Other	**Sum of all capacitances (in capacitor bank)**	**<only if cap. bank is used>**	**-**
	Net inductance used	2.88n + 25p	**-**
	Simulator used	Virtuoso	**-**

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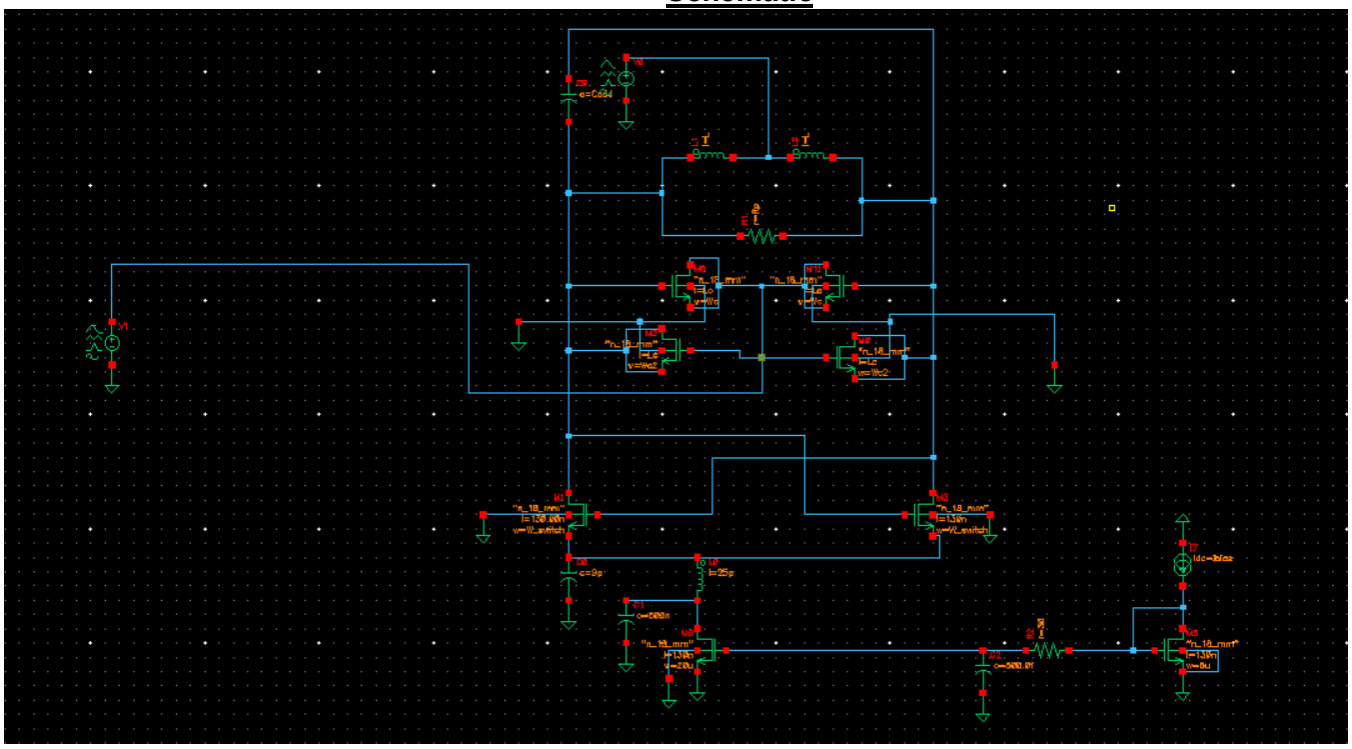
Component Values Table

Component	Value <report only those which are used by you>
(W, L) Current Mirror MOS	5u, 130n
(W, L) Tail MOS	20u, 130n
(R, C) Low Pass Noise Cancelling Filter	30, 500f
Tail Capacitance	500n
(L, C) Tail Tank	25p, 9p
(W, L) Cross Coupled MOS(s)	NA
(W, L) Switching MOS(s)	15u, 130n
(C1, C2) Capacitor Bank	NA
(W, L) Varactor MOS	(50u, 130n) all 4 varactors
(R, L) Drain Tank	3K, 2.88n
(V bias, I bias)	1.2V, 100u

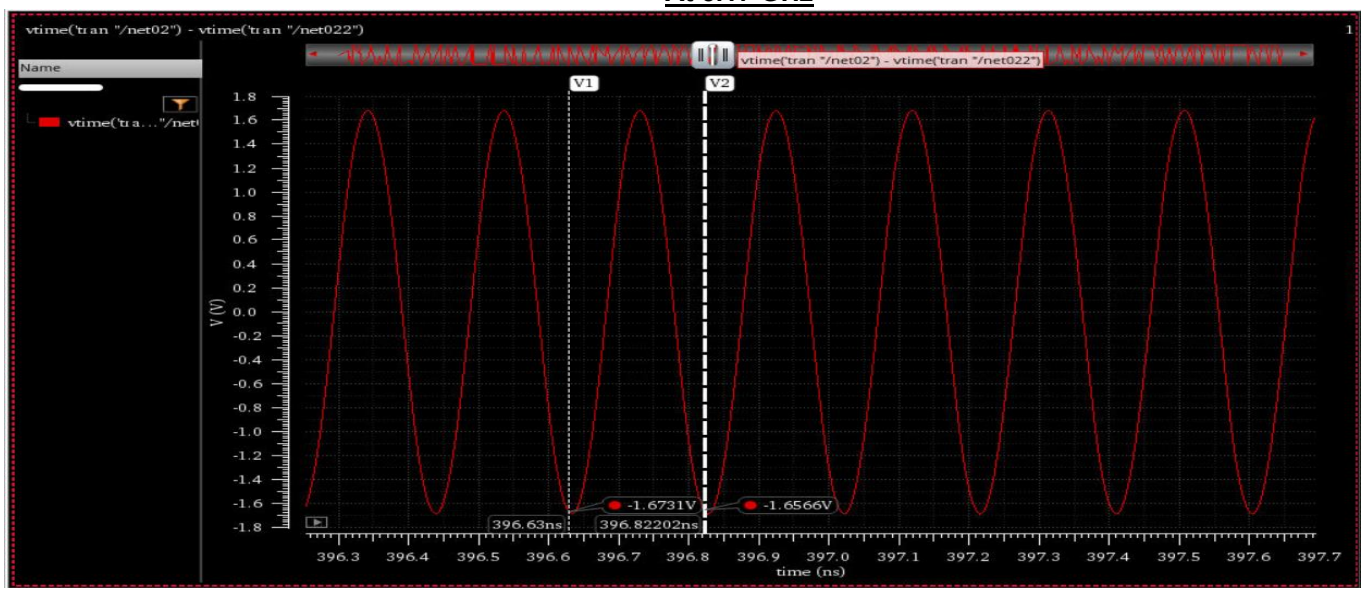
Schematic



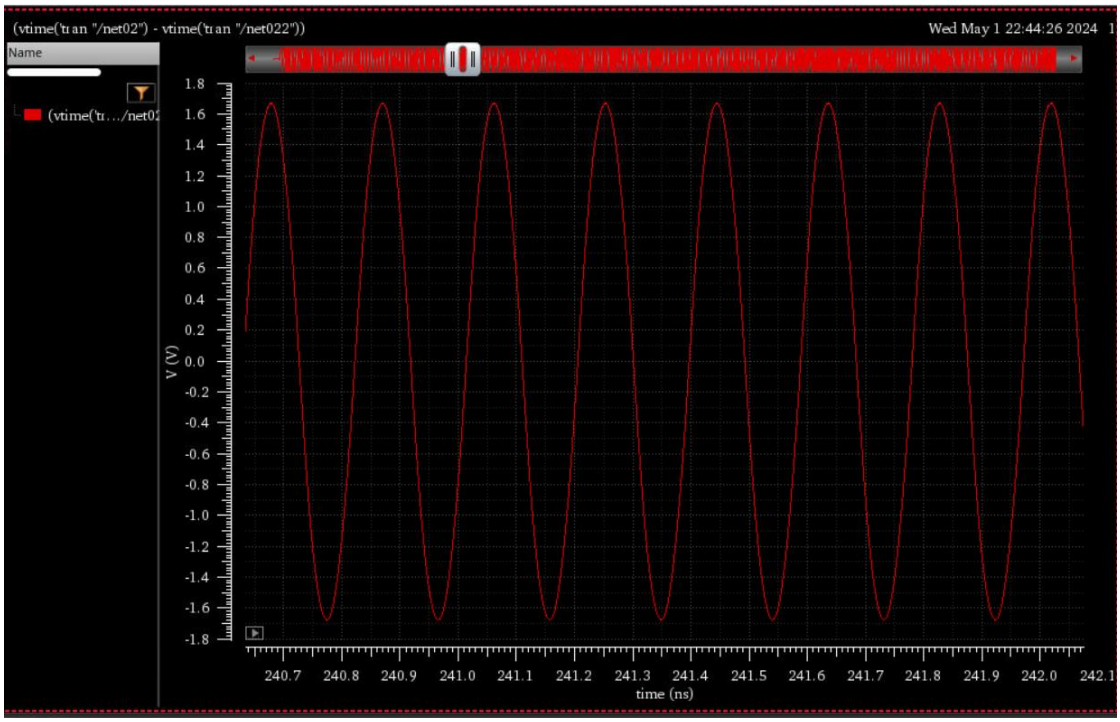
Output Amplitude Plots

(differential settled waveforms)

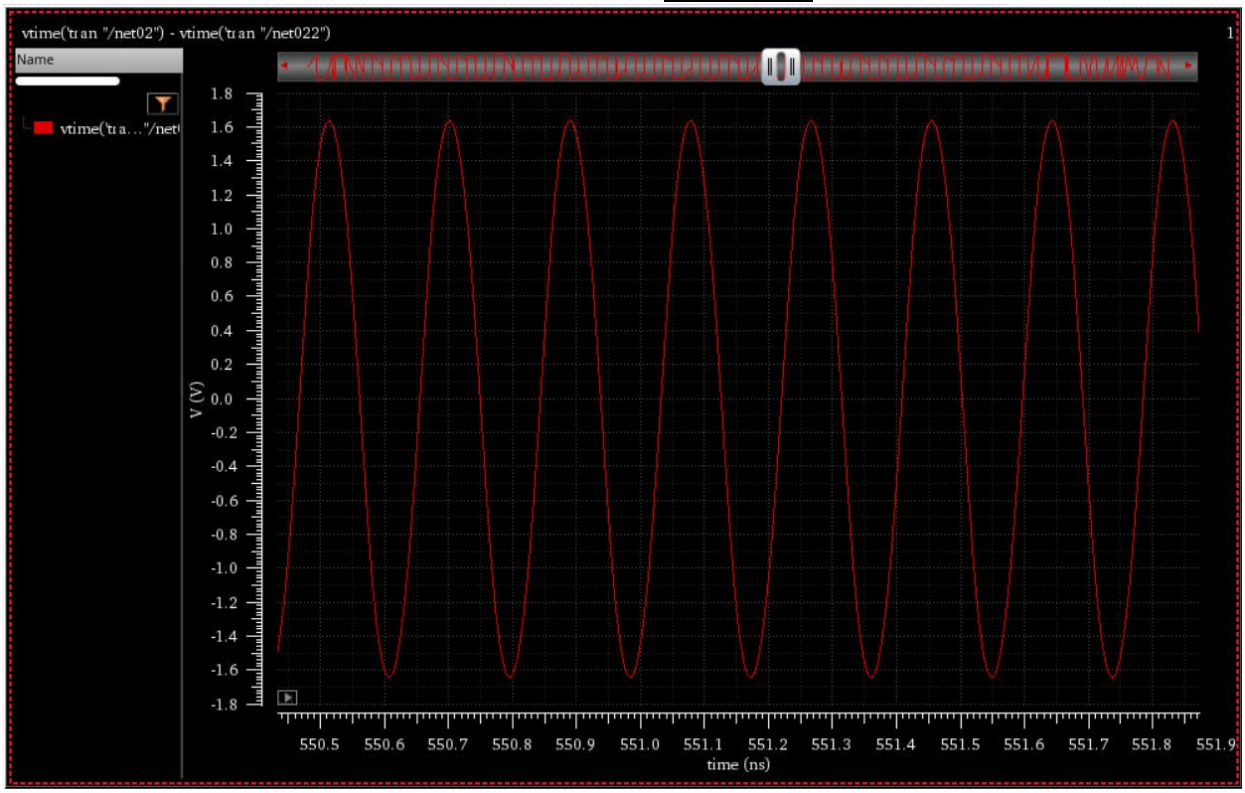
At 5.17 GHz



At 5.245 GHz



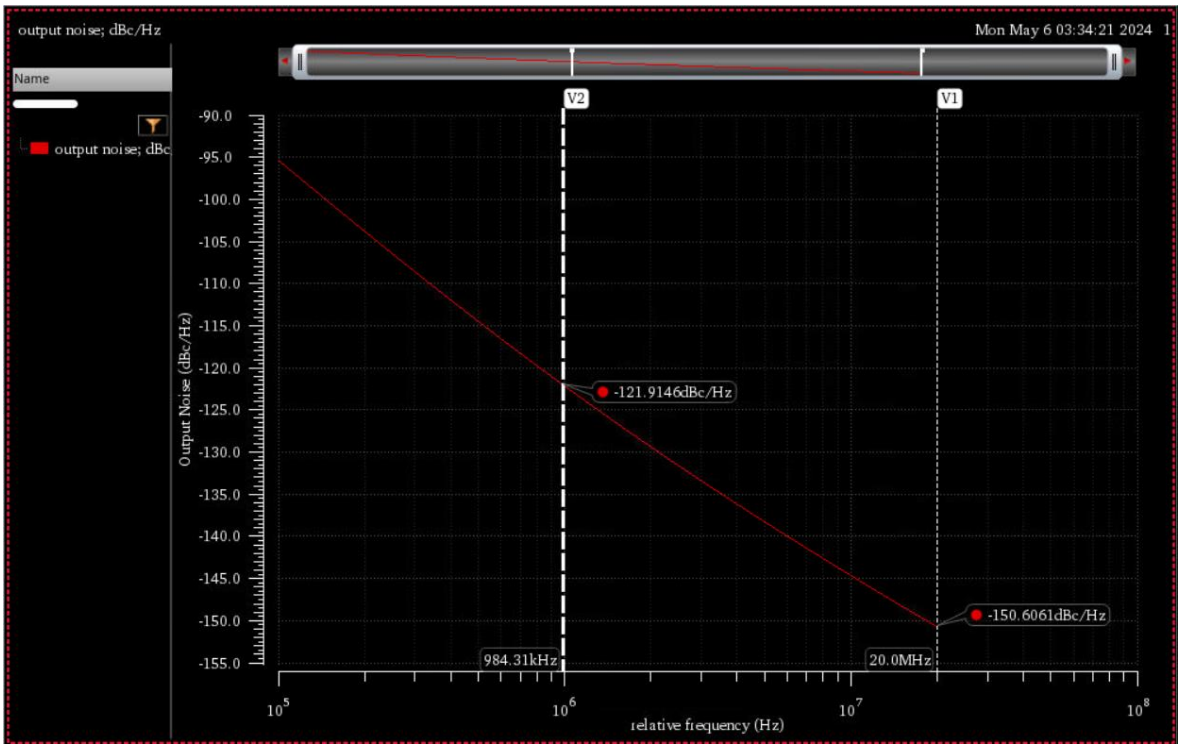
At 5.32 GHz



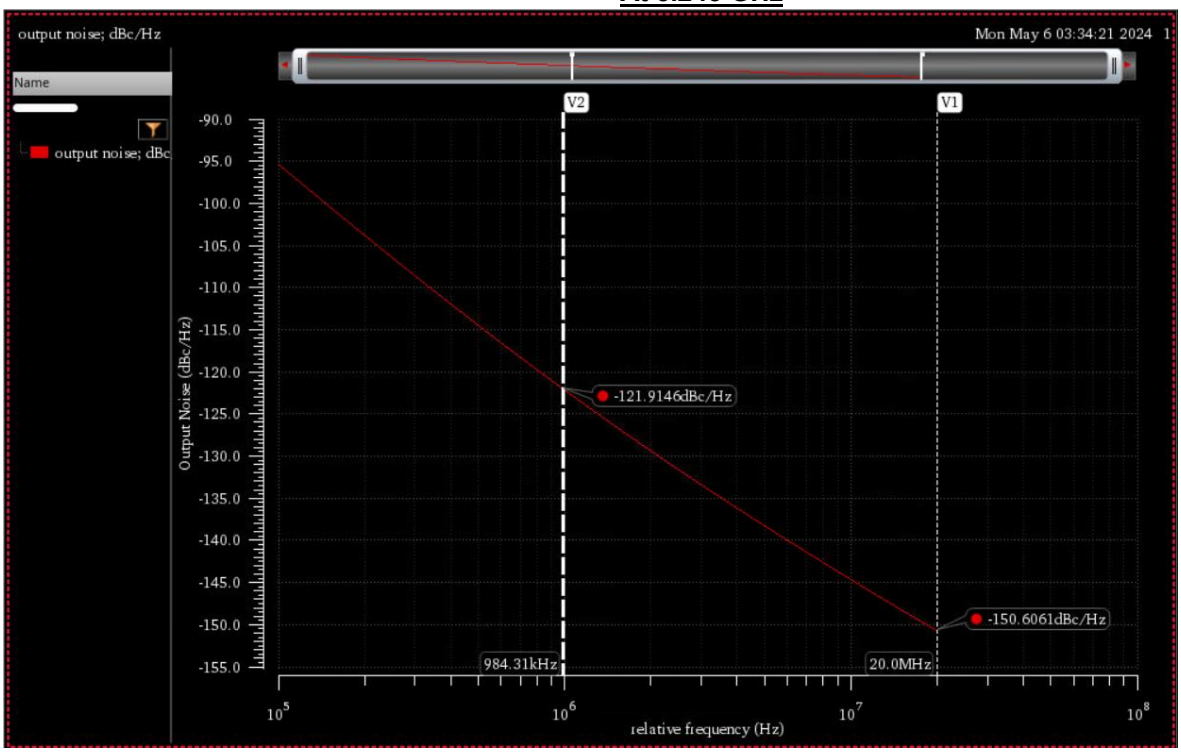
Phase Noise Plots

(at 1 MHz and 20 MHz)

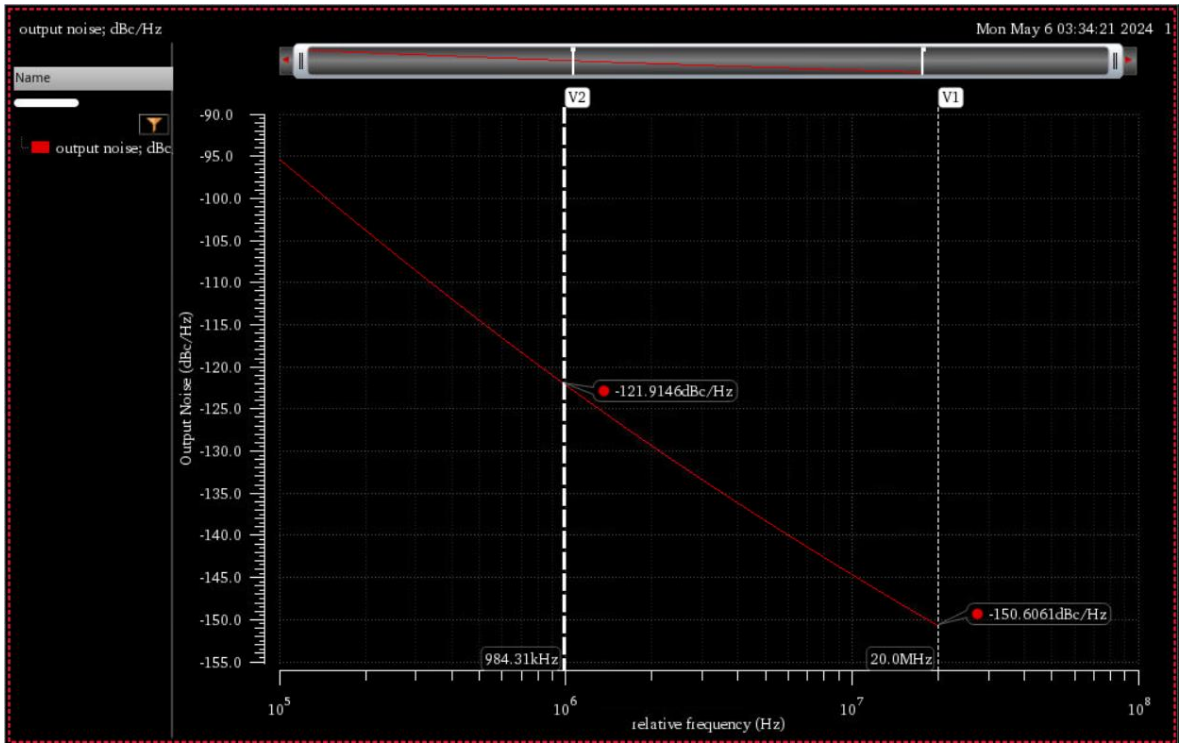
At 5.17 GHz



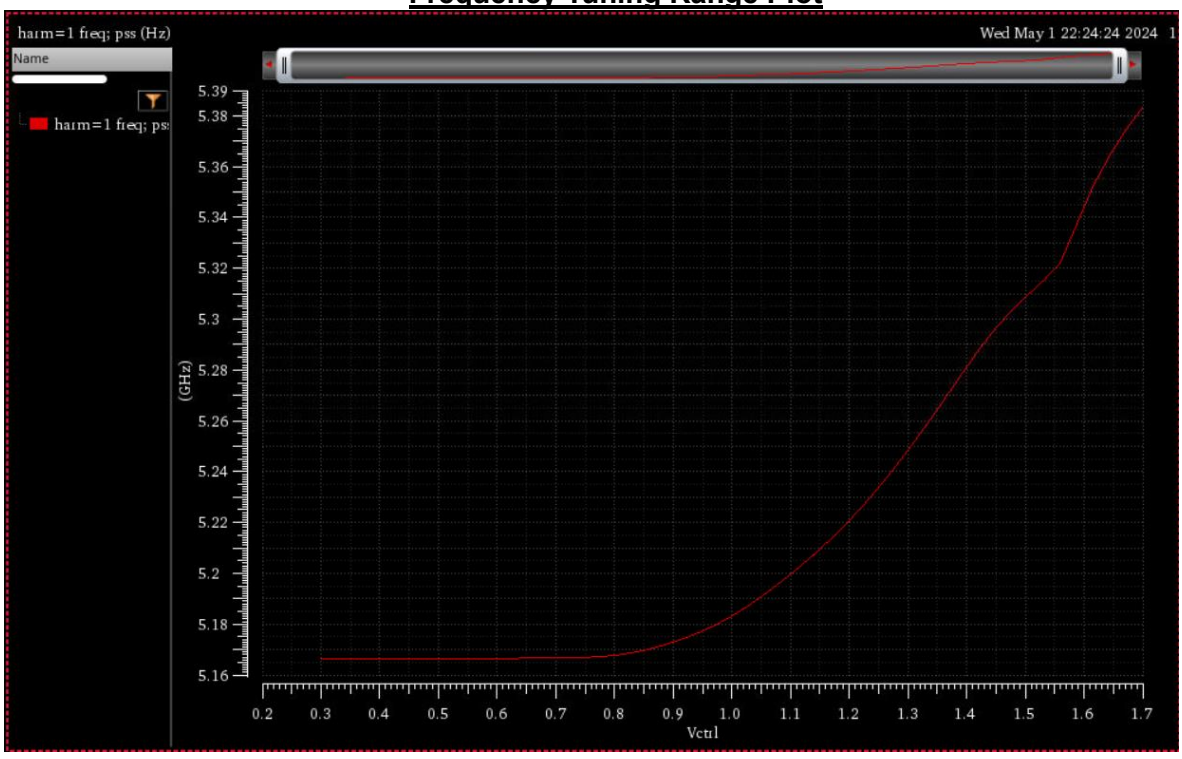
At 5.245 GHz



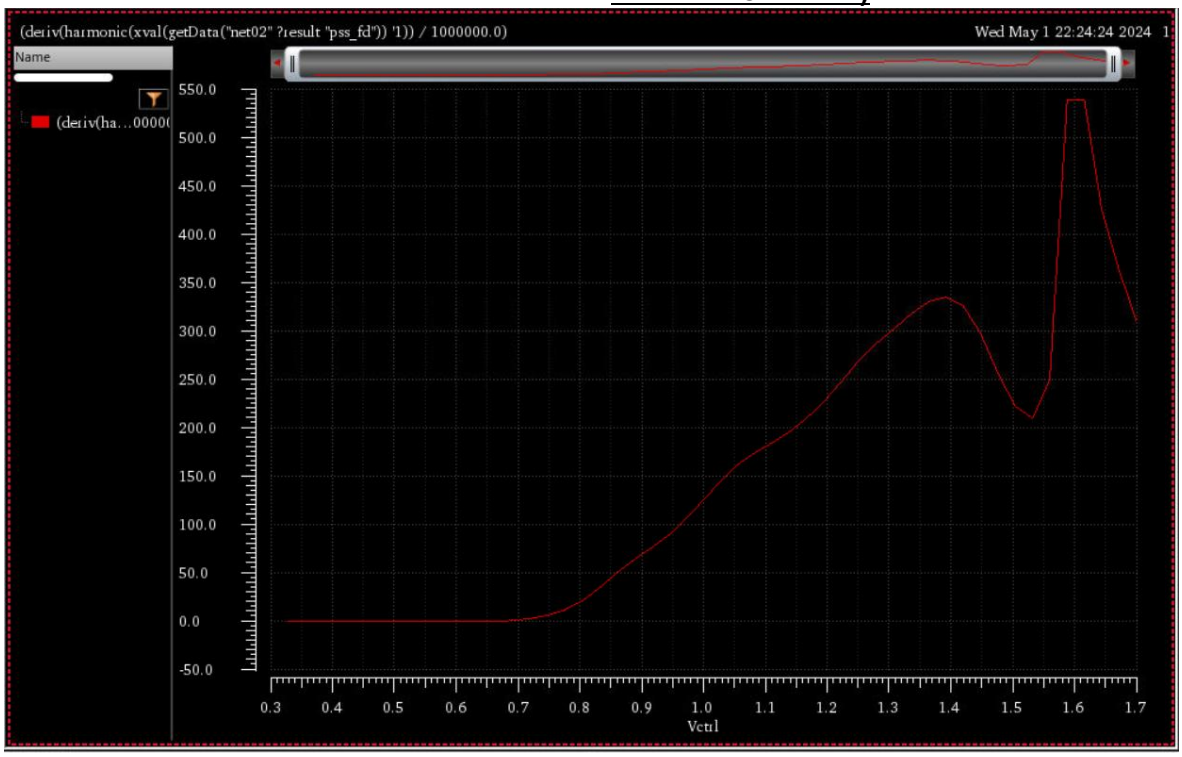
At 5.32 GHz



Frequency Tuning Range Plot

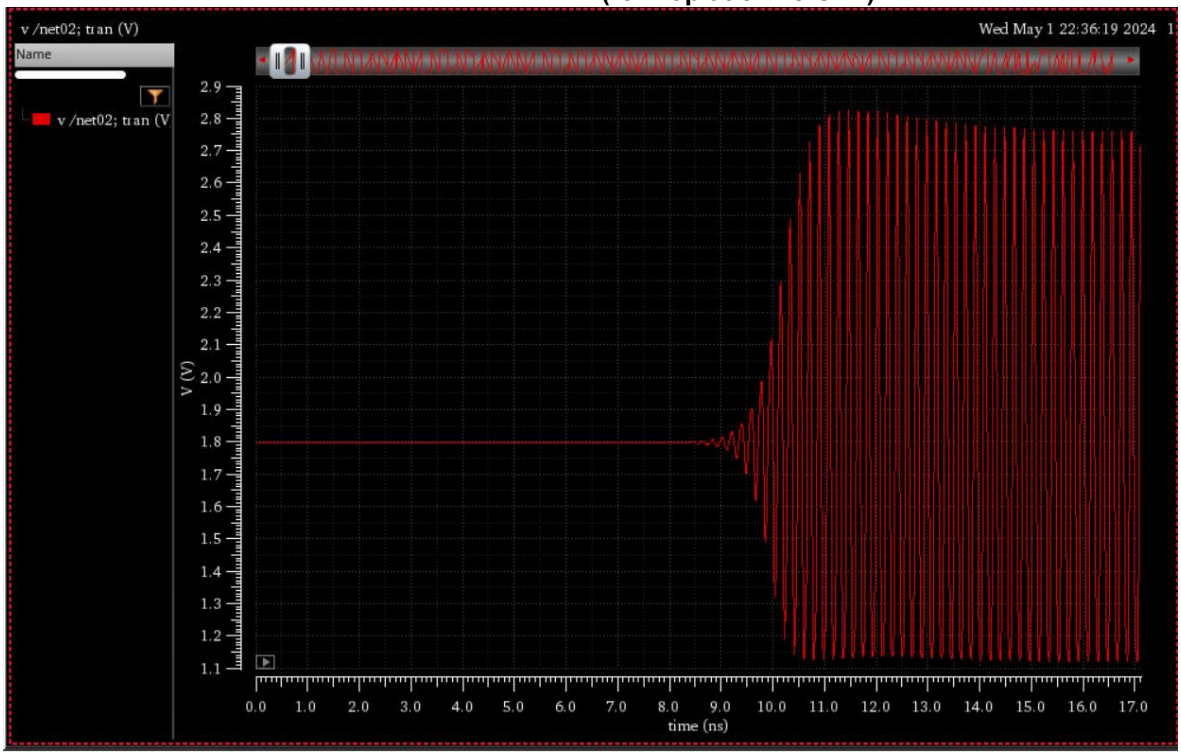


KVCO Plot (Average = 154.7 – Calculated using average function in Calculator**)**

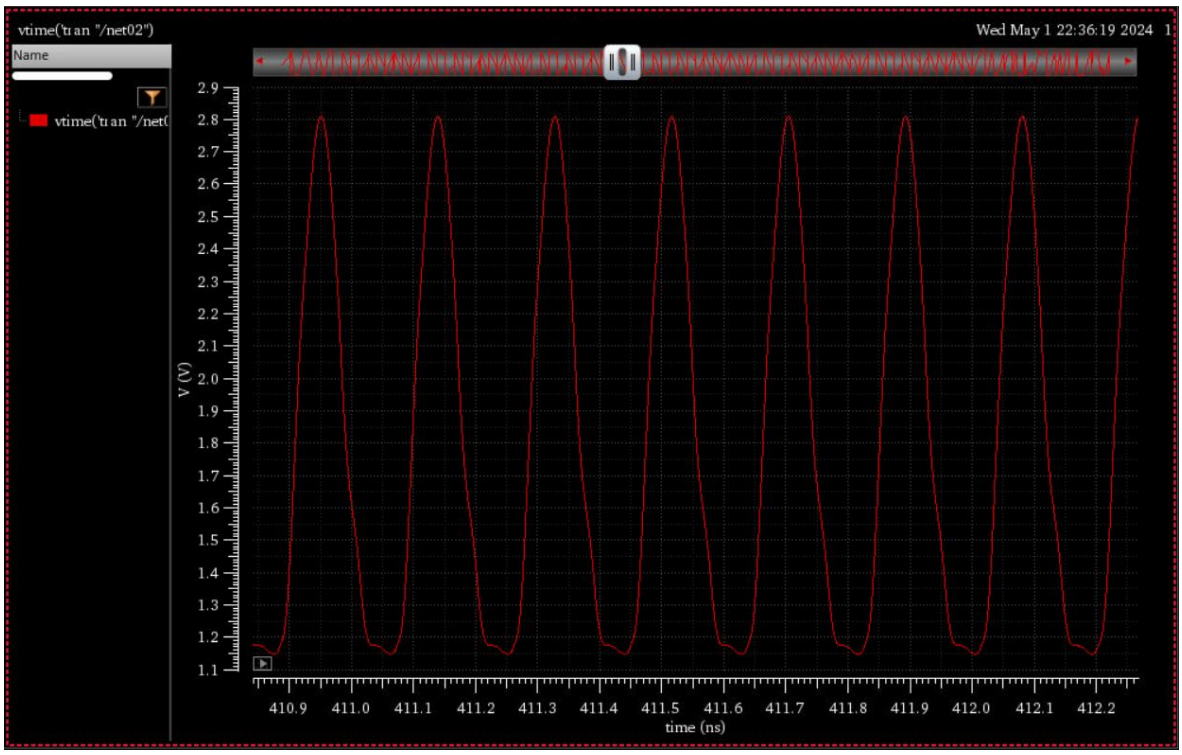


Initial Transient Response Plot

(for Vop at 5.245 GHz)

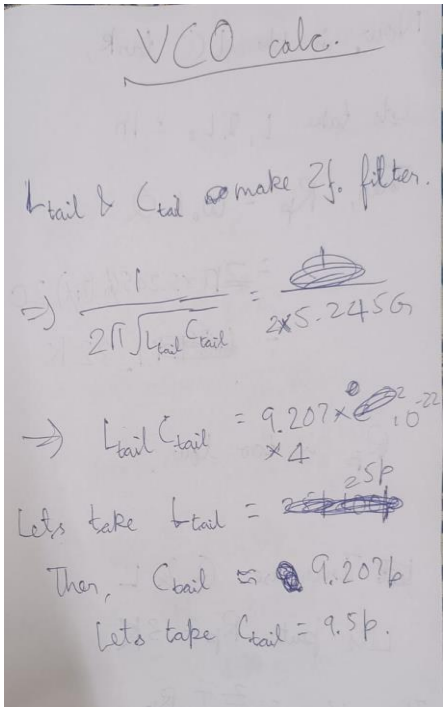


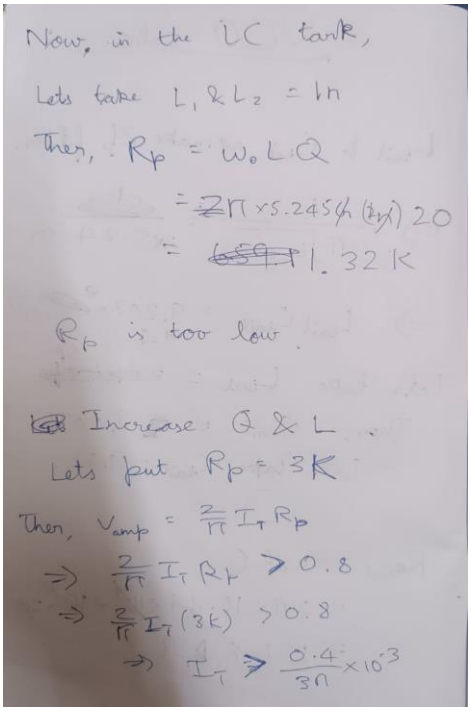
Single Ended Output Plot (Vop & Von) (at 5.245 GHz)

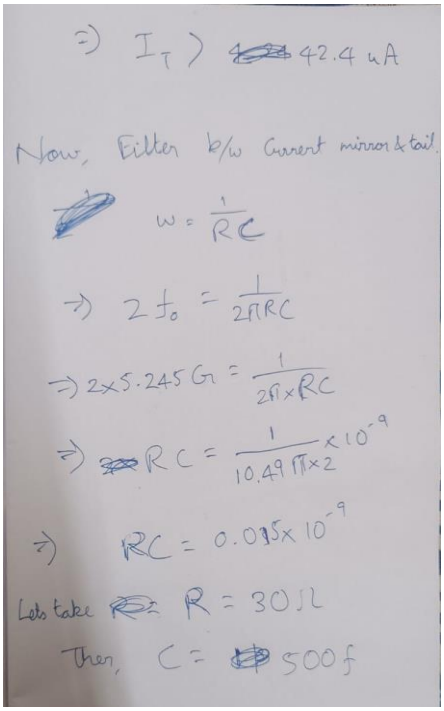


Design Procedure

- I calculated the values for the LC filter for 2f freq at the tail. Used those values.
- I used Rp at the drain = 3K. Based on that, calculated an approximate value for current needed for sin wave.
- The RC values needed for the filter of current mirror was also calculated.
- A I bias value of 100u was chosen and the W parameters of MOS were chosen based on that.
- A DC analysis was run to find the capacitance value of the Varactor of suitable lengths.
- A additional capacitance(Cadd) was added across two terminals to increase range and improve tuning.
- The inductor L value of the LC tank was determined based on this.
- As the tuning range was looking little less, I added one more level of a pair of varactors to increase it further. Then, I modified the connections of the varactor and connected the bulk to the ground instead of source.
- Tweaked the L, C parameters little bit to achieve the required tuning range and kVCO.
- The calculations needed for the filters mentioned above is attached below.







Path to Project Files

Path : home/ee21b103/cadence_project/RFIC_2024/vco_1