**EE6320 RF Integrated Circuits**

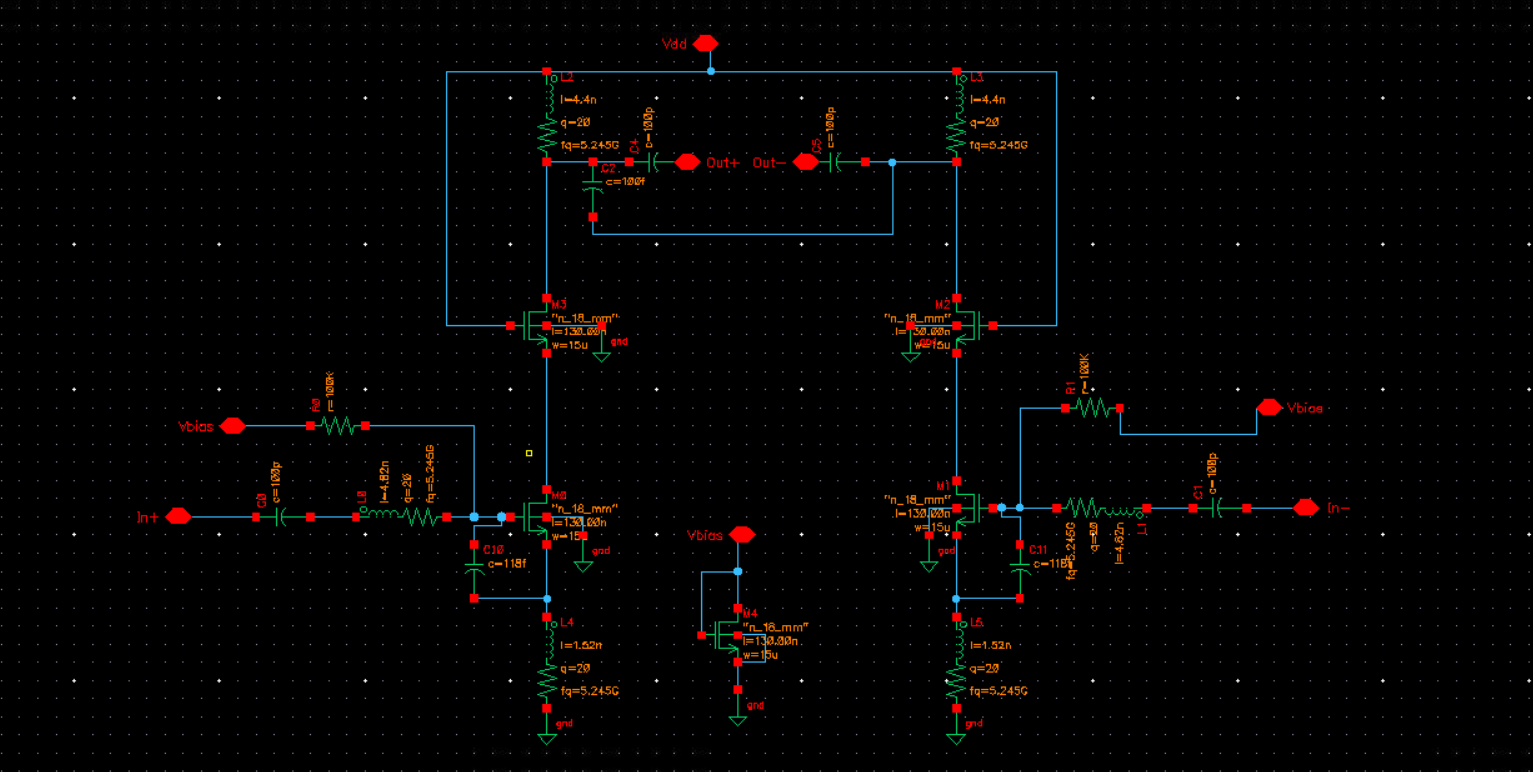
**Project: LNA Design**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Performance Summary Table** | |  |
| **Design metric** | **Measurement** | **Simulation Result** | **Requirement** |
| **Input matching** | Worst case S11 in the specified band | -13.35 | < −10dB |
| Band over which S11 ≤ −10dB | 4.989GHz – 5.929GHz | 5.17GHz to 5.32GHz |
| Band over which S11 ≤ −15dB | - | - |
| **Voltage Gain** | Minimum Gain in the specified band | 32.83 | ≥ 20dB |
| Maximum Gain in the specified band | 34.05 | ≥ 20dB |
| Gain flatness in specified band [Max-Min Gain] | 1.22 dB | ≤ 2dB |
| 3dB Bandwidth | 273MHz | - |
| Load Capacitance [Differential] | 100fF | 100f F |
| **Noise Figure** | Maximum Noise Figure in the specified band | 1.539 dB | ≤ 3dB |
| Minimum Noise Figure in the specified band | 1.52819 | - |
| Band over which NF ≤ 3dB | 3.69 GHz – 6.93 GHz | - |
| **Linearity** | IIP3 Tones used | 5.245G, 5.246G | - |
| Input power used for extrapolation | -70dB | - |
| Power of Fundamental Tone at output (at chosen input power) | -35.5 | - |
| Power of IM3 Tone at output (at chosen input power) | -162.3 | - |
| Extrapolated IIP3 | -6.532 | ≥ -10dBm |
| **Power** | LNA DC power consumption [Excluding Bias] | 742 uW | Minimize |
| Bias circuit power consumption (power supplied by i\_bias) | 158.9 uW | Minimize |
| **Other** | Sum of all on-chip inductances | 11.3n | - |
| Sum of all off-chip inductances (2 Lg's) | 9.64n | - |
| Sum of all resistances [Including bias] | 200K | - |
| Sum of all capacitances [Including AC coupling, excluding load] | 200.236p | - |
| Simulator Used | Spectre | - |

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**Roll No: EE21B103**

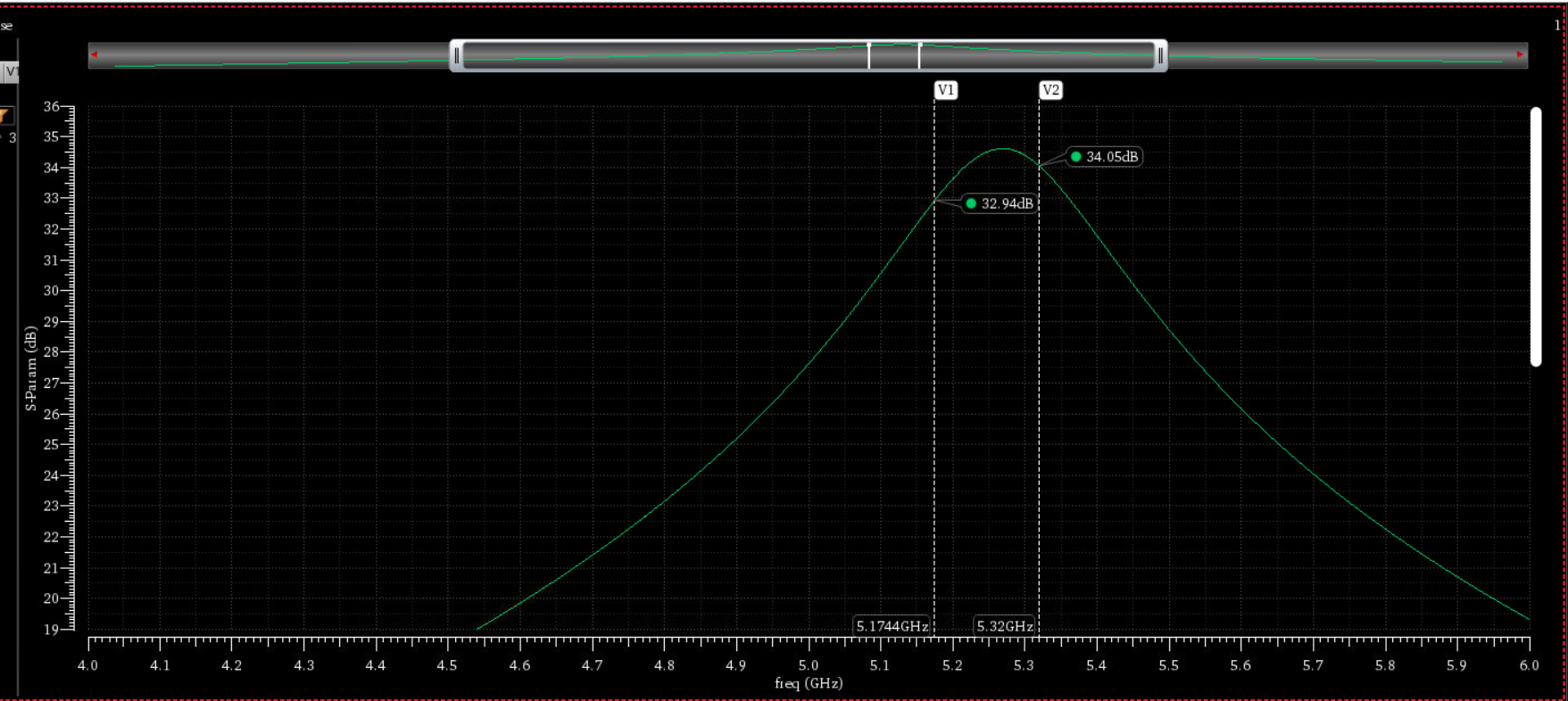
# LNA Schematic



|  |  |  |
| --- | --- | --- |
| **Component Values (one side values)** | | |
| **Design Component** | **Hand Calculated Value** | **Simulated Value** |
| **Lg (gate inductance)** | 4.82n | 4.82n |
| **Ls (source inductance)** | 1.52n | 1.52n |
| **Ld (drain inductance)** | 4.603n | 4.4n |
| **Rd\* (drain resistance)** | 3034.4 | 2966 |
| **R\_ls\* (res. parallel with Ls)** | 1007 | 1007 |
| **Rg\* (res. parallel with Lg)** | 3177 | 3177 |
| **Fixed Constant Parameters** | | |
| **● LNA MOS parameters: W = 15u M, L = 0.13u M** | | |
| **● Current Mirror MOS parameters: W = 15u M, L = 0.13u M** | | |
| **● I\_bias (current): 300u A** | | |
| **● C\_coupling: 100p each terminal** | | |

**\* - intrinsic resistance to respective inductors (doesn’t come in net resistance on/off the chip)**

**Gain (S21) Plot (only for representation)**



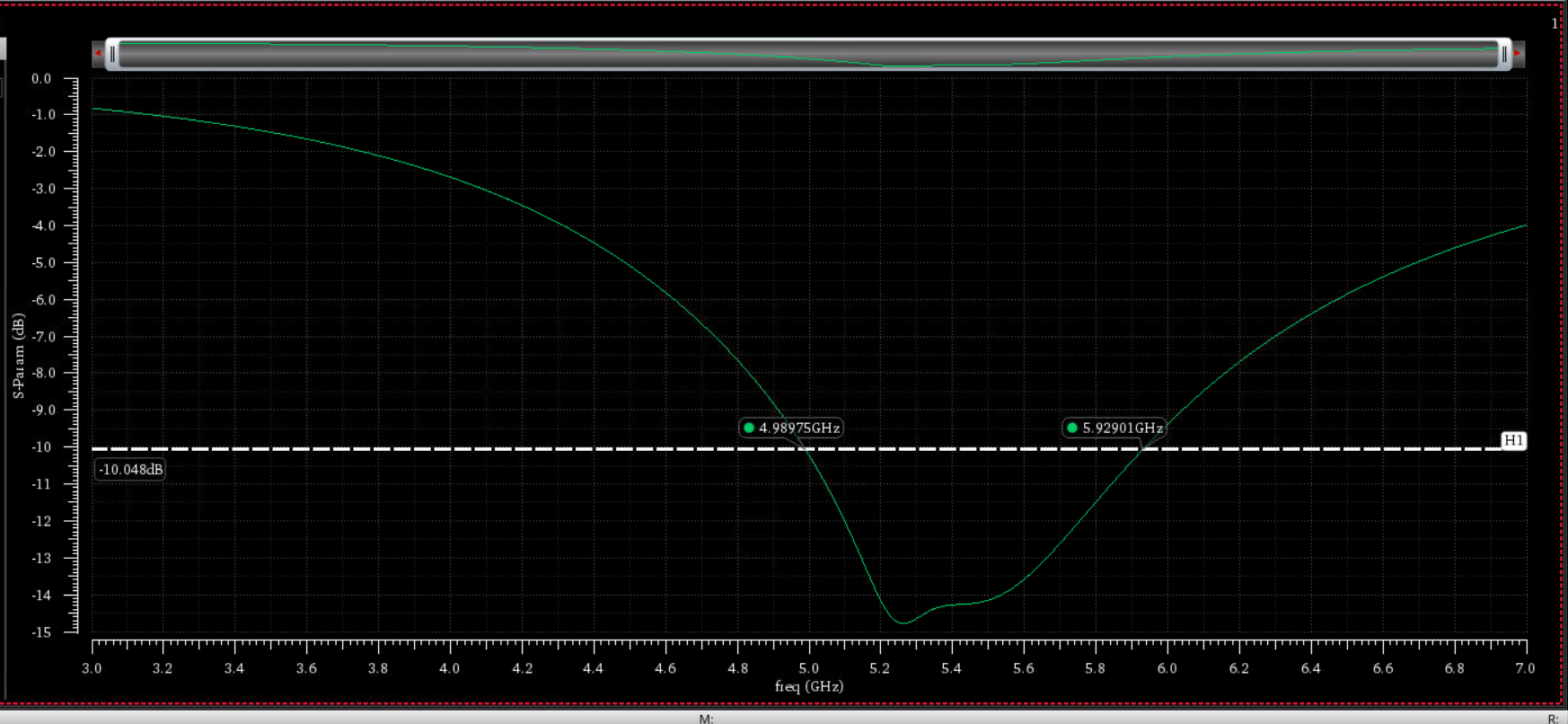
**Max Gain through hand calculation: <fill here>**

**Max Gain from the simulation: 34.62**

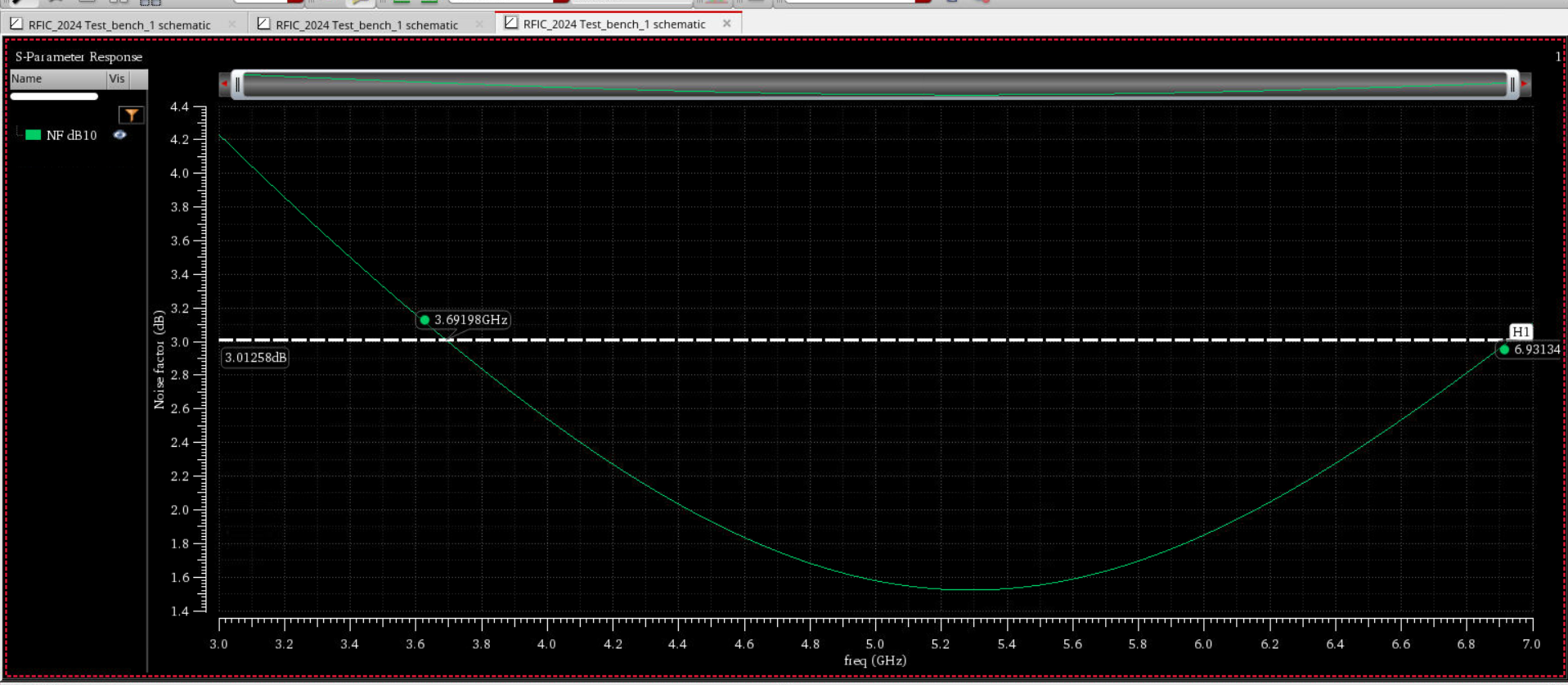
**-3dB Gain comes out to be: 31.62**

**From the figure, 3dB bandwidth comes out to be: 273 MHz**

**S11 Plot (only for representation)**



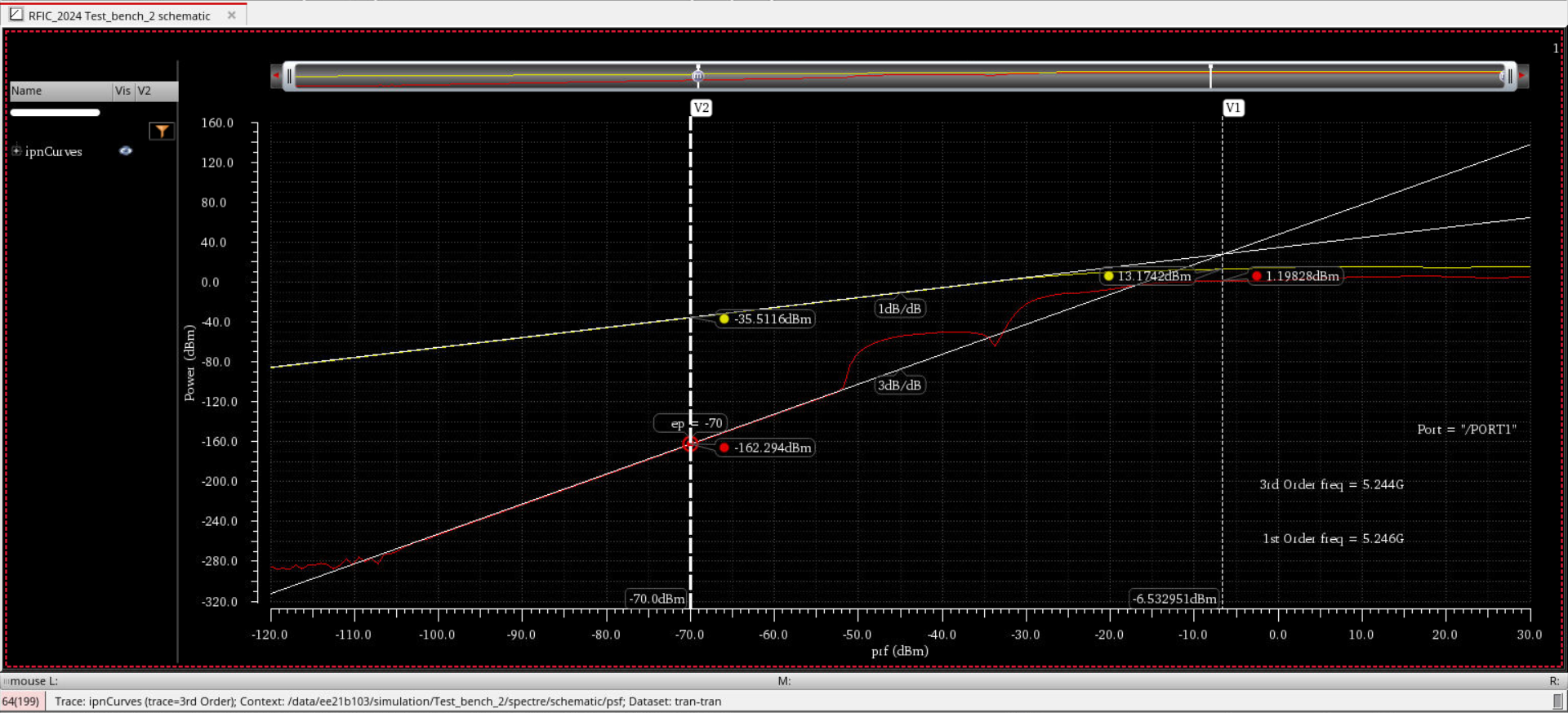
**NF Plot (only for representation)**



**From hand calculations, NF comes out to be: 1.902 dB**

**From the plot, NF comes out to be: 1.528 dB**

**Linearity Plot (IIP3 Computation) (only for representation)**

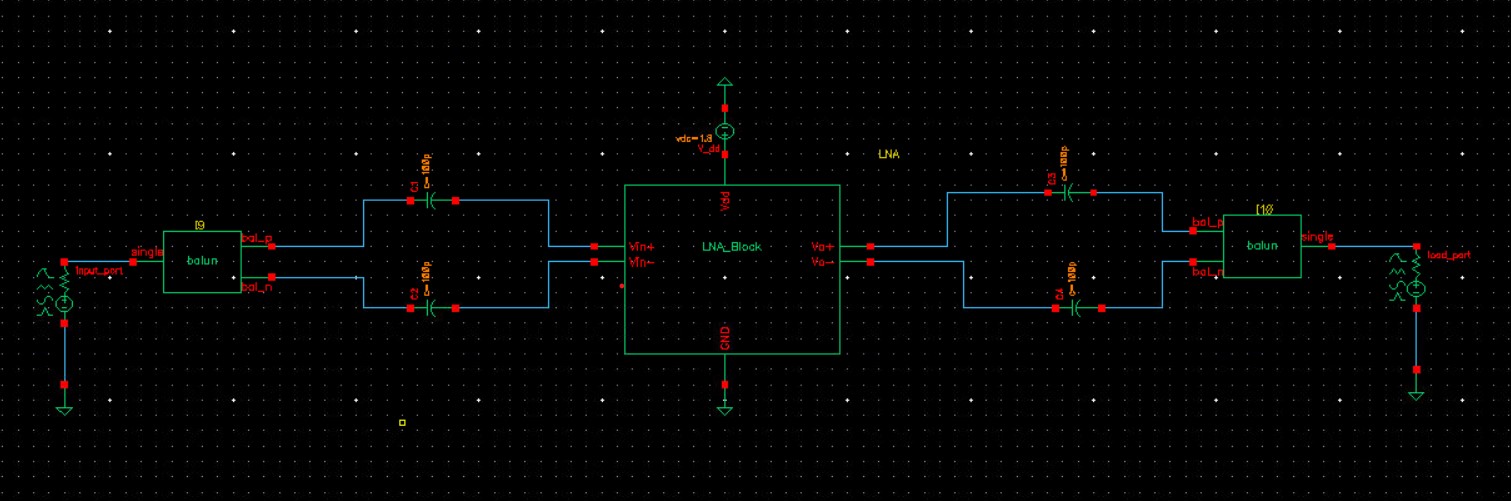


**Tones used: 5.245G, 5.246G**

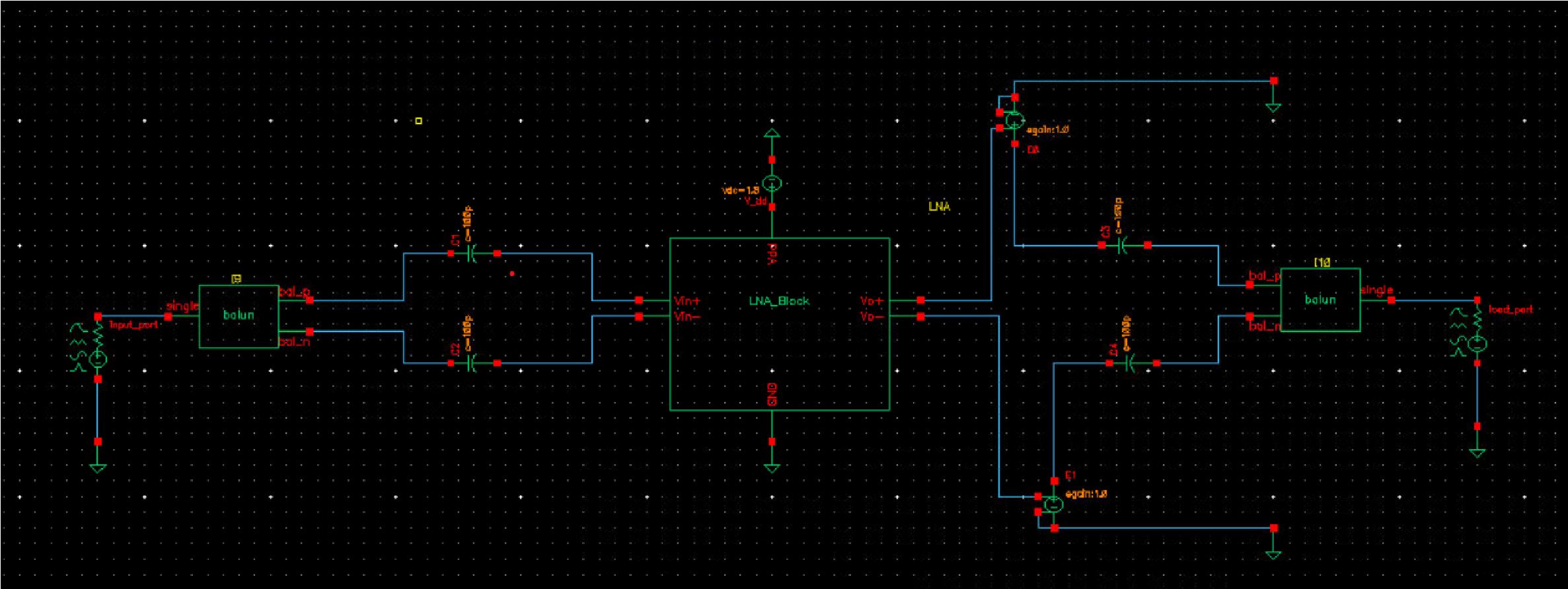
**IIP3 point comes out to be: -6.533 dB**

# LNA Testbench

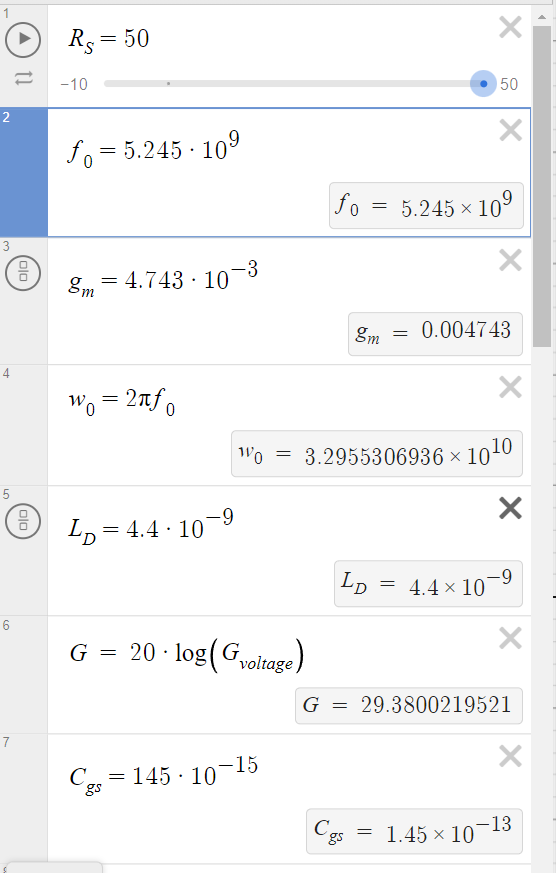
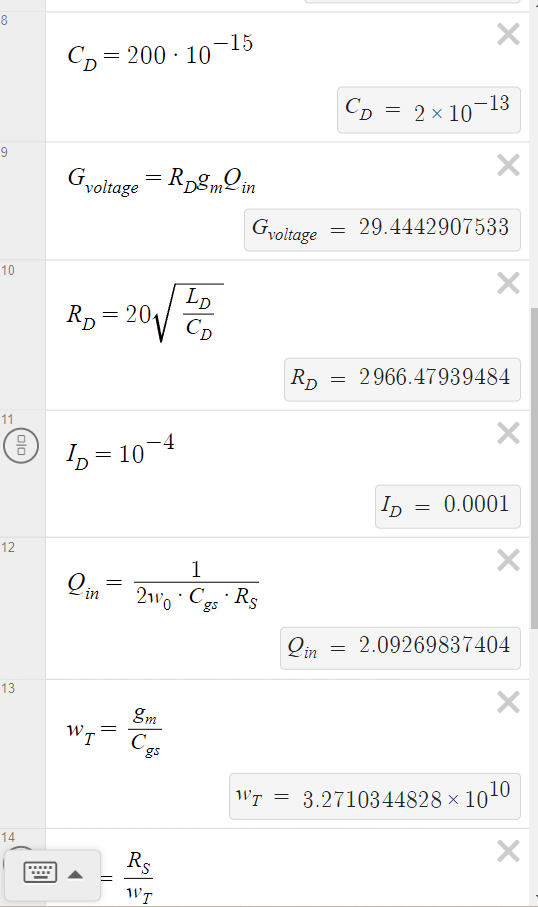
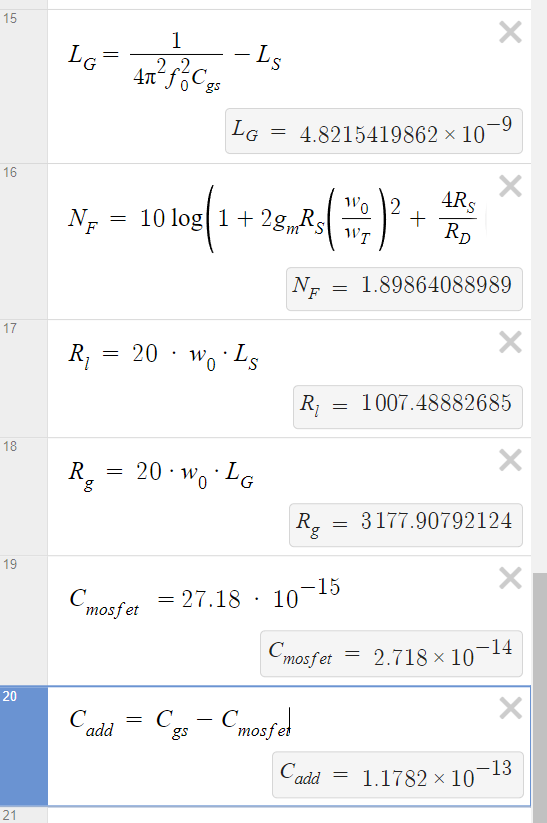
**This testbench is used to compute S11, NF, and IIP3 point.**



**This testbench is used to compute voltage gain (S21).**



**Hand Calculations done for the Project**

**  **

**Design Procedure**

* Made the schematic from the LNA help document
* Learnt about all the different analysis given there
* Approximately calculated some values and simulated using them
* Then got a good idea from them about the different parameters
* Then calculated all those values again rigorously from scratch
* Tweaked some of them slightly to get the required specifications.
* Got the required LNA amplifier.

# Note

**All the images put here (except the test benches) are only for representational purposes, i.e., do not use them as references for your spec values. Use this as a template to make the report (if you are making the report in docs); LaTeX reports are also fine, but maintain the structure as given here.**

**Path of the library:**

**Home/ee21b103/cadence\_project/RFIC\_2024**