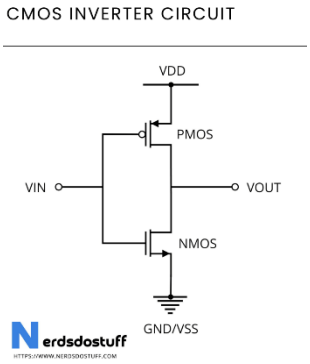
DAY3: REPORT:CMOS FUNDAMENTALS

1. CMOS Basics

CMOS (Complementary Metal Oxide Semiconductor) technology uses both NMOS and PMOS transistors to implement logic circuits. It is characterized by,

- Low static power consumption
- High noise immunity
- High packing density
- Scalable with technology

CMOS Inverter Structure:



PMOS at top (pull-up network)

NMOS at bottom (pull-down network)

Output taken from common drain

Only one transistor conducts in steady state

2. MOSFET Operation Principles

Modes of Operation for NMOS

Region	**Condition**	**State**
Cutoff	VGS < Vth	Transistor OFF
Linear	VGS > Vth and VDS < (VGS − Vth)	Acts like a resistor
Saturation	VGS > Vth and VDS ≥ (VGS − Vth)	Acts like a current source

Same applies to PMOS with polarities reversed

3. V–I Characteristics of MOSFET

Linear Region Current

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Saturation Region Current

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

Where:

- μ = carrier mobility
- Cox = oxide capacitance
- W/L = transistor aspect ratio

4. Channel Length Modulation (CLM)

- In saturation, drain current slightly increases with VDS
- Effective channel length reduces
- Similar to Early effect in BJT

Modified Saturation Current

$$I_D = I_{Dsat}(1 + \lambda V_{DS})$$

Effect:

- Reduces output resistance
- Degrades analog gain

5. Body Effect

- Occurs when source nor equal to substrate voltage
- Threshold voltage increases

Threshold Voltage with Body Effect

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

Impact:

- Reduced drive current
- Slower circuits

6. Technology Evolution

Scaling Goals

- Higher speed

- Lower power
- Higher density

Scaling Challenges

- Short channel effects
- Leakage currents
- Variability
- Heat dissipation
- Interconnect delay

7. FinFET vs Planar CMOS

Aspect	**MOSFET**	**FinFET**
Structure	Planar	Three dimensional or fin structure
Gate Control	Voltage controlled conductivity	Voltage controlled gate width
Leakage Current	Higher leakage current	Lower leakage current
Power Efficiency	Relatively lower	Improved power efficiency
Speed & Performance	Moderate speed	Faster speed
Transistor Capacitance	Higher	Reduced
Scalability	Limited scalability in smaller process nodes	Better scalability in smaller process nodes
Integration	Limited integration capability	Improved integration capability
Manufacturing Process	Relatively simpler manufacturing process	More complex manufacturing process
Cost	Lower manufacturing cost	Higher manufacturing cost
Applications	Wide range of applications	Similar range of applications as MOSFET
Future Trends	Limited potential for future improvements	Further potential for development

8. BiCMOS Technology

BiCMOS = CMOS + BJT

Advantages

- High speed (BJT)
- Low power (CMOS)
- High drive capability

Applications

- Analog circuits
- RF circuits
- High-speed I/O

9. CMOS Inverter Characteristics

Voltage Transfer Characteristic (VTC)

- Shows relationship between Vin and Vout
- Defines switching behavior

Key Parameters

- VOH: Output high voltage
- VOL: Output low voltage
- VIL / VIH: Input thresholds
- VM: Switching threshold

10. Noise Margins

$$NM_H = VOH - VIH$$

$$NM_L = VIL - VOL$$

Higher noise margin means Better reliability

11. Propagation Delay

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

Where:

- tPLH = Low → High delay
- tPHL = High → Low delay

Depends on:

- Load capacitance
- Drive strength
- Supply voltage

12. Power Dissipation in CMOS

Dynamic Power

$$P_{dyn} = \alpha C_L V_{DD}^2 f$$

Static Power

$$P_{static} = I_{leak} \times V_{DD}$$

Leakage Mechanisms

- Subthreshold leakage
- Gate oxide tunneling
- Junction leakage

13. Power Optimization Techniques

- Voltage scaling
- Clock gating
- Power gating
- Multi-Vth cells
- Transistor sizing

14. Layout Effects

Parasitics

- Parasitic capacitance
- Parasitic resistance

Proximity Effects

- Well proximity effect (WPE)
- Length of diffusion effect (LOD)

Matching Techniques

- Common centroid
- Interdigitated layout
- Dummy devices

15. Thermal Effects

- Mobility decreases with temperature
- Leakage increases
- Reliability issues (electromigration)

16. Analog Building Blocks

Current Mirrors

- Copy current from reference branch
- Accuracy depends on matching

Types:

- Simple mirror
- Cascode mirror
- Wilson mirror

Differential Amplifier

- Amplifies difference between two inputs
- Rejects common-mode signals

Key parameters:

- Differential gain
- CMRR
- Input common-mode range

Operational Amplifier Fundamentals

- High gain

- High input impedance
- Low output impedance

Key specs:

- Gain
- Bandwidth
- Phase margin
- Slew rate
- Stability

17. Gain, Bandwidth & Stability

- Gain-bandwidth product (GBW) is constant
- Phase margin > 45° preferred
- Compensation required for stability

Conclusion

- CMOS inverter is the foundation of digital VLSI
- Device physics strongly impacts performance
- Layout and parasitics are critical in nanometer nodes
- Analog blocks rely heavily on matching and biasing