DAY2: REPORT

Timing Concepts in Digital Design

1. Single-Cycle Path

- Data launched from FF1
- Captured by FF2 in same clock cycle
- Must satisfy:Clock period ≥ combinational delay + setup time
- Most common timing assumption
- Limits max clock frequency
- Used when operation is simple and fast

2. Multi-Cycle Path

- Data allowed to take more than 1 clock cycle
- Capture after N cycles
- Used for:Complex arithmetic & Non-critical operations
- Timing constraint is relaxed
- Improves timing without changing hardware

Single vs Multi Cycle

- Single-cycle for fast but strict timing
- Multi-cycle for slower but easier timing closure

3. False Paths

- Timing paths that never occur in real operation
- Exist structurally but not functionally
- Example: Mutually exclusive control signals & Mode-dependent logic
- Avoid false timing violations ,Prevent unnecessary optimization& Faster and accurate timing analysis
- Tools should ignore these paths

4. Critical Path

- Longest delay path in the design
- Determines:Maximum clock frequency
- If violated causes timing failure

5. Reducing Critical Path Delay

(a) Pipelining

- Insert registers in long combinational logic
- Break path into stages
- Higher clock frequency
- More latency

(b) Logic Simplification

- Reduce logic depth
- Simplify Boolean equations
- Remove unnecessary conditions
- Use efficient RTL coding

(c) Parallelism

- Perform independent operations together
- Avoid long sequential logic

(d) Good RTL Coding

- Avoid deep nested if–else
- Use registers wisely
- Match design to hardware resources

Conclusion:

Correct timing constraints & clean RTL means High-performance and reliable design