CSE 420: Assignment 2

1) Consider this command:

./sim-outorder -cache:il1 il1:64:64:16:s -cache:dl1 dl1:64:64:16:s

Here, this represents the configuration of L1 instruction and data cache where il1 - L1 instruction and dl1 - L1 data cache. The options are:

64 sets, block size is 64 bytes, 16 way set associative cache, SRRIP policy(s).

The different cache replacements policies are:

LRU - l FIFO- f Random - r PLRUt - t (Added as a part of the assignment)

SRRIP - s (Added as a part of the assignment)

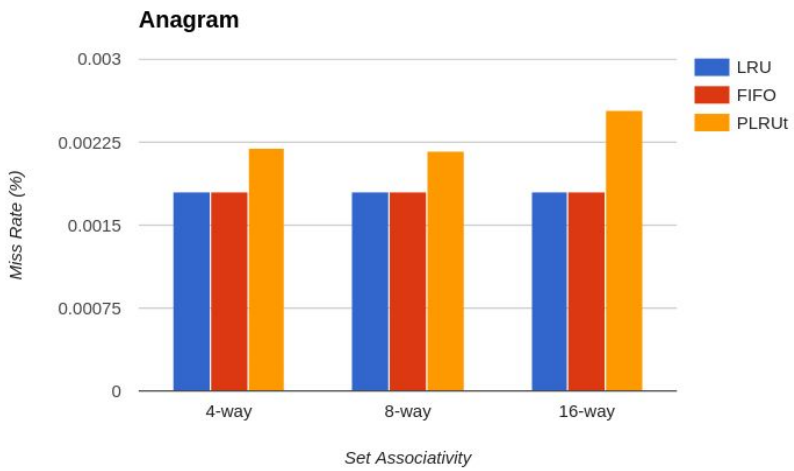
Cache simulation in SimpleScalar:

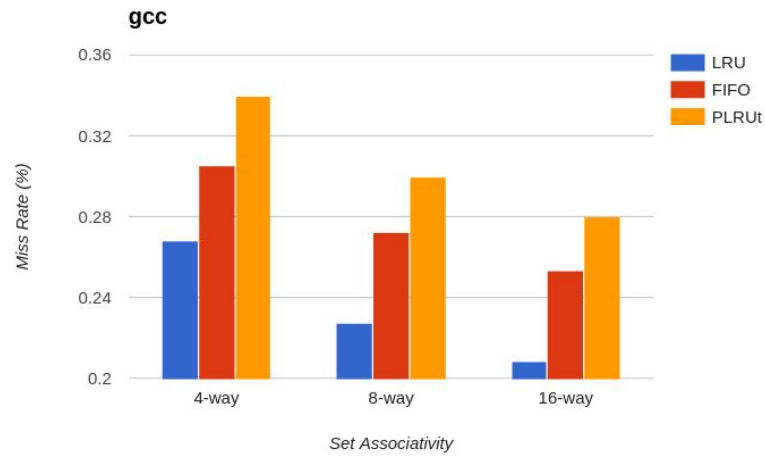
The cache structure is initialised. Whenever there is a load or store operation (for data cache) and for all the instructions (instruction cache), then the control goes to the function '*unsigned int cache_access()*'. Here:

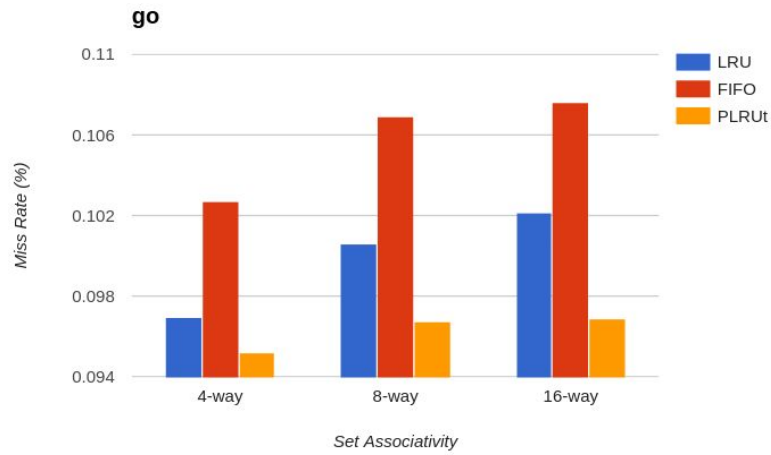
1. Based on the cache configuration, we get the tag, index and byte_offset from the PC (program counter) of that instruction.
2. We check the tag bits at the index specified by PC and if the tag is found, then it is a cache hit and the control goes to cache hit handling and the hit counter is incremented.
3. Else the control goes to cache miss handling at the switch statement *switch(cp->policy)*.
4. In case of conflict misses, an appropriate cache line is evicted based on the cache replacement policy that is specified in the command line argument. In case of compulsory miss, the available cache line is filled with the required data and miss counter is incremented.

2) L1 Instruction Cache Miss rate comparison: (Miss Rate values are in percentages)

	Anagram			Gcc			Go		
Set Associativity	**LRU**	**FIFO**	**PLRUt**	**LRU**	**FIFO**	**PLRUt**	**LRU**	**FIFO**	**PLRUt**
4-way	0.001808457	0.001808453	0.002200651	0.267799535	0.305348032	0.339470041	0.096913725	0.102684384	0.095213485
8-way	0.001808457	0.001808453	0.002167966	0.227671261	0.272083397	0.299615289	0.100569193	0.106943466	0.096723597
16-way	0.001808457	0.001808454	0.002541991	0.208210853	0.253559457	0.28000001	0.10216287	0.107595212	0.096891792

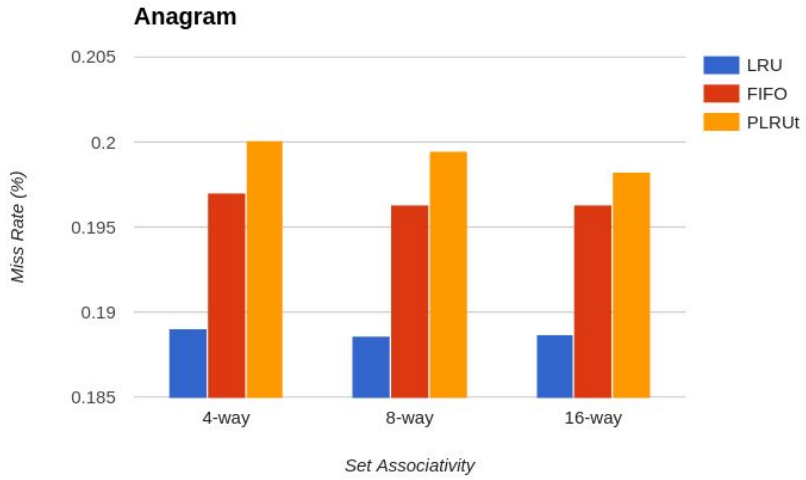


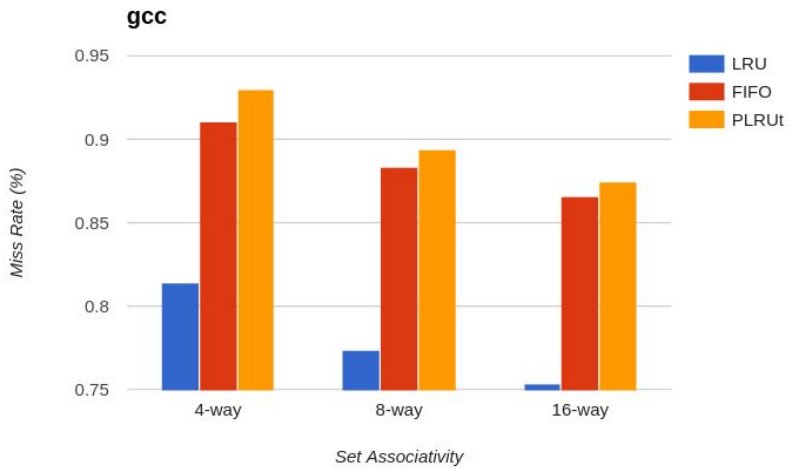


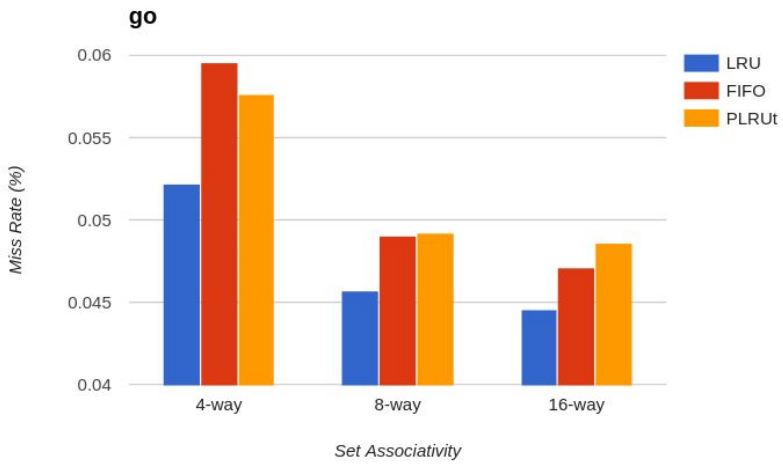


L1 Data Cache Miss rate comparison: (Miss Rate values are in percentages)

	Anagram			Gcc			Go		
Set Associativity	**LRU**	**FIFO**	**PLRUt**	**LRU**	**FIFO**	**PLRUt**	**LRU**	**FIFO**	**PLRUt**
4-way	0.189065346	0.196991836	0.200101655	0.813655935	0.910598701	0.929517959	0.052232267	0.05952973	0.057664407
8-way	0.188635206	0.196275355	0.199484997	0.773959002	0.88319868	0.893713307	0.045695546	0.049005512	0.049194758
16-way	0.188668365	0.196341075	0.198259502	0.753944693	0.865993629	0.874135839	0.044599888	0.047112814	0.048567544

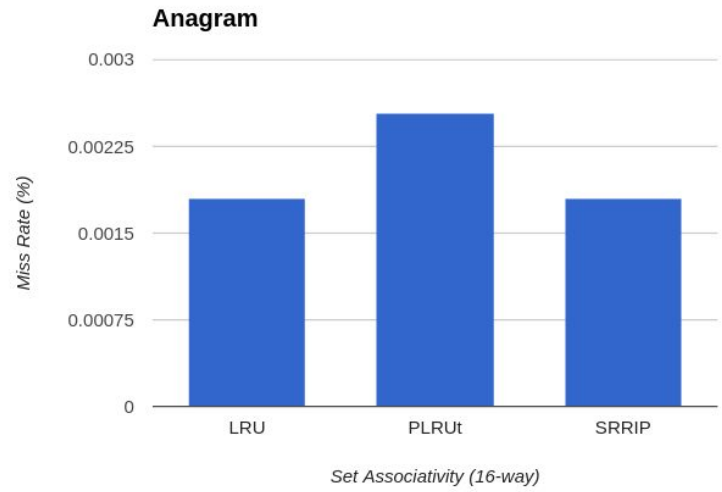


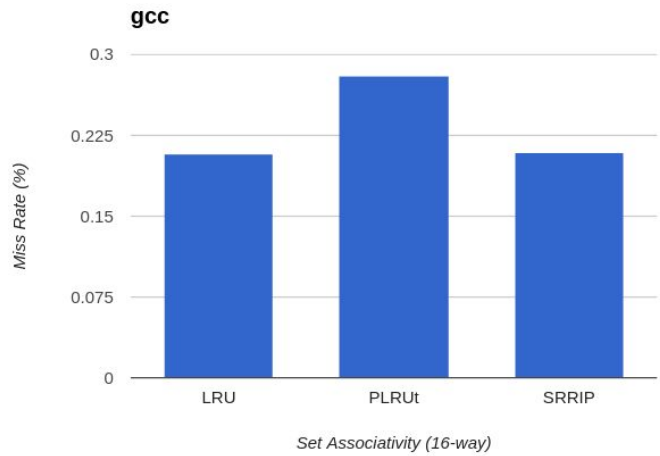


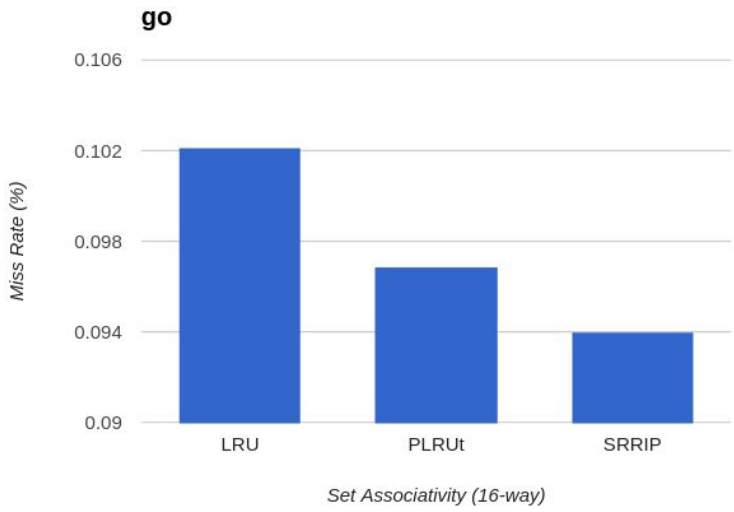


L1 Instruction Cache Miss rate comparison: (Miss Rate values are in percentages)

	Anagram			Gcc			Go		
Set Associativity	**LRU**	**PLRUt**	**SRRIP**	**LRU**	**PLRUt**	**SRRIP**	**LRU**	**PLRUt**	**SRRIP**
16-way	0.001808457	0.002541991	0.001808457	0.208210853	0.28000001	0.209535196	0.10216287	0.096891792	0.093975852

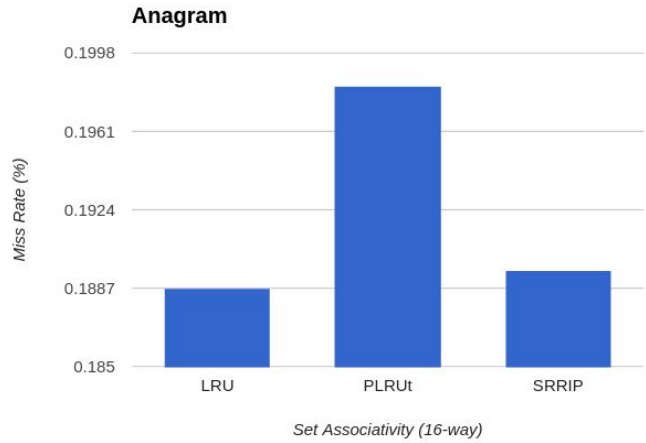


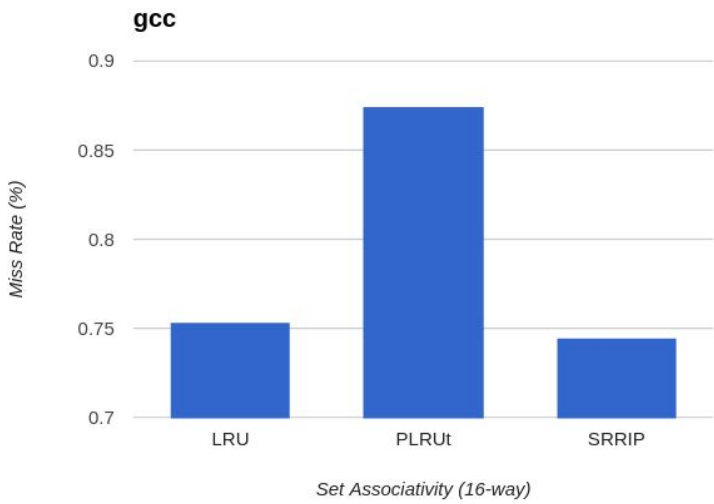


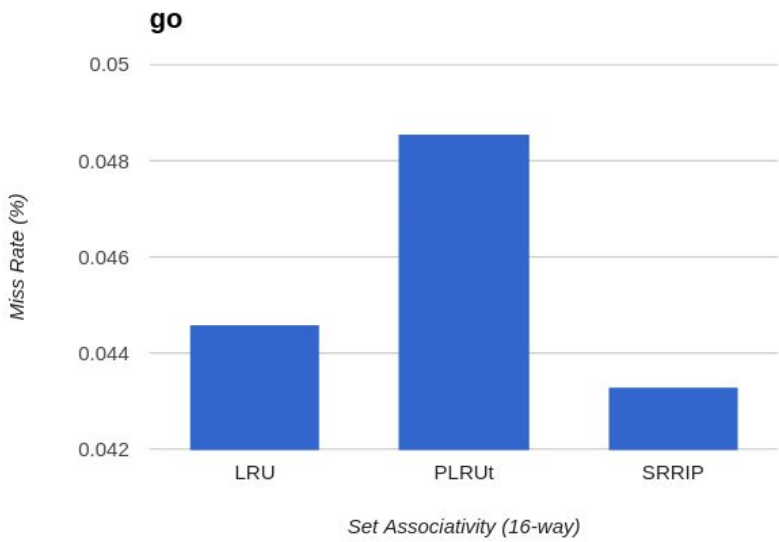


L1 Data Cache Miss rate comparison: (Miss Rate values are in percentages)

	Anagram			Gcc			Go		
Set Associativity	**LRU**	**PLRUt**	**SRRIP**	**LRU**	**PLRUt**	**SRRIP**	**LRU**	**PLRUt**	**SRRIP**
16-way	0.188668365	0.198259502	0.189528271	0.753944693	0.874135839	0.745093705	0.044599888	0.048567544	0.04328244


Anagram
0.1998
0.1961
0.1924
0.1887
0.185
Miss Rate (%)
LRU
PLRUt
SRRIP
Set Associativity (16-way)


gcc
0.9
0.85
0.8
0.75
0.7
Miss Rate (%)
LRU
PLRUt
SRRIP
Set Associativity (16-way)


go
0.05
0.048
0.046
0.044
0.042
Miss Rate (%)
LRU
PLRUt
SRRIP
Set Associativity (16-way)