ECE 585: MICROPROCESSORS SYSTEM DESIGN

Fall 2021

Final Project

DRAM Memory Controller

Group 35

Prepared by

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1. Introduction

- In this project, we have simulated a DRAM memory controller using System Verilog Programming Language.
- It can serve the shared last level cache of a four core 3.2 GHz processor employing a single memory channel.
- The system uses a relaxed consistency (XC) model. The memory channel is populated by a single-ranked 8GB PC4-25600 DIMM (constructed with memory chips organized as x8 devices with a 1KB page size and 24-24-24 timing). There is no ECC.

2. Design Attributes

A. Address Mapping

Given are the details about the DIMM and processor:

- 4 core 3.2 GHz processor employing Single memory channel
- Single rank 8GB PC4-25600 DIMM
- DIMM had 8 SDRAM chips and No ECC
- Memory chips are organized as by x8 devices with 2KB page size

a. Calculating the column bits from Page Size

Page size(byte) = (Number of Columns * Internal access size)/8

2KB = (N*64 bits)/8

$N = 2^8 = 256$

Column bits = 8

b. We must assume the bank group and bank bits. We will assume it to be 2 bits each.

Now the DIMM has a capacity of 8GB. The SDRAM capacity of each one would be 8Gib (chip capacity expressed in bits). Now we can calculate the number of row bits

DRAM Capacity = Number of Rows * Number of high Columns * Number of bank groups * Number of banks * Access width * Low column access bits

8Gib = Number of rows * 256 * 4 * 4* 8 * 8

Number of rows = $(8 * 2^{30})/ (2^{18}) = 2^{18}$

Row bits = 15

Address Mapping

35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNUSED			ROW																HIGH COLUMNS							BANK		BANK GROUP		BURST INDEX			BYTE SELECT		

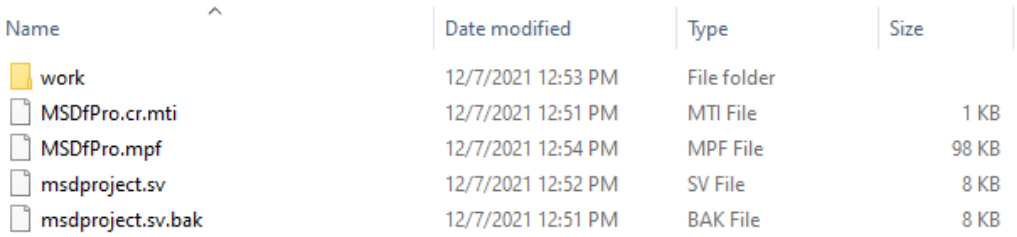
- Bits [35:33] are not used
- Bits [32:17] are used for Row Select
- Bits [16:10] are used for high Column MSB select
- Bits [9:8] are used for Bank Select
- Bits [7:6] are used for Bank Group Select
- Bits [5:3] are used for low Column LSB to select the burst order
- Bits [2:0] are byte select (not used here)

As we are using Open Page Policy, we chose the mapping described above. The advantage of this mapping is that it makes accessing different columns of different banks and bank groups much easier in the same row. It also allows the control of burst order.

We have followed in-order scheduling of memory requests without bank parallelism

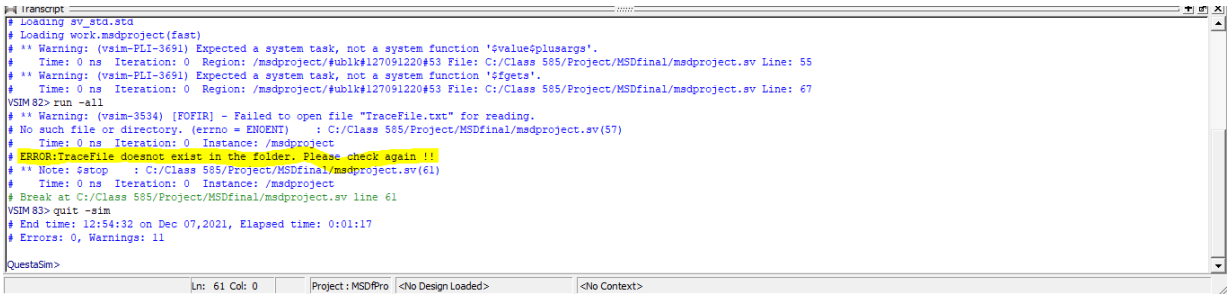
3. Testing (Some more testcases are present in the testcases folder)

a. TraceFile is not present in the folder

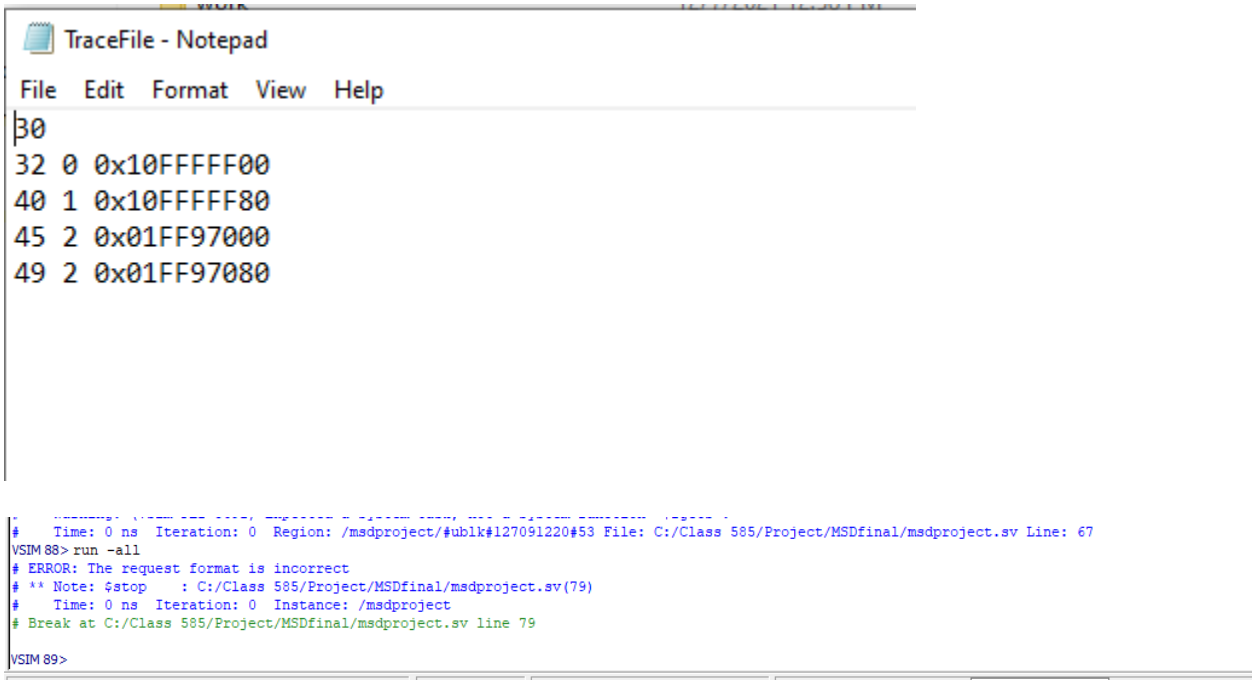


Name	Date modified	Type	Size
work	12/7/2021 12:53 PM	File folder	
MSDfPro.cr.mti	12/7/2021 12:51 PM	MTI File	1 KB
MSDfPro.mpf	12/7/2021 12:54 PM	MPF File	98 KB
msdproject.sv	12/7/2021 12:52 PM	SV File	8 KB
msdproject.sv.bak	12/7/2021 12:51 PM	BAK File	8 KB

Error Message displayed in Transcript

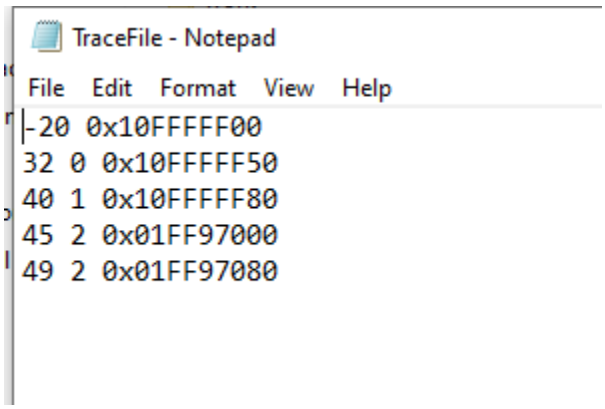


b. TraceFile request format is incorrect



c. Opcode is greater than 2

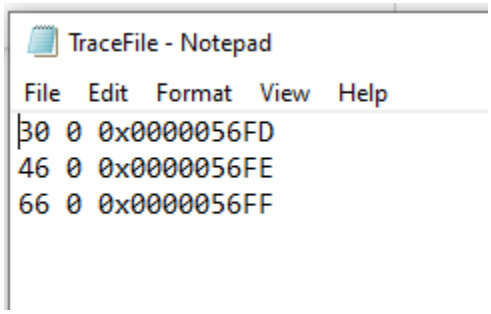
d. Request Time is not correct

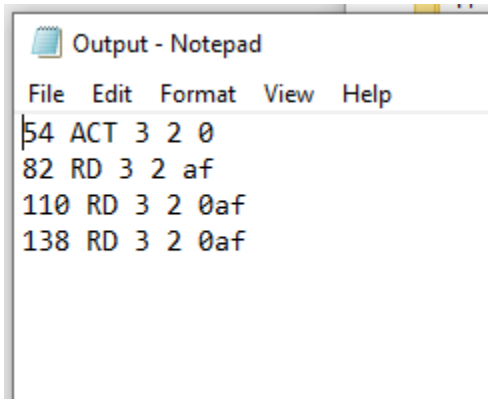



```
VSIM 94> run -all
# ERROR: The request format is incorrect please check your cputime '{cputime:-20, opcode:0, mem_address:4563402496, counter:0}
# ** Note: $stop    : C:/Class 585/Project/MSDfinal/msdproject.sv(84)
#    Time: 0 ns  Iteration: 0  Instance: /msdproject
# Break at C:/Class 585/Project/MSDfinal/msdproject.sv line 84

VSIM 95>
```

e. All Read Requests to Same Bank, same BankGroup





f. All write Requests to Same Bank, Same BankGroup

TraceFile - Notepad

File Edit Format View Help

```
30 1 0x0000026FD
46 1 0x0000026FE
66 1 0x0000026FF
```

Output - Notepad

File Edit Format View Help

```
54 ACT 3 2 0
78 WR 3 2 4f
102 WR 3 2 04f
126 WR 3 2 04f
```

g. Request to same different banks and different bank groups

TraceFile - Notepad

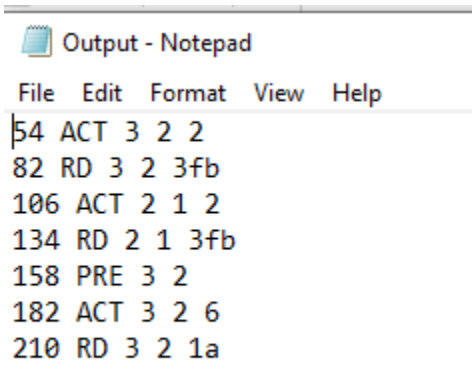
File Edit Format View Help

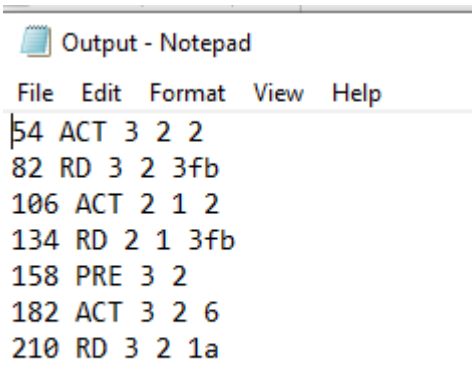
```
30 0 0x00005FED8
46 0 0x00005FD98
52 0 0x0000C0ED2
```

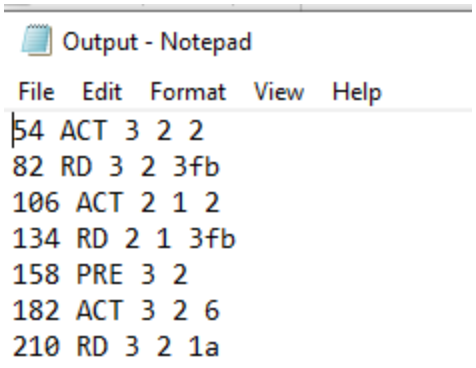
Output - Notepad

File Edit Format View Help

```
54 ACT 3 2 2
82 RD 3 2 3fb
106 ACT 2 1 2
134 RD 2 1 3fb
158 PRE 3 2
182 ACT 3 2 6
210 RD 3 2 1a
```


Output - Notepad
File Edit Format View Help
54 ACT 3 2 2
82 RD 3 2 3fb
106 ACT 2 1 2
134 RD 2 1 3fb
158 PRE 3 2
182 ACT 3 2 6
210 RD 3 2 1a


Output - Notepad
File Edit Format View Help
54 ACT 3 2 2
82 RD 3 2 3fb
106 ACT 2 1 2
134 RD 2 1 3fb
158 PRE 3 2
182 ACT 3 2 6
210 RD 3 2 1a


Output - Notepad
File Edit Format View Help
54 ACT 3 2 2
82 RD 3 2 3fb
106 ACT 2 1 2
134 RD 2 1 3fb
158 PRE 3 2
182 ACT 3 2 6
210 RD 3 2 1a