HDL Assignment 1: FULL Adder Circuit

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Code:

Test code:

testbench.sv

SV/Verilog Testbench

```
module test; //By Vanteddu Thanishq
  //S20200020311, HDL
    reg A,B,C; //inputs A,B,C
    wire Sum,Carry;  //Outputs Sum and Carry
  fulladder dut(A, B, C, Sum, Carry);
  initial
  begin
    A=1'b0; //Defining A = 0 at initial
    #40 A=1'b1;
    #40 $finish;
  end
  initial
  begin
    B=1'b0; //Defining and initiating input B
    #20 B=~B;
    #20 B=~B;
    #20 B=~B;
    #20 $finish;
  end
  initial
    begin
      C=1'b0;  //DEfining and Initiating input C
      #10 C=1'b1;
      #10 C=1'b0;
      #10 C=1'b1;
      #10 C=1'b0;
      #10 C=1'b1;
      #10 C=1'b0;
      #10 C=1'b1;
      #10 $finish;
    end
  initial
    begin
      $monitor($time," A = %d", A , " B= %d" , B," C= %d",C," SUM
= %d", Sum , "  CARRY = %d" , Carry);
    end

endmodule
```

Design Code:

design.sv

```
module fulladder(A,B,C,Sum,Carry);
  input A,B,C; //inputs
  output Sum,Carry;  //Outputs
   wire p,q,r;
  and a1(q,A,B); //AND of A and B equal to q
  and a2(r,p,C);  //AND of p and C equal to r
  xor a3(p,A,B);  //AND of A and B equal to p
  xor a4(Sum,p,C); //Defining Sum
  or a5(Carry,q,r);  //Defining Carry
endmodule
```

SV/Verilog Design

Output:

```
[2023-01-13 13:13:51 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
                   0 A = 0 B= 0 C= 0 SUM = 0  CARRY = 0
                  10 A = 0 B= 0 C= 1 SUM = 1  CARRY = 0
                  20 A = 0 B= 1 C= 0 SUM = 1  CARRY = 0
                  30 A = 0 B= 1 C= 1 SUM = 0  CARRY = 1
                  40 A = 1 B= 0 C= 0 SUM = 1  CARRY = 0
                  50 A = 1 B= 0 C= 1 SUM = 0  CARRY = 1
                  60 A = 1 B= 1 C= 0 SUM = 0  CARRY = 1
                  70 A = 1 B= 1 C= 1 SUM = 1  CARRY = 1
Done
```