

EE619A SPICE Project

Done by:-

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QUESTION 1 : Simulation of symmetrical and skewed CMOS inverter, and pass transistor

Minimum sized NMOS parameters:-

Channel length(L_n) = $180\mu m$

Channel Width(W_n) = $400\mu m$

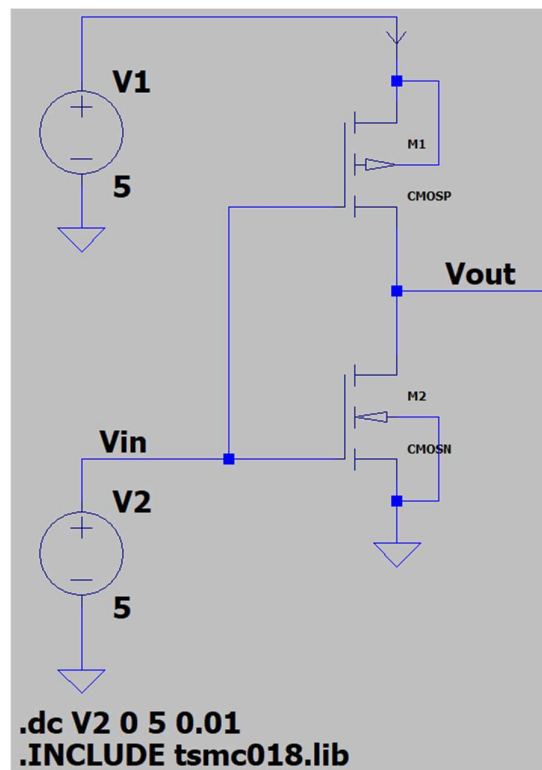
Minimum sized PMOS parameters:-

Channel length(L_p) = $180\mu m$

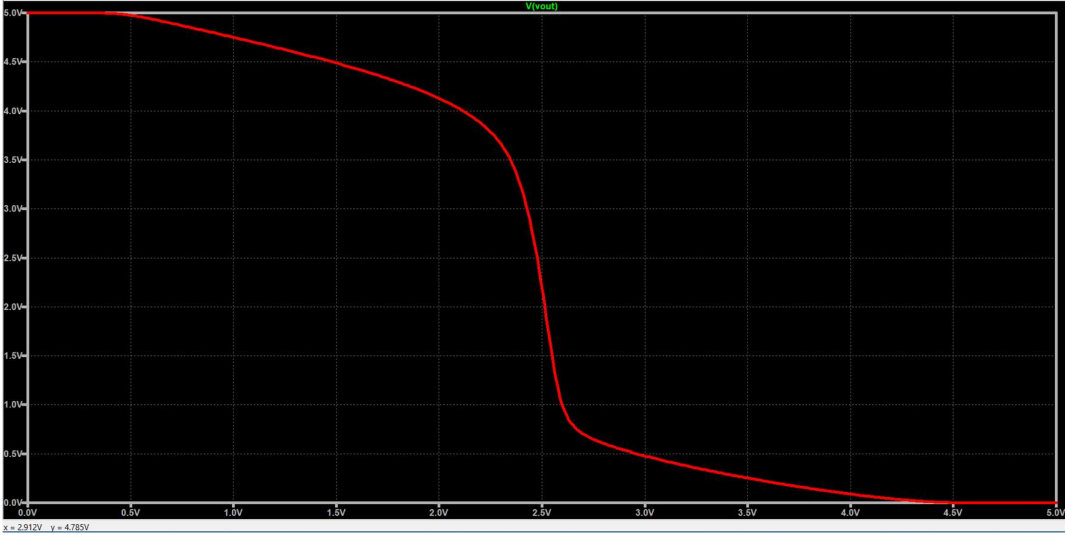
Channel width(W_p) = $800\mu m$

PART A:

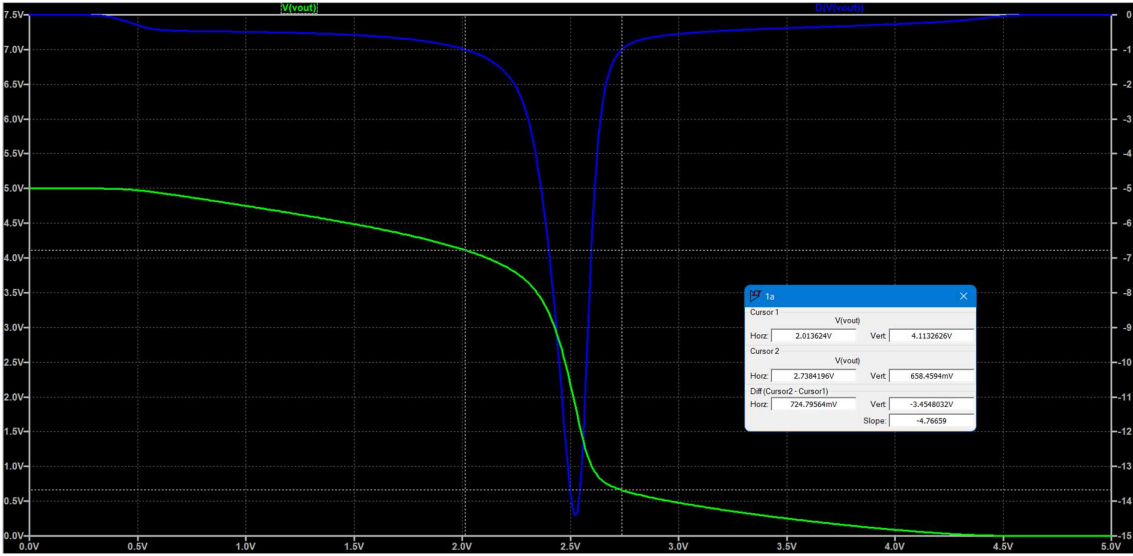
Since $2\mu_p = \mu_n$, we take W/L ratio of pmos twice as that of nmos

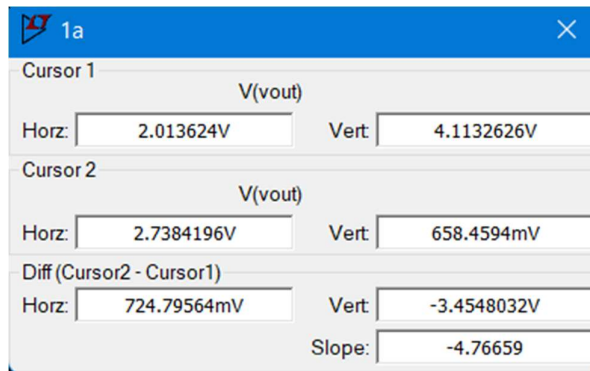


VTC of minimum sized inverter:



Calculation of VOL, VIL, VOL, VOH





$VOL = 658.459 \text{ mV}$

$VIL = 2.013 \text{ mV}$

$VIH = 2.73 \text{ mV}$

$VOH = 4.11 \text{ mV}$

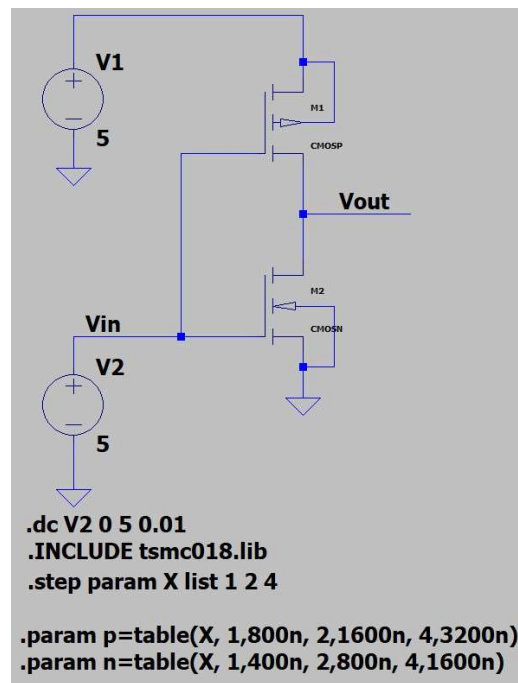
High noise margin = $VOH - VIH = 1.38 \text{ mV}$

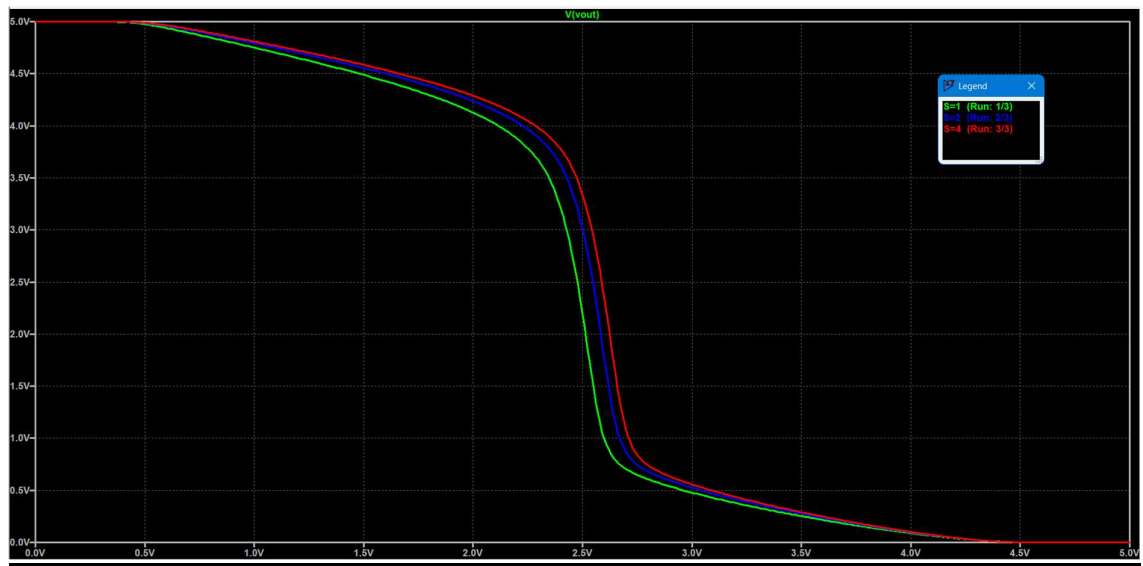
Low noise margin = $VIL - VOL = 1.4428 \text{ mV}$

Noise immunity of inverter

VTC of inverter when S=1,2,4 :-

Schematic:



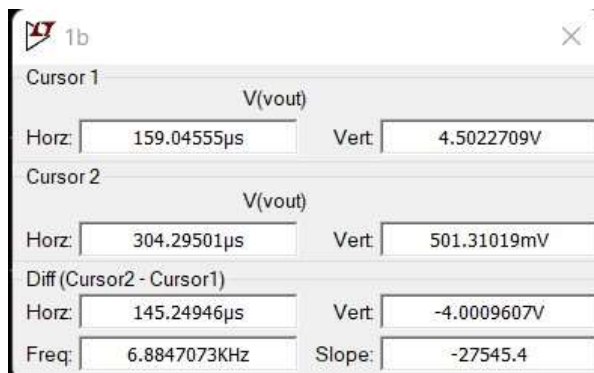


As S increases, VTC shifts towards right

PART B:

(i) When no external capacitance is attached.

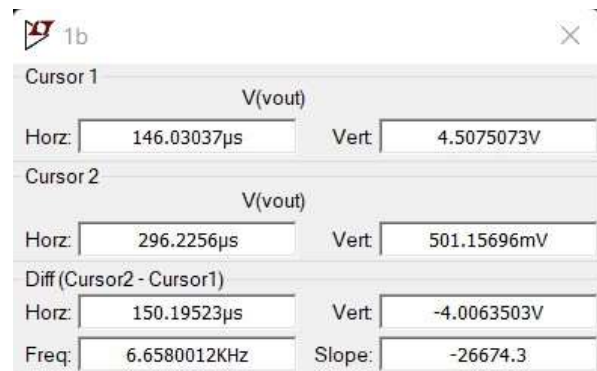
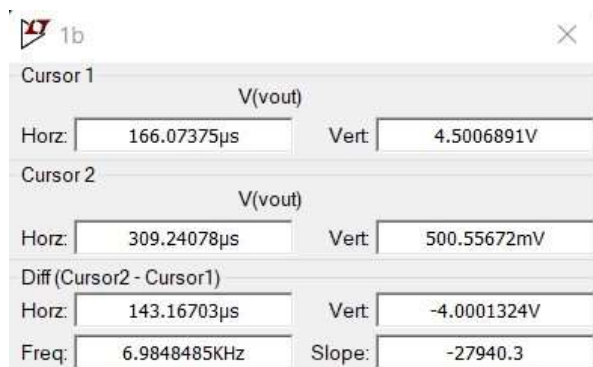
Fall Time :



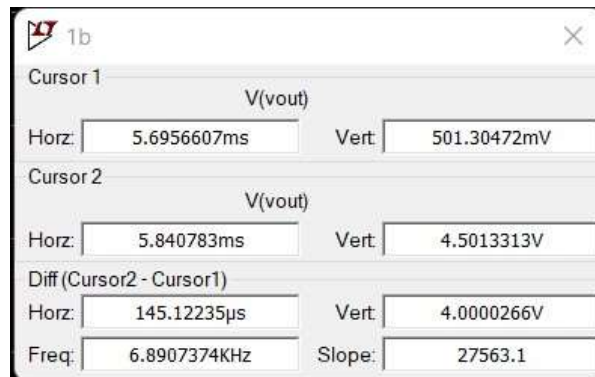
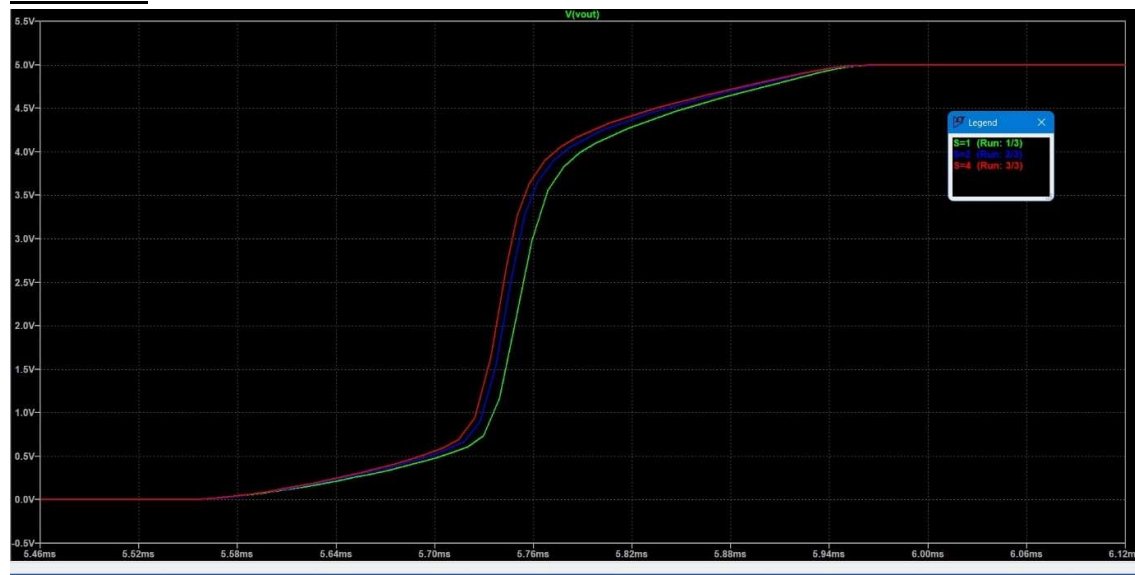
Fall time delay when S is 1 = 150.19 μs

Fall time delay when S is 2 = 145.24 μs

Fall time delay when S is 4 = 143.167 μs



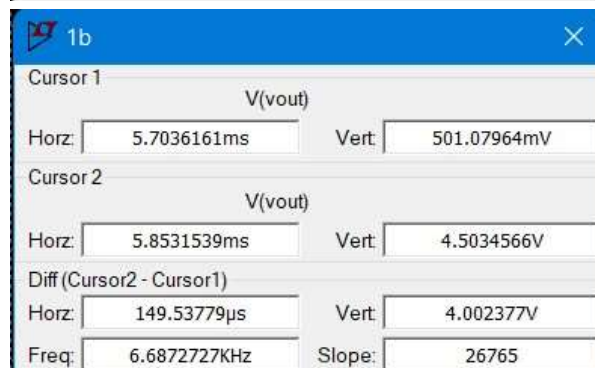
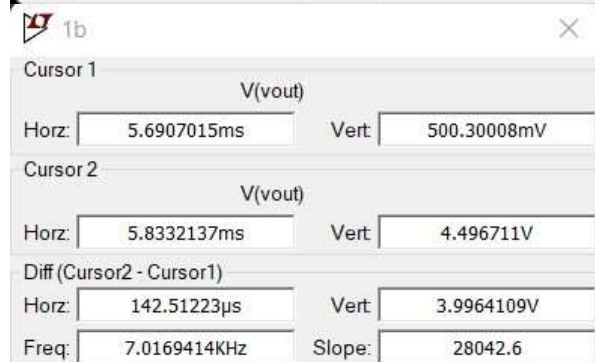
Rise Time:



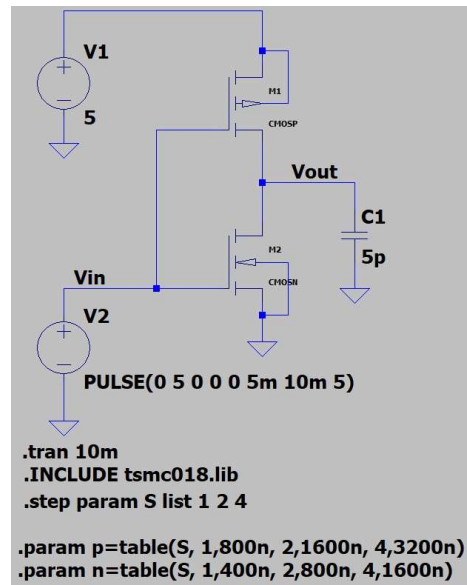
Rise time delay when S is 1 = 149.53 μ s

Rise time delay when S is 2 = 145.122 μ s

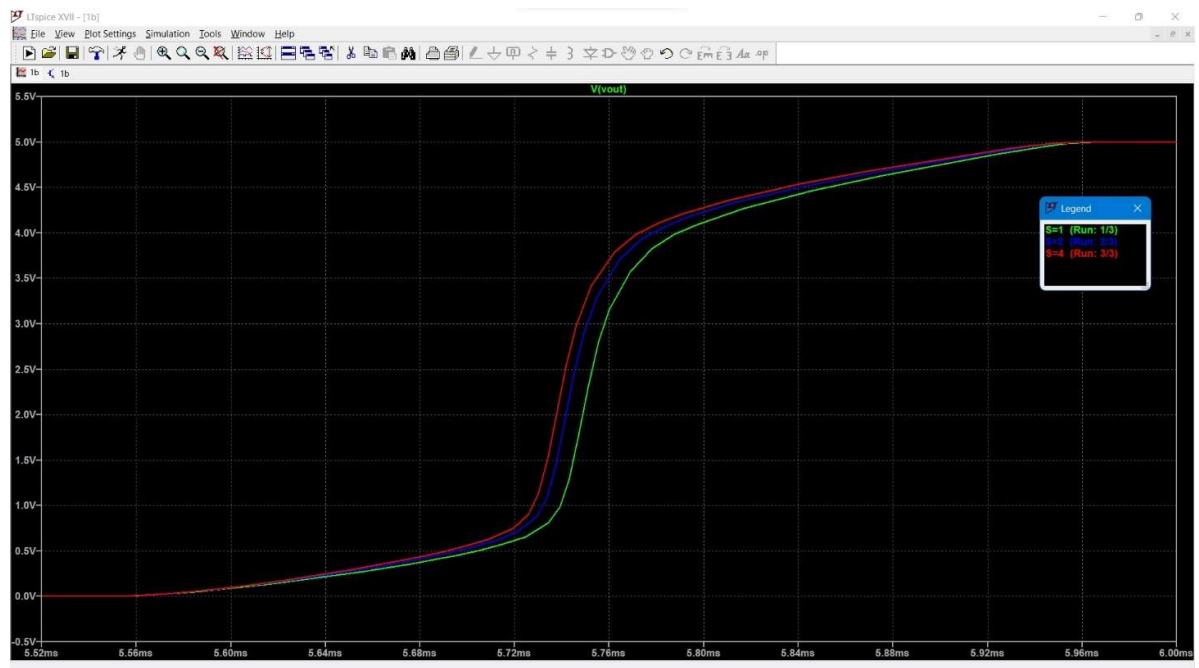
Rise time delay when S is 4 = 142.51 μ s



(ii) When external capacitance(5pF) is attached:



Rise time:

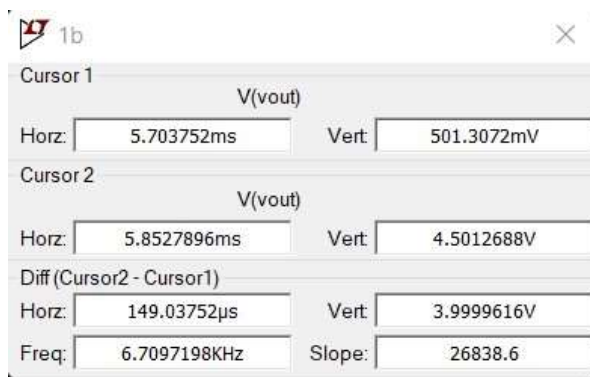


Rise time delay when S is 1 = 149.53 μs

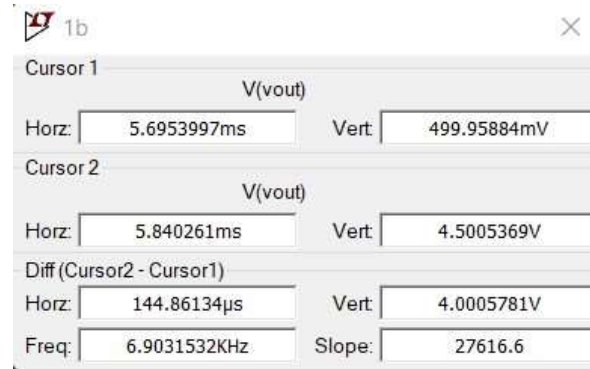
Rise time delay when S is 2 = 145.122 μs

Rse time delay when S is 4 = 142.51 μs

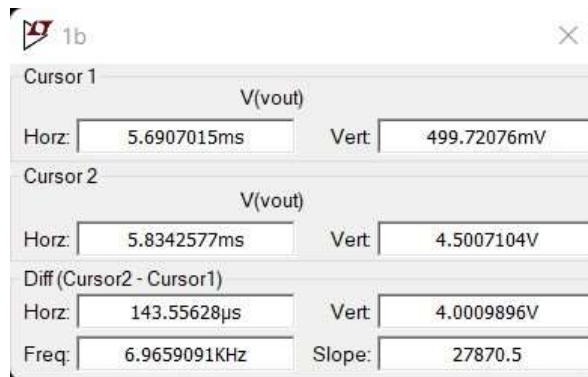
S=1



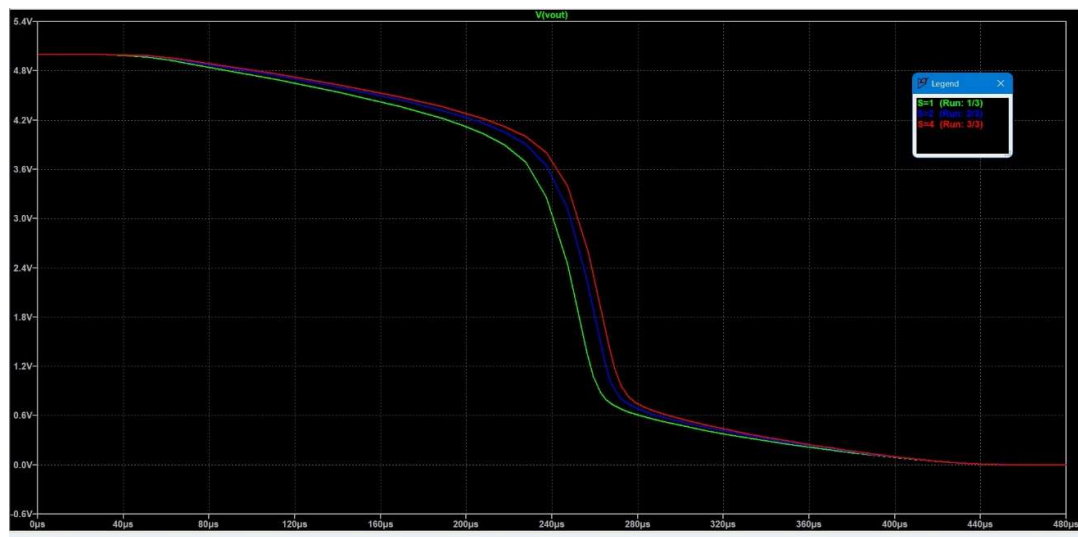
S=2



S=3



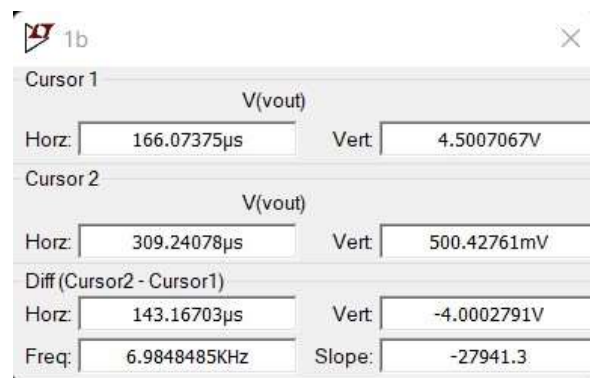
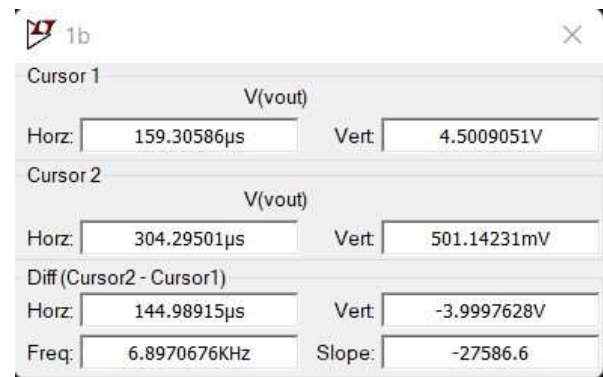
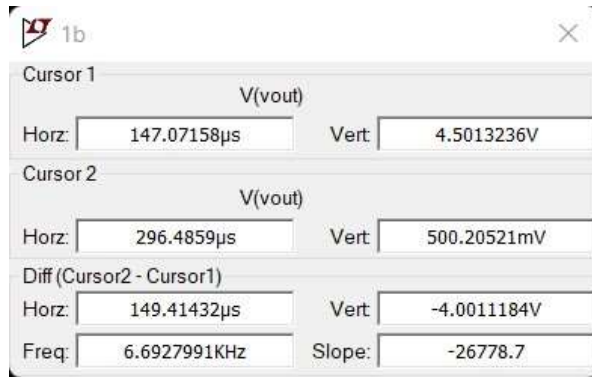
Fall Time:



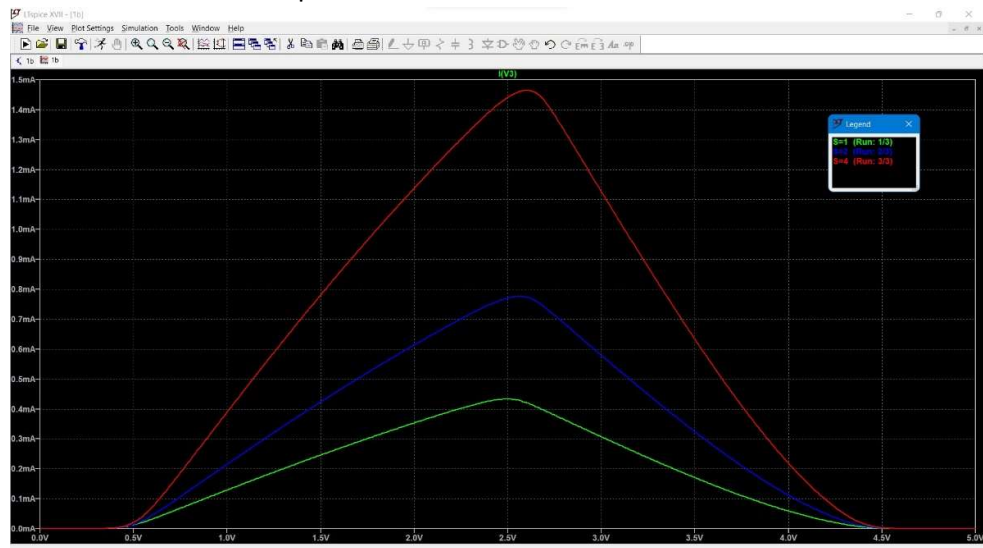
Fall time delay when S is 1 = $149.41 \mu s$

Fall time delay when S is 2 = $144.989 \mu s$

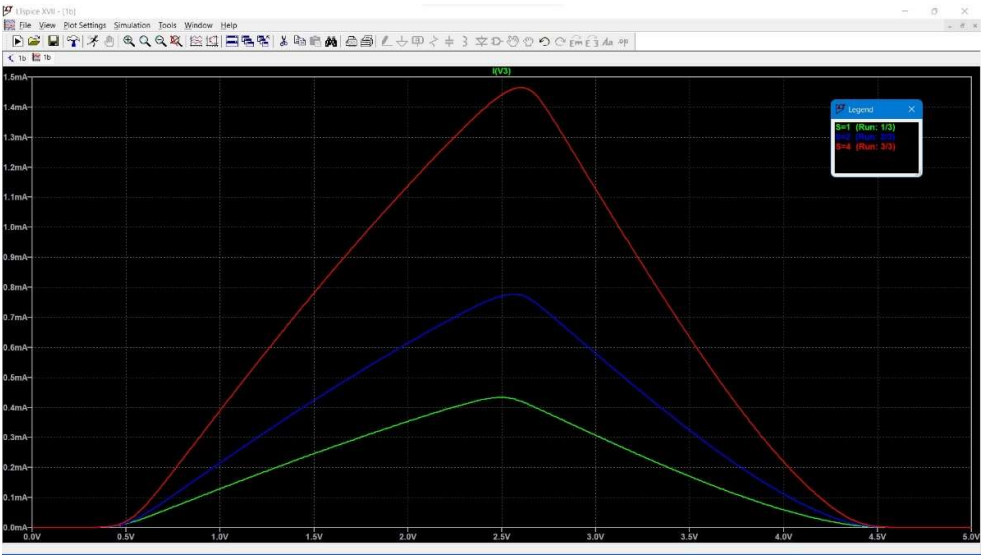
Fall time delay when S is 1 = $143.16 \mu s$



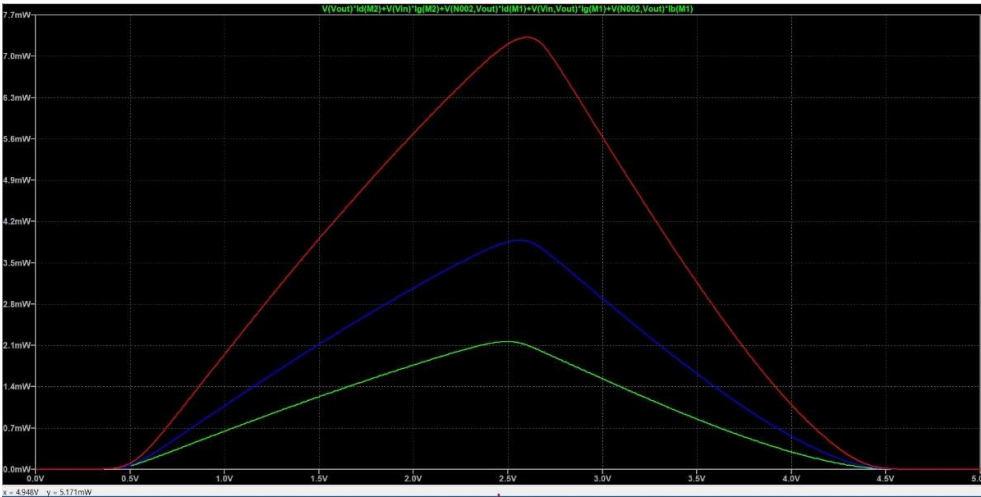
Current drawn when capacitor is not connected :



Current drawn when capacitance is connected:

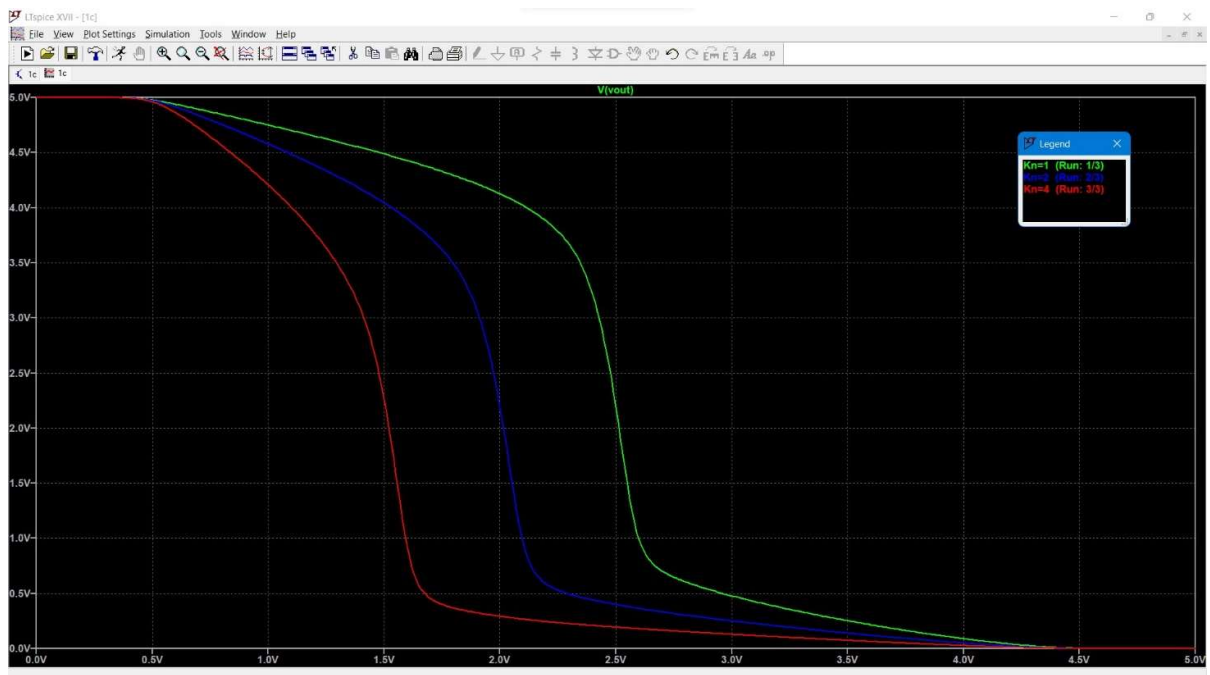
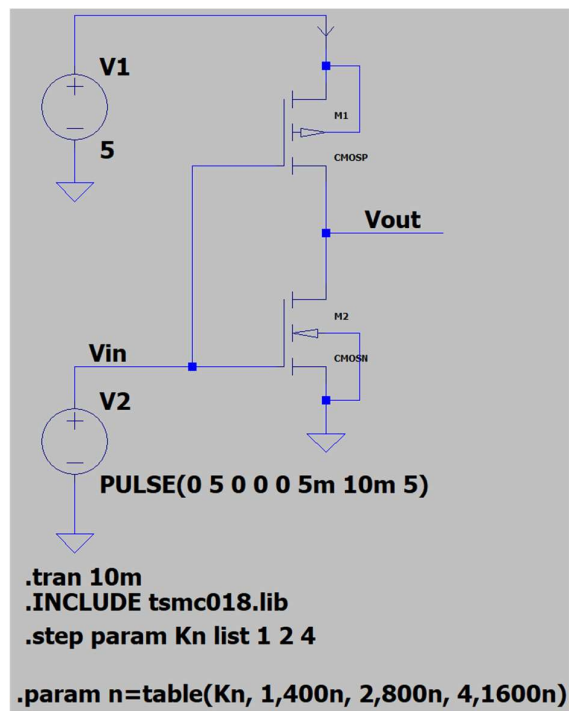


Power dissipation:



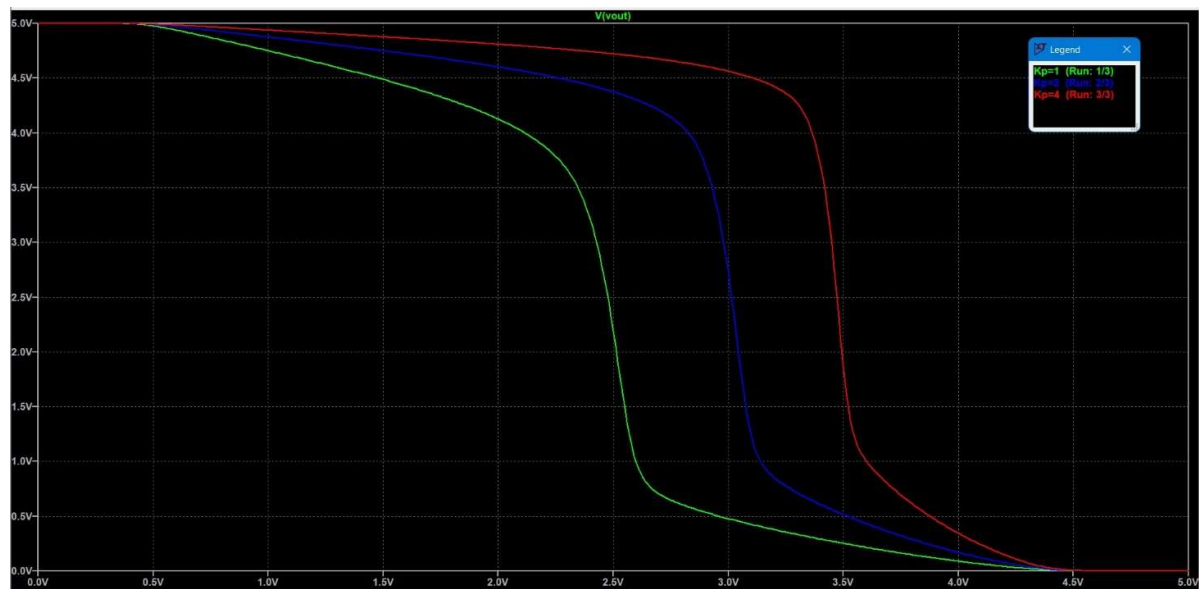
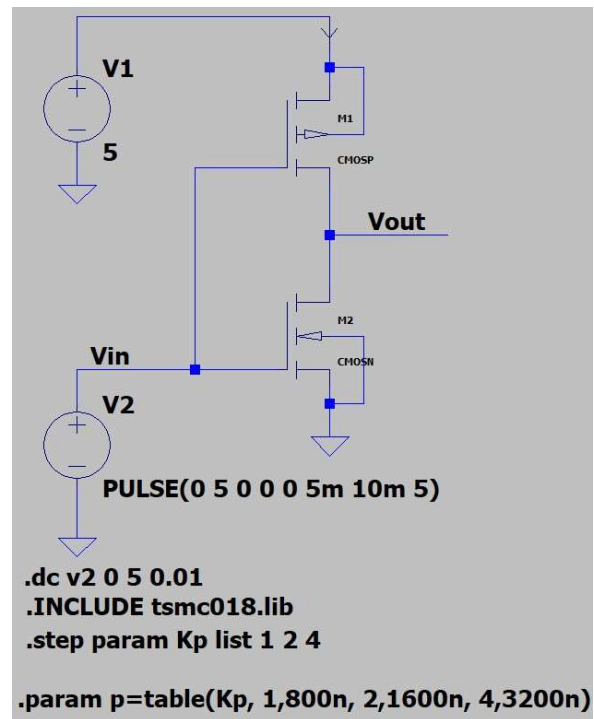
PART C:

(i) VTC when $K_n = 1, 2, 4$:



As K_n increases, VTC shifts towards left

(ii) VTC when $K_p = 1, 2, 4$

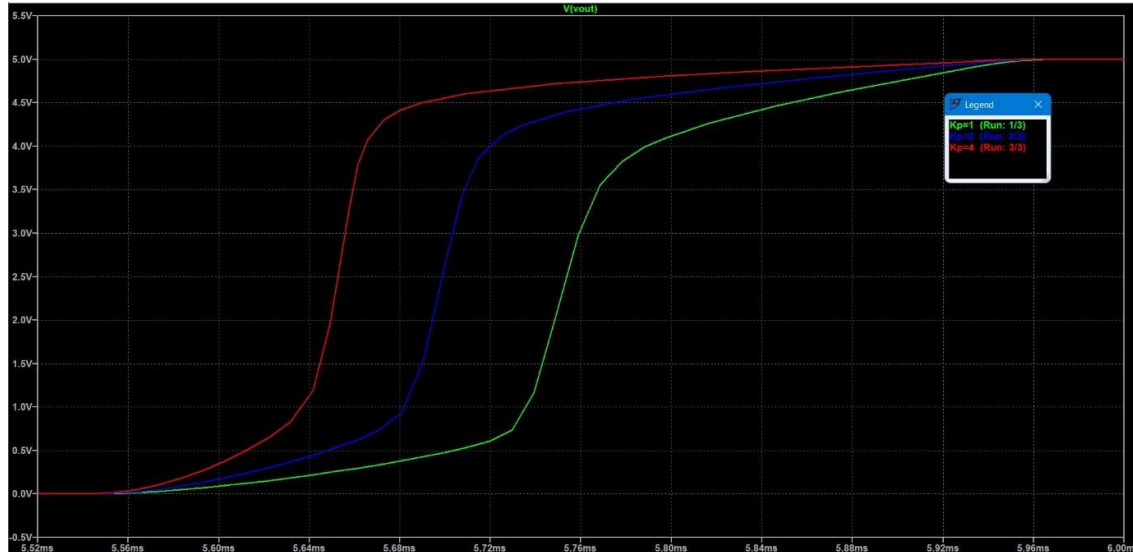


As K_p increases, VTC shifts towards right

PART D:

When Kp is varied(Kp=1,2,4) and Kn is fixed.

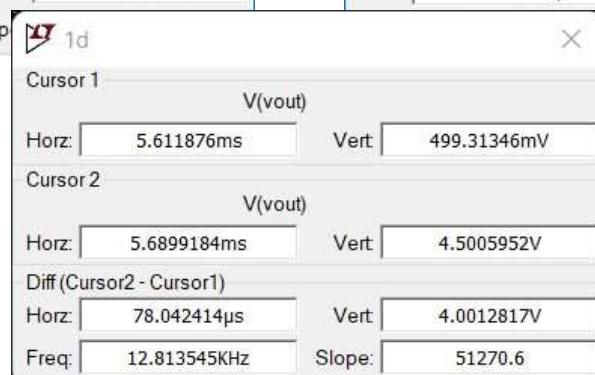
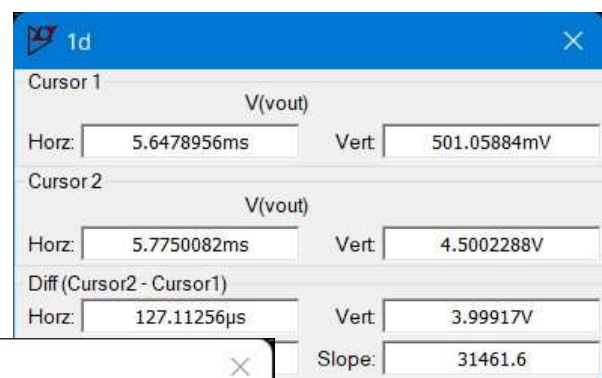
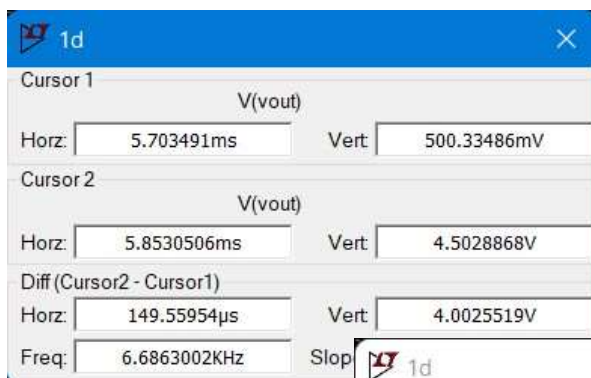
(i) Rise time delays when external capacitor is not attached :



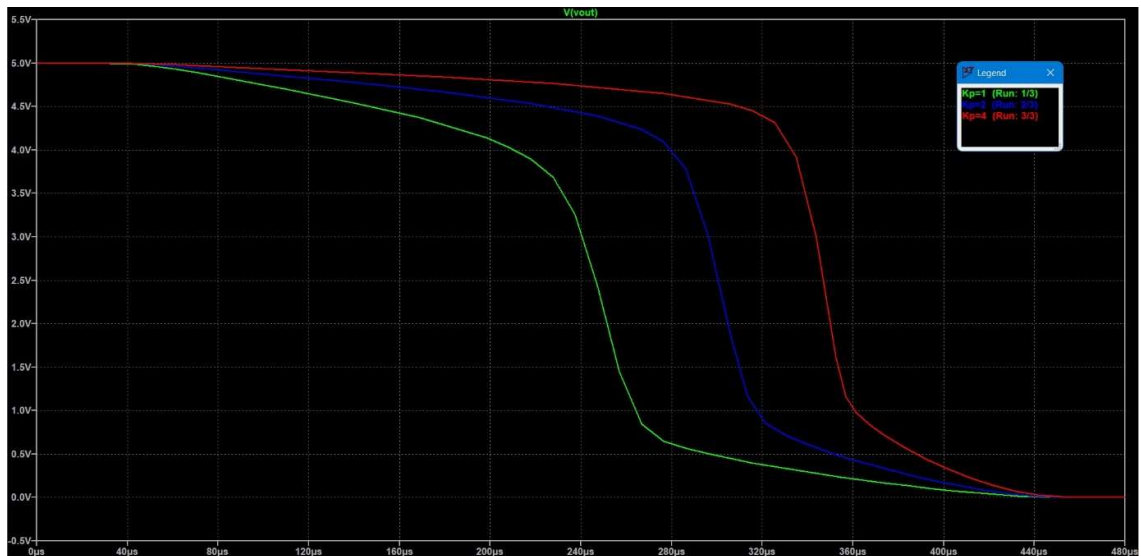
Rise time delay when Kp is 1 = $149.55 \mu s$

Rise time delay when Kp is 2 = $127.11 \mu s$

Rise time delay when Kp is 4 = $78.04 \mu s$



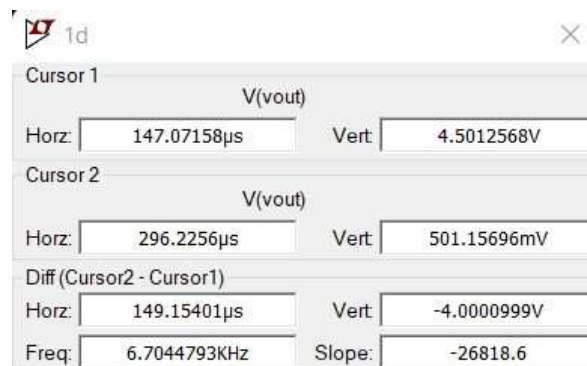
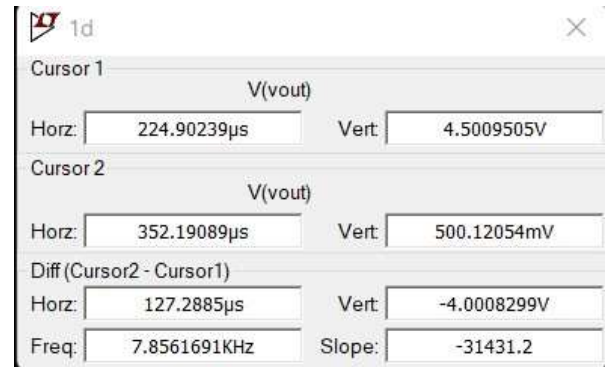
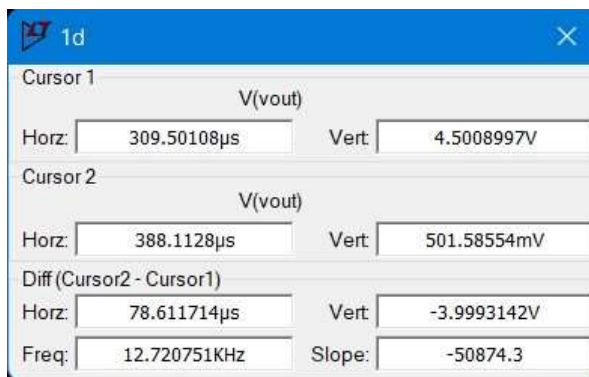
(ii) Fall time delays when external capacitor is not attached :



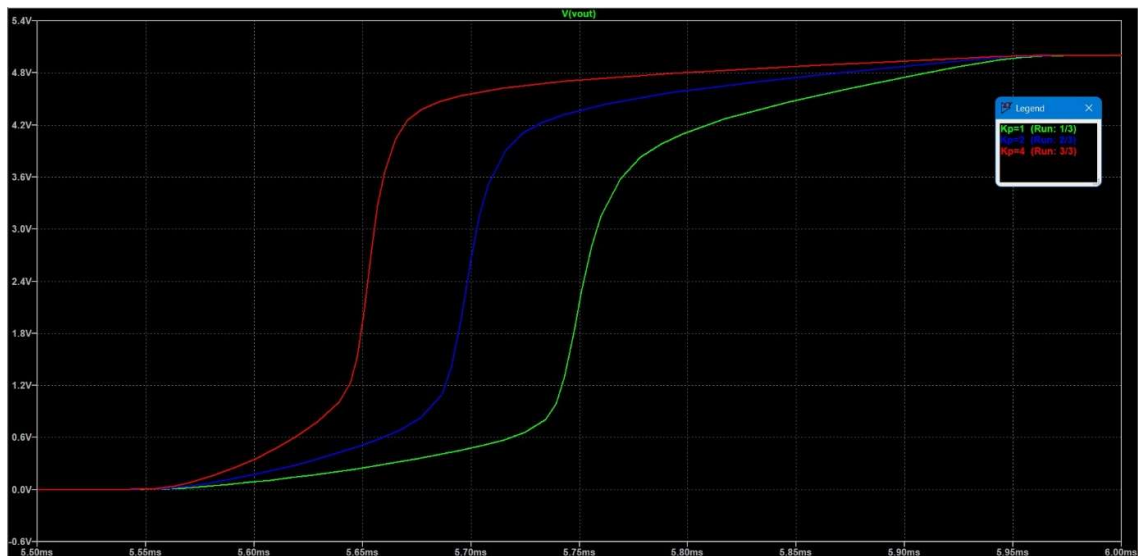
Fall time delay when Kp is 1 = $78.611 \mu s$

Fall time delay when Kp is 2 = $127.2885 \mu s$

Fall time delay when Kp is 4 = $149.154 \mu s$



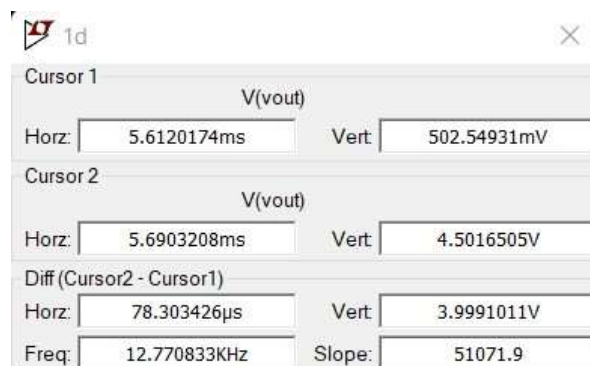
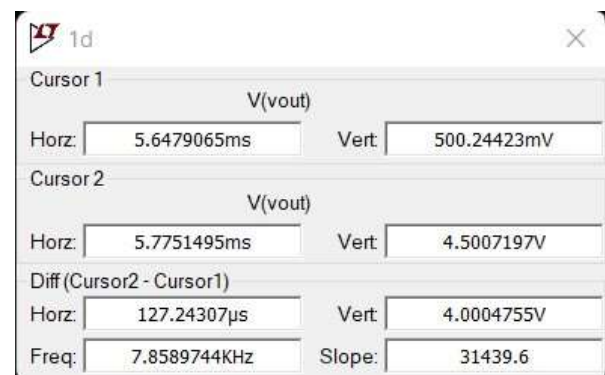
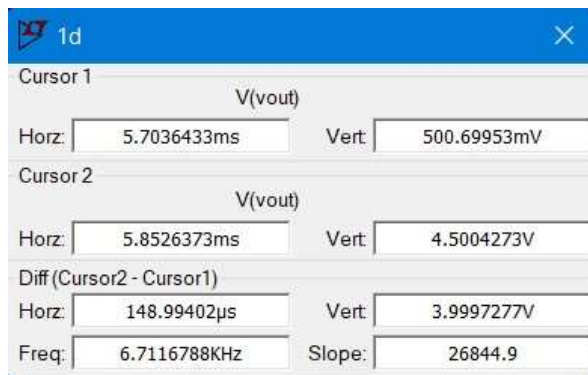
(iii) Rise time delays when external capacitor is attached :



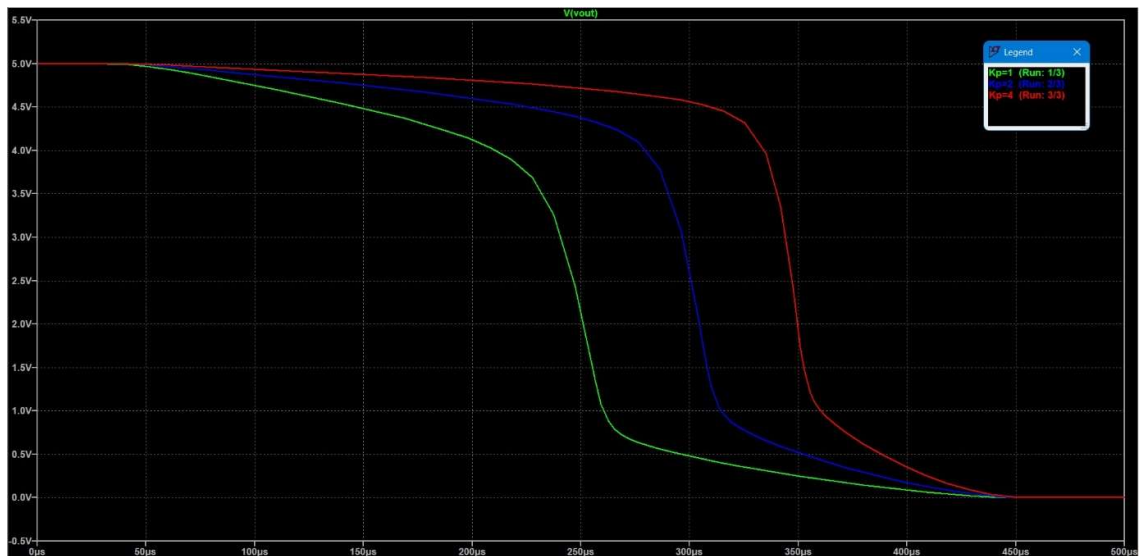
Rise time delay when Kp is 1 = 148.99 μ s

Rise time delay when Kp is 2 = 127.243 μ s

Rise time delay when Kp is 4 = 78.303 μ s



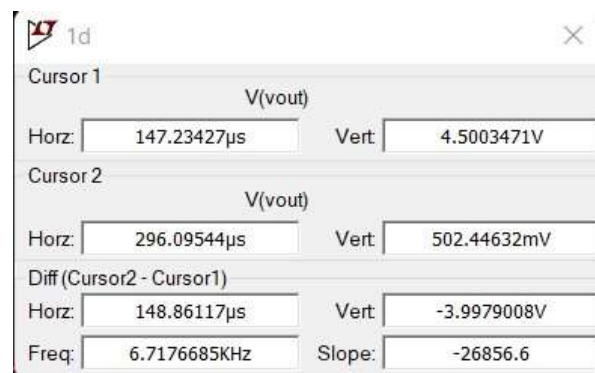
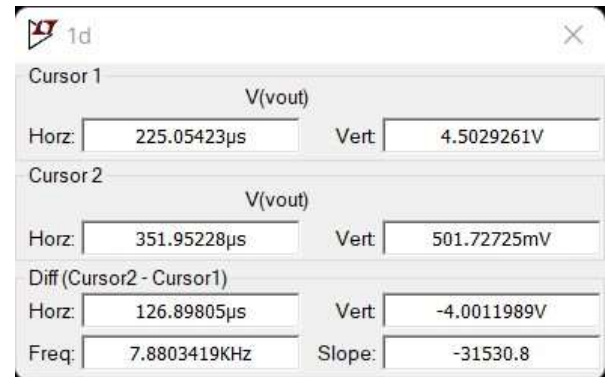
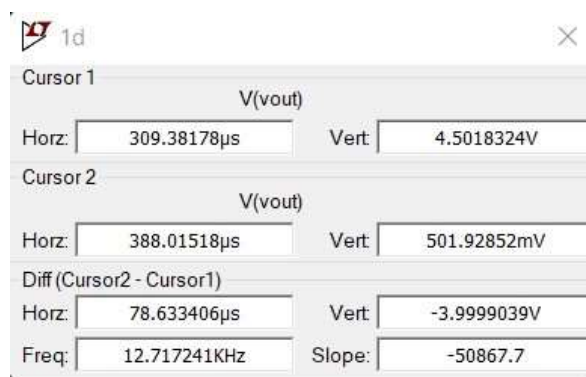
(iv) Fall time delay when capacitor is attached:



Fall time delay when Kp is 1 = $78.633 \mu s$

Fall time delay when Kp is 2 = $126.89 \mu s$

Fall time delay when Kp is 4 = $149.86 \mu s$



When K_n is varied ($K_n=1,2,4$) and K_p is fixed.

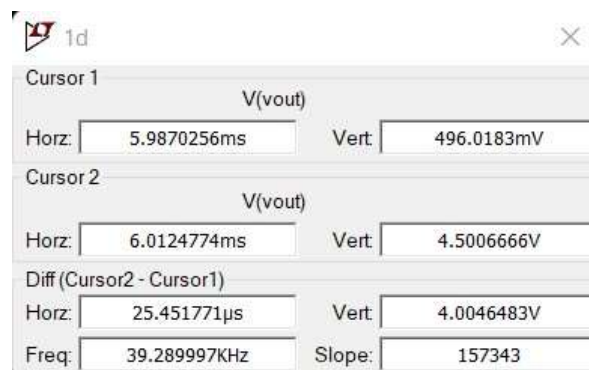
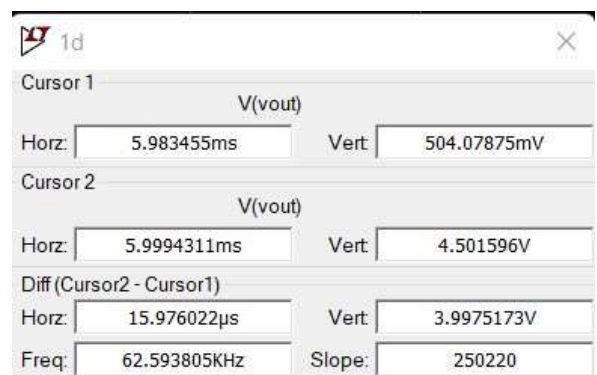
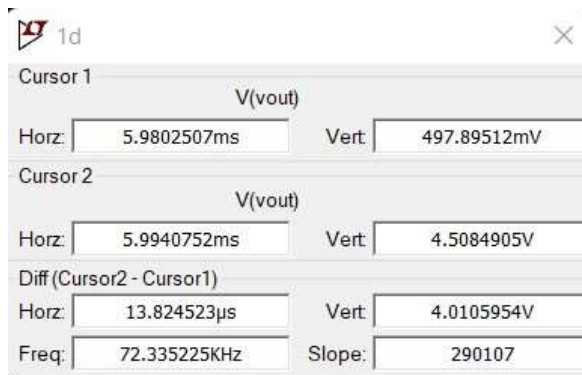
(i) Rise time delay when no external capacitance is connected



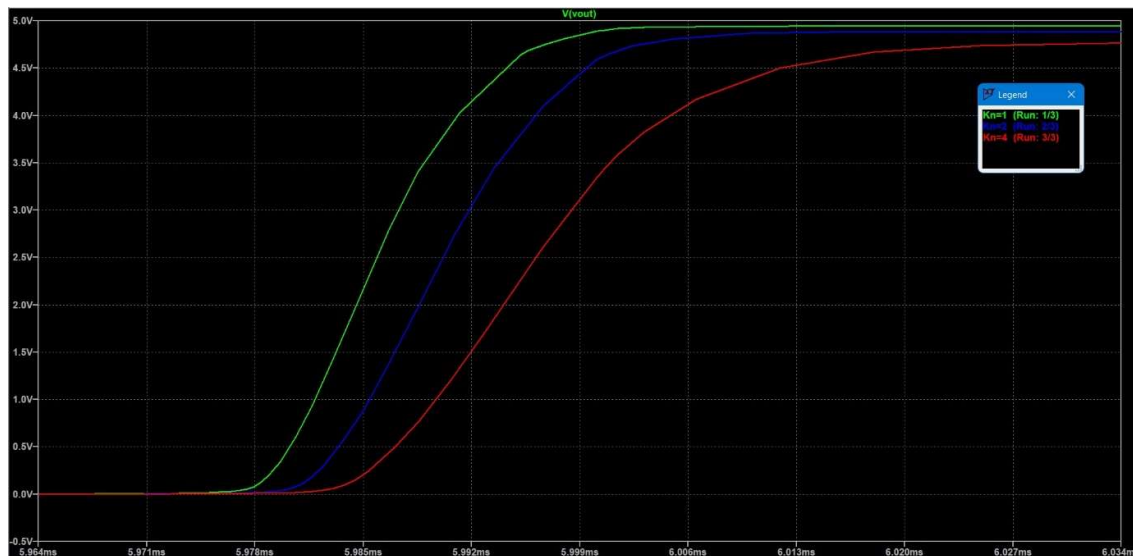
Rise time delay when K_n is 1 = $13.824 \mu s$

Rise time delay when K_n is 2 = $16 \mu s$

Rise time delay when K_n is 4 = $25.451 \mu s$



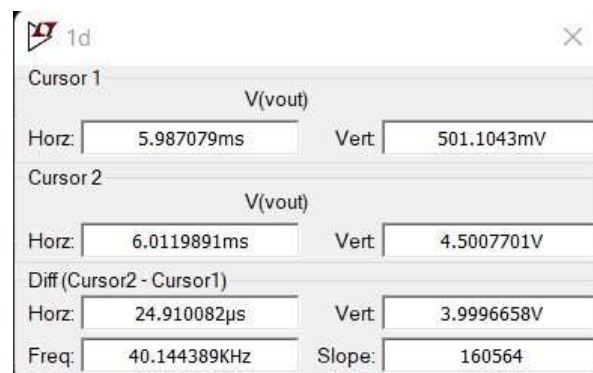
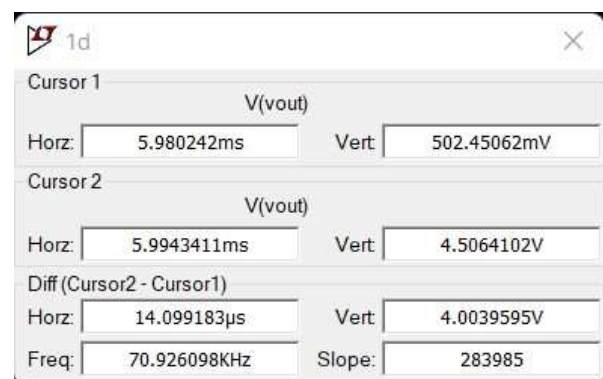
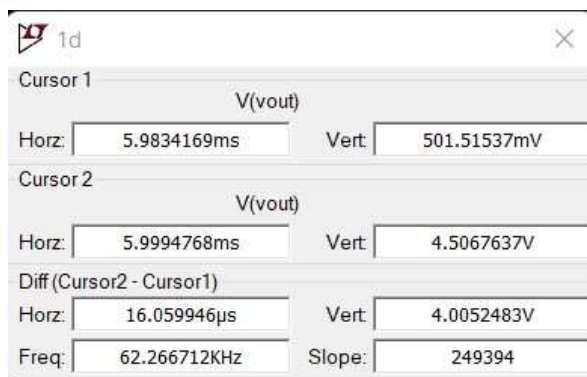
(ii) Rise time delay when external capacitance(5pF) is connected:



Rise time delay when Kn is 1 = 16.05 μ s

Rise time delay when Kn is 2 = 14.1 μ s

Rise time delay when Kn is 4 = 24.91 μ s



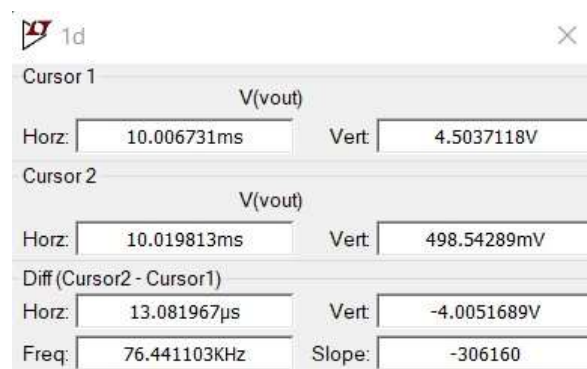
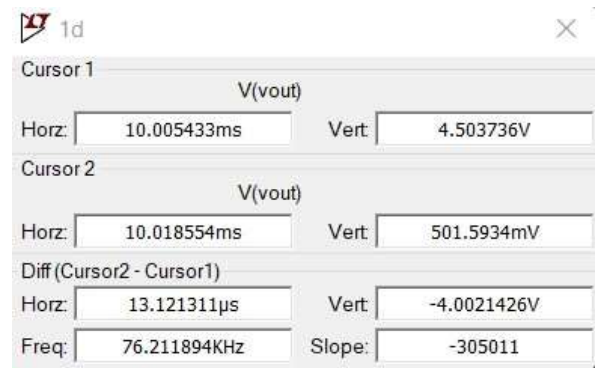
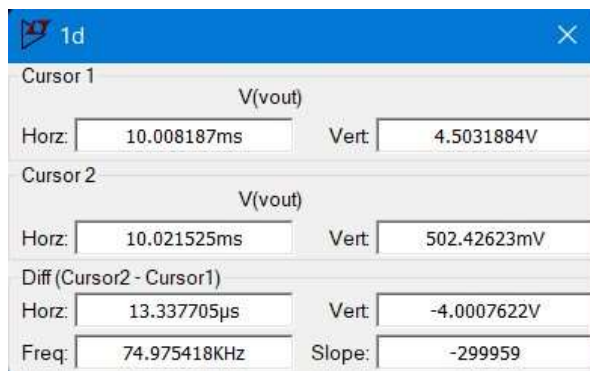
(iii) Fall time delay when external capacitor is not connected:



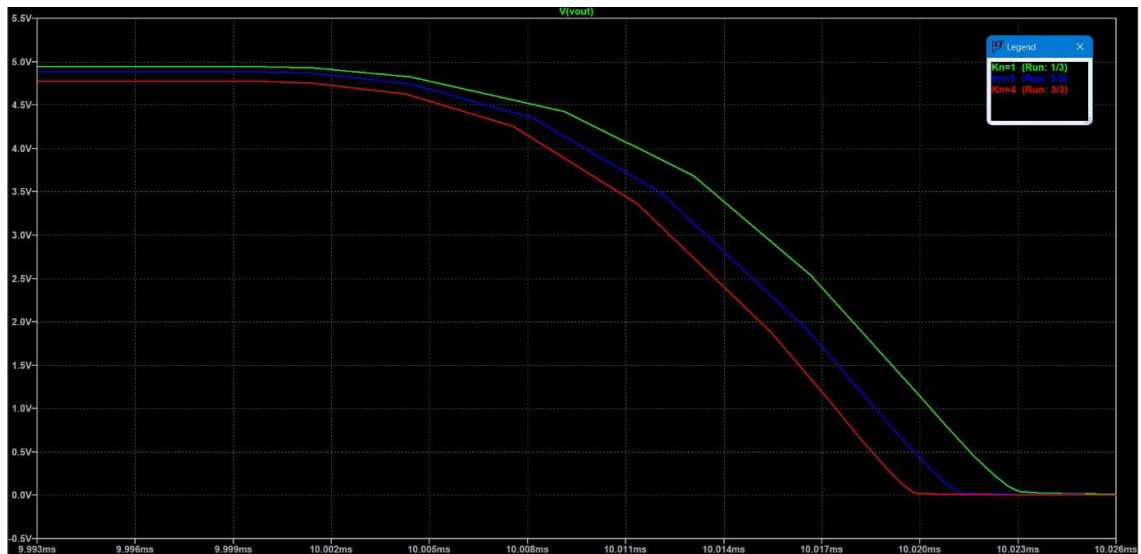
Fall time delay when Kn is 1 = 13.33 μ s

Fall time delay when Kn is 2 = 13.12 μ s

Fall time delay when Kn is 4 = 13.081 μ s



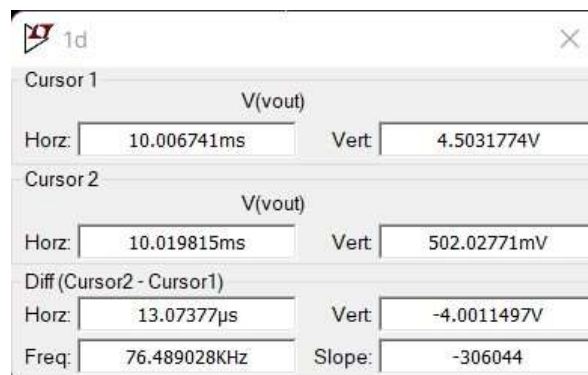
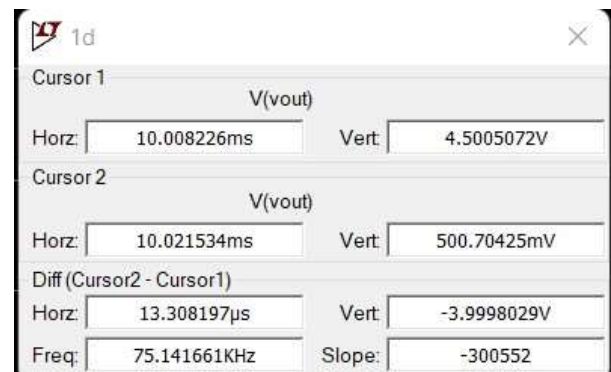
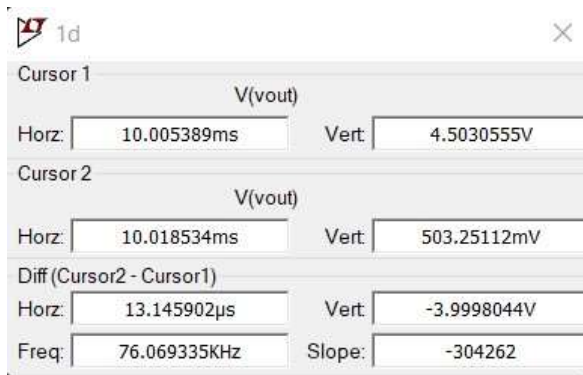
(iv) Fall time delay when external capacitor(5pF) is connected:



Fall time delay when Kn is 1 = 13.14 μs

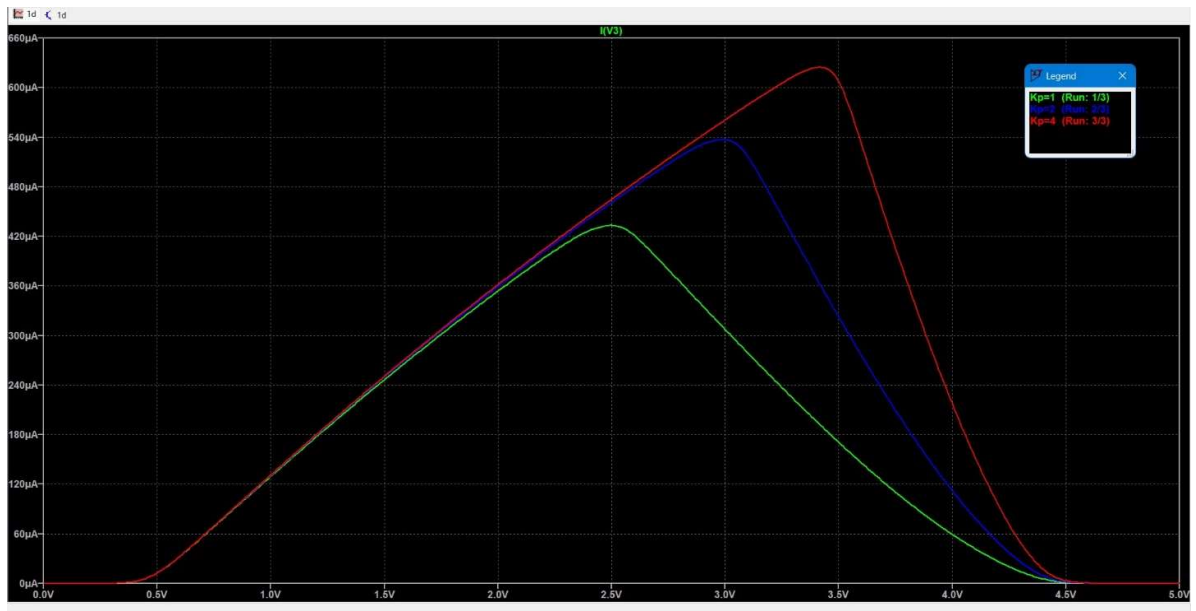
Fall time delay when Kn is 1 = 13.3 μs

Fall time delay when Kn is 1 = 13.07 μs

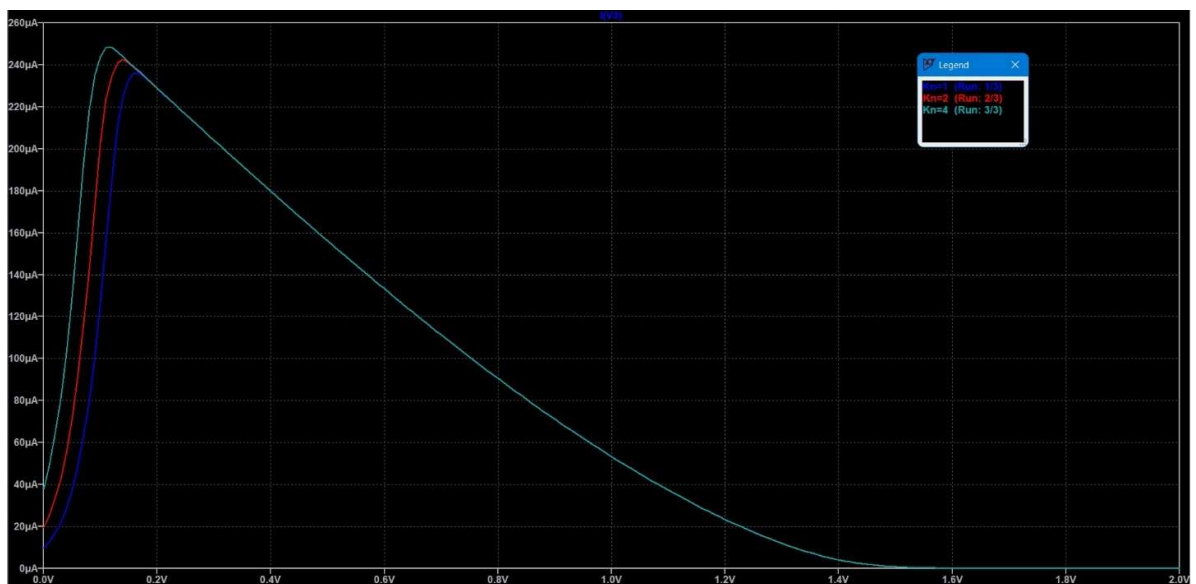


Current drawn from the power supply when capacitor is not connected at the output:

(i) When K_p is varied ($K_p=1,2,4$) and K_n is fixed

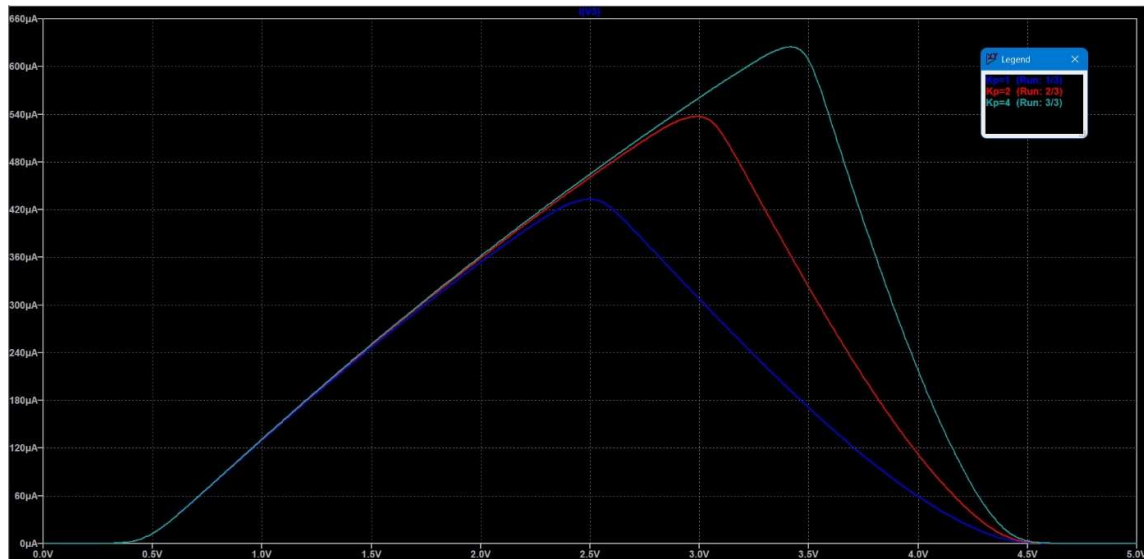


(ii) When K_n is varied ($K_n=1,2,4$) and K_p is fixed



Current drawn from the power supply when capacitor is connected at the output:

(i) When K_p is varied ($K_p=1,2,4$) and K_n is fixed



(ii) When K_n is varied ($K_n=1,2,4$) and K_p is fixed

