

FIELD EFFECT TRANSISTORS.Introduction

FET \rightarrow a semiconductor device which depends for its operation on the control of current by an electric field.

* Output Characteristics of FET

\hookrightarrow controlled by input voltage
(not input current).

* So, FET \rightarrow Voltage - controlled device.

\rightarrow flow of current through conduction region is only by majority carriers.

\therefore FET \rightarrow Unipolar device.

\rightarrow has 3 terminals. DRAIN, SOURCE & GATE

Types:-

1. Junction FET (JFET).

2. Metal Oxide Semiconductor FET (MOSFET) (or)
Insulated Gate FET (IGFET)

* Depending upon majority carriers, JFET can be classified as,

- (i) N-channel JFET (electrons)
- (ii) P-channel JFET (holes)

Features:-

- \rightarrow operation depends upon flow of majority carriers only
- \rightarrow immune to radiation
- \rightarrow high input impedance ($M\Omega$).
- \rightarrow Less noisy
- \rightarrow thermal stability.

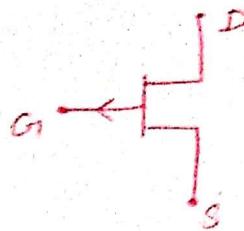
CONSTRUCTION OF JFET:-

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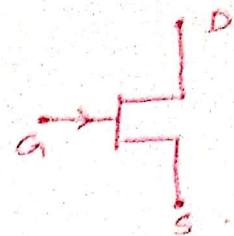
JFET → has a P-type (or) N-type Silicon Bar.

- * Bar is made up of N-type material \Rightarrow N-channel
- * P-type material Bar \Rightarrow P-channel.

SYMBOL



P-channel JFET.



N-channel JFET.

- * Ohmic contacts made at two ends of the bar, are called Source and Drain.

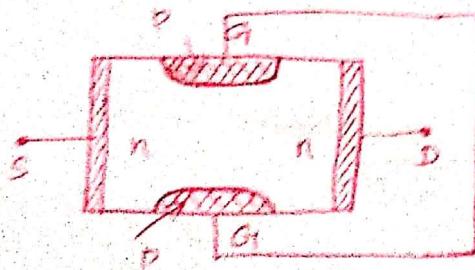
Source (S) → Majority charge carriers enter the bar through this terminal.

Drain (D) → Majority carriers leave the bar through this terminal.

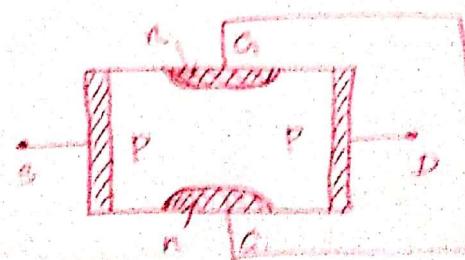
Gate (G) → Heavily doped silicon is diffused on both sides of the silicon bar by which PN-junctions are formed.

→ these layers joined together and called Gate.

Channel → The region between the two gate regions through which the majority carriers move from S to D.



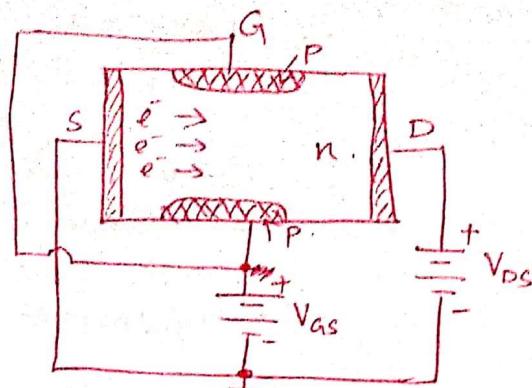
N-channel JFET.



P-channel JFET.

Operation of N-channel JFET.

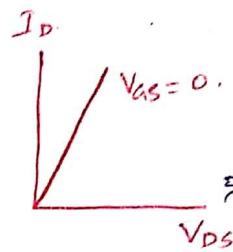
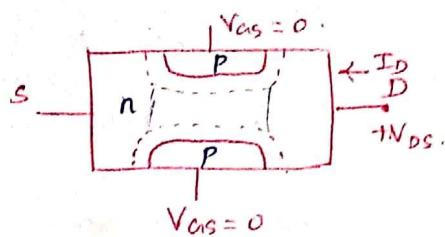
- N-region b/n two p-regions \Rightarrow channel.
- \rightarrow majority carriers (electrons) flow b/n source and drain.



Source \rightarrow carriers enter
Drain \rightarrow carriers leave.

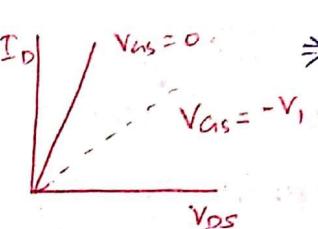
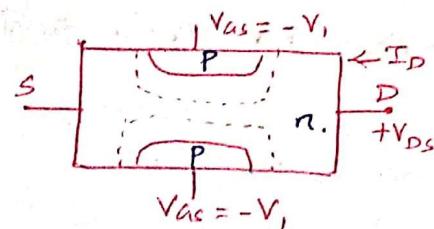
Gate terminals \rightarrow tied together.

JFET \rightarrow majority carrier device.

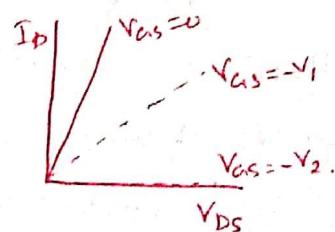
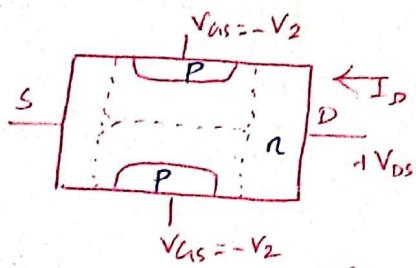


$\Rightarrow V_{GS} = 0, V_{DS} = \text{small positive voltage}$.
 \downarrow
I_D flows.

\Rightarrow approx. linear.



$\Rightarrow V_{GS} = -V_1, (\text{small})$
 \star Gate - channel \rightarrow reverse biased.
 \star depletion region widens
 \star channel \rightarrow narrows.
 \therefore Curve shifts to V_DS axis.



$\Rightarrow V_{GS} = -V_2 (\text{large}).$
 \star depletion region completely filled channel.
 \Downarrow pinch-off.

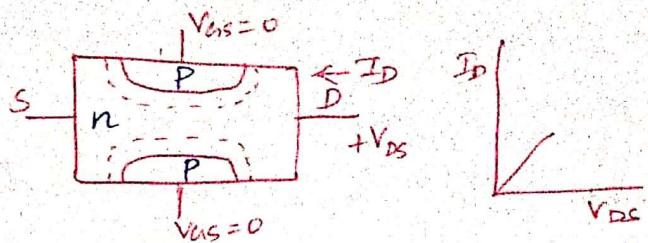
Channel \Rightarrow resistance.

* Normally ON (or) depletion mode device.

V_{GS} \rightarrow necessary to turn-OFF JFET.

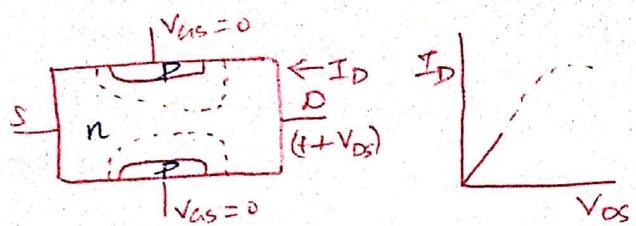
* Consider,

$$V_{GS} = 0 \text{ and } V_{DS} \rightarrow \text{varied.}$$



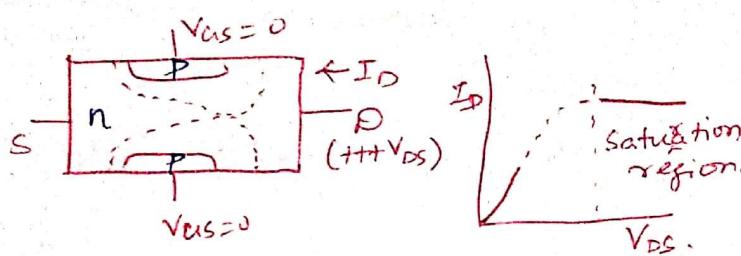
$V_{GS} = 0, V_{DS} = \text{Small}$.

Linear.



$V_{DS} \rightarrow \text{increased}$.

Gate-channel \rightarrow reverse biased near drain.



* depletion region extends into channel.

* channel resistance varies along channel length.

$\Rightarrow V_{DS} \rightarrow \text{large}$,

channel \rightarrow pinched off at drain.

for $V_{DS} > V_{DS(\text{sat})} \rightarrow \text{sat. region}$.

(i) When $V_{GS} = 0$ and $V_{DS} = 0$.

\rightarrow when no voltage is applied b/n drain and source, and gate and source,

* thickness of depletion \rightarrow uniform.

(ii) When $V_{DS} = 0$ and $V_{GS} \rightarrow \text{decreased from zero}$.

\rightarrow PN junctions are reverse biased

\therefore thickness of depletion increases.

\rightarrow for, large V_{GS} voltages,

depletion layers make contact with each other

In this condition, channel \rightarrow cut off.

(iii) When $V_{GS} = 0$ and $V_{DS} \rightarrow \text{increased from zero}$.

Drain \rightarrow positive with respect to source

* Majority carriers (electrons) flow through the N-channel from source to drain.

\rightarrow conventional current flows ($D \rightarrow S$).

* The magnitude of current will depend upon,

1. no. of majority carriers (electrons) available in channel
2. length of channel (L)
3. cross-sectional area (A) of channel
4. magnitude of applied voltage V_{DS} .

→ Channel → acts as resistance.

$$R = \frac{\rho L}{A} \quad \text{--- (1)}$$

$$I_D = \frac{V_{DS}}{R} = \frac{A \cdot V_{DS}}{\rho L} \quad \text{--- (2)}$$

where,

$\rho \rightarrow$ resistivity

* Because of resistance of channel and applied voltage V_{DS} ,

→ gradual increase of positive potential along the channel from source to drain.

→ reverse voltage across PN junction increases so thickness of depletion region also increases.

∴ Channel → Wedge shaped.

→ As V_{DS} is increased, cross sectional area of channel reduced.

→ At a certain value V_p of V_{DS} , cross-sectional area is minimum.

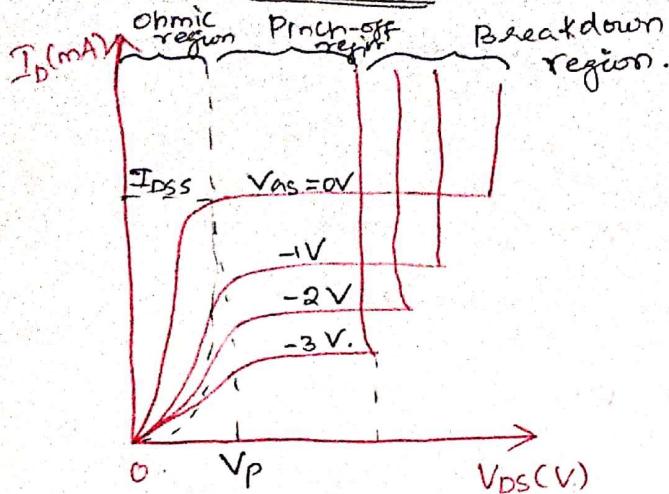
→ At this voltage,

channel → Pinched off.

and $V_p \rightarrow$ Pinch-off voltage.

Drain characteristics

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* Region from $V_{DS} = 0$ to $V_{DS} = V_p$.
↳ Ohmic region.

→ resistance in ohmic region is linear.

↳ Voltage Variable Resistor (VVR).
* When $V_{DS} = V_p$, $I_D \rightarrow$ maximum
→ for $V_{DS} > V_p$, length of pinch-off → increases.

∴ No increase of I_D .

* At certain voltage,
 $I_D \rightarrow$ Suddenly increases.

↳ due to "Avalanche multiplication"

(iv) When V_{GS} is negative and $V_{DS} \rightarrow$ increased.

$V_{GS} \rightarrow$ negative, junction further increased.

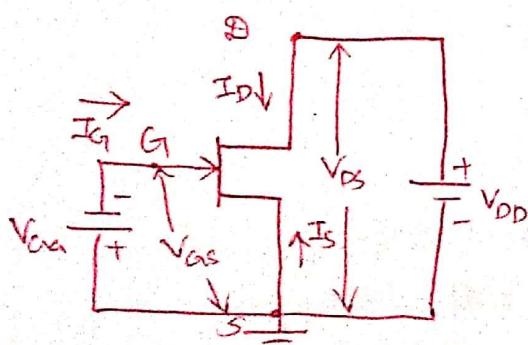
* Above pinch off voltage,

→ I_D increases with increase of V_{GS} .

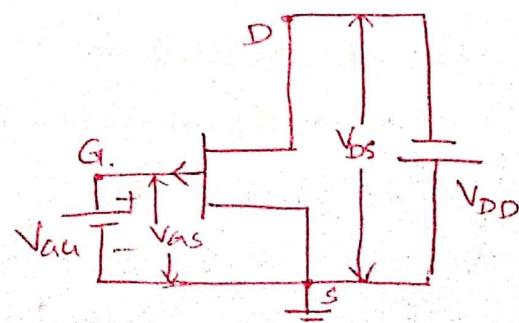
* At $V_{DS} = V_p$, I_D is not reduced to zero.

→ To make $I_D = 0$, reverse biasing of V_{GS} is essential for pinching off the channel.

→ I_D controlled by electric field.



N-channel JFET



p-channel JFET

Characteristic Parameters of JFET

$I_D \rightarrow$ depends upon V_{DS} , V_{GS} .

(1) Mutual conductance (or Transconductance) (g_m)

\rightarrow Slope of transfer characteristic curves.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} \rightarrow \text{constant.}$$

unit \rightarrow mho.

(2) Drain resistance (r_d)

\rightarrow reciprocal of slope of drain characteristics.

$$r_d = \frac{\partial V_{DS}}{\partial I_D} = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \rightarrow \text{constant.}$$

unit \rightarrow ohm.

(3) Amplification factor (μ)

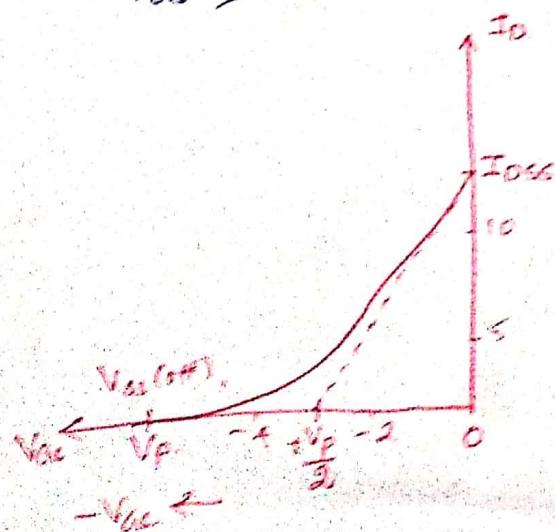
$$\mu = - \frac{\partial V_{DS}}{\partial V_{GS}} = - \frac{\Delta V_{DS}}{\Delta V_{GS}}, I_D \rightarrow \text{constant.}$$

negative sign \rightarrow when $V_{GS} \rightarrow$ increased, $\left. \begin{array}{l} \uparrow \text{for } I_D \\ V_{DS} \rightarrow \text{must be decreased} \end{array} \right\} \text{to be constant.}$

Transfer Characteristics.

* $V_{DS} \rightarrow$ constant at a suitable value.
 $(V_{DS} > V_p)$.

* $V_{GS} \rightarrow$ decreased from zero till I_D reduced to zero.



+ Shape of transfer char
 \hookrightarrow parabola

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad \text{--- (1)}$$

where,

$I_{DS} \rightarrow$ drain-source saturation current.

$I_{DSS} \rightarrow$ value of I_{DS} at $V_{GS} = 0$.

$V_p \rightarrow$ Pinch off voltage.

Differentiating eqn. (1), with respect to V_{DS} ,

$$\frac{\partial I_{DS}}{\partial V_{DS}} = I_{DS} \times 2 \left(1 - \frac{V_{DS}}{V_p} \right) \left(-\frac{1}{V_p} \right).$$

but, $G_m = \frac{\partial I_{DS}}{\partial V_{DS}}$, $V_{DS} \rightarrow \text{constant}$.

$$\therefore G_m = -\frac{2 I_{DS}}{V_p} \left(1 - \frac{V_{DS}}{V_p} \right) \quad \text{--- (2)}$$

From (1),

$$\left(1 - \frac{V_{DS}}{V_p} \right) = \sqrt{\frac{I_{DS}}{I_{DS}^2}} \quad \text{--- (3)}$$

Substitute (3) in (2),

$$G_m = -\frac{2 \sqrt{I_{DS} \cdot I_{DS}}}{V_p}$$

Suppose, $G_m = G_{m0}$, when $V_{DS} = 0$, then

$$G_{m0} = -\frac{2 I_{DS}}{V_p} \quad \text{--- (4)}$$

\therefore from (2) & (4),

$$G_m = G_{m0} \left(1 - \frac{V_{DS}}{V_p} \right). \quad \text{--- (5)}$$

$G_m \rightarrow$ varies as square root of saturation current.

Slope of transfer characteristics at I_{DS} .

$$\text{From (3), } G_m = -\frac{2 \sqrt{I_{DS} \cdot I_{DS}}}{V_p} = \frac{\partial I_{DS}}{\partial V_{DS}}$$

$$\text{Sub. } I_{DS} = I_{DS}, \quad \frac{\partial I_{DS}}{\partial V_{DS}} = -\frac{2 I_{DS}}{V_p} = \frac{-I_{DS}}{\frac{V_p}{2}}$$

\rightarrow above eqn., shows tangent to curve at $I_D = I_{DS}$, $V_{DS} = 0$ will have an intercept at $-\frac{V_p}{2}$.

* At $V_p = V_{DS(\text{cutoff})}$,

$$I_D = I_{DS} \left(1 - \frac{V_{DS}}{V_{DS(\text{cutoff})}} \right)^2$$

JFET

- depends only on flow of majority carriers only.
- No junctions. So less noisy.
- High input impedance ($M\Omega$) low output impedance.
- Voltage controlled device.
- Easy to fabricate.
- does not suffer from minority carrier storage effects.
- Costly.

BJT

- depends on both majority and minority carriers.
- More noisy.
- low input impedance, high output impedance.
- current controlled device.
- difficult.
- suffers from minority carriers effects.
- cheap.

Applications:

1. used as a buffer in measuring instruments, receivers
2. used in RF amplifiers in FM tuners and comm. equipments.
3. used in cascade amplifiers in measuring and testing equipments.
4. used as voltage variable resistor
5. used in mixer circuits in FM and TV receivers.
6. used in oscillator circuits.
7. used in low frequency amplifiers
8. used in digital circuits in computers, memory circuits.

Metal Oxide Semiconductor FET (MOSFET)

- * Insulated Gate FET (IGFET).
- Two basic forms of MOSFET.
 1. Enhancement MOSFET
 2. Depletion MOSFET.

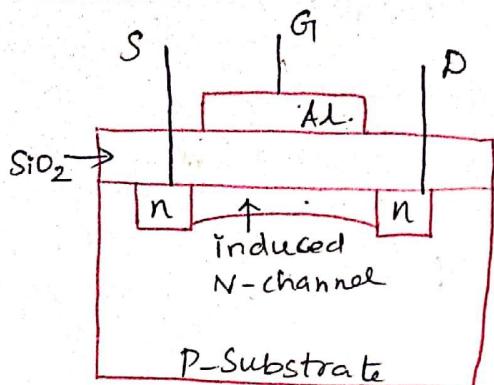
Principle → By applying a transverse electric field across an insulator, deposited on the semiconducting material, the thickness and hence resistance of a conducting channel can be controlled.

depletion MOSFET \rightarrow controlling electric field reduces the no. of majority carriers.

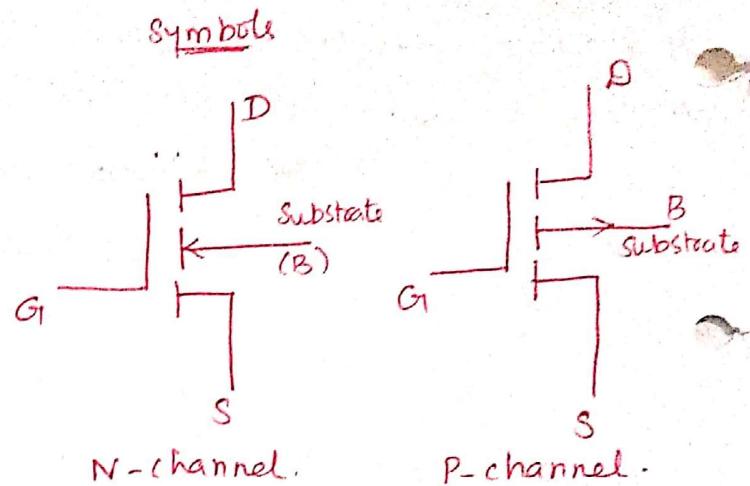
enhancement MOSFET \rightarrow application of electric field causes an increase in majority carrier density.

Enhancement MOSFET.

Construction.



N-channel E-MOSFET.



N-channel.

P-channel.

- * Two highly doped N-regions are diffused in a lightly doped substrate of P-type silicon substrate.

One N-region \rightarrow Source (S)

Other N-region \rightarrow Drain (D).

- * A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into oxide layer, allowing contact with source and drain.

- * A thin layer of metal aluminium is formed over the layer of SiO_2 .

\rightarrow metal layer covers the entire channel region and it forms the gate (G).

Gate (G) + SiO_2 layer + channel \Rightarrow parallel plate capacitor.

- * insulating layer of $\text{SiO}_2 \rightarrow$ gives extremely high input impedance.

Operation:-

- If, substrate \rightarrow grounded,
Gate \rightarrow positive voltage is applied
- * positive charge on G induces an equal negative charge on substrate b/n source and drain regions.
 - \rightarrow electric field is produced b/n source and drain.
 - \rightarrow direction of electric field is perpendicular to plates of capacitor through oxide.
 - * negative charge of electrons which are minority carriers in P-type substrate forms an inversion layer.
- As positive voltage on Gate \uparrow ,
- * induced negative charge in semiconductor increases.
 - \rightarrow Hence, conductivity increases and current flows from source to drain through induced channel.
 - * $I_D \rightarrow$ enhanced by positive gate voltage.

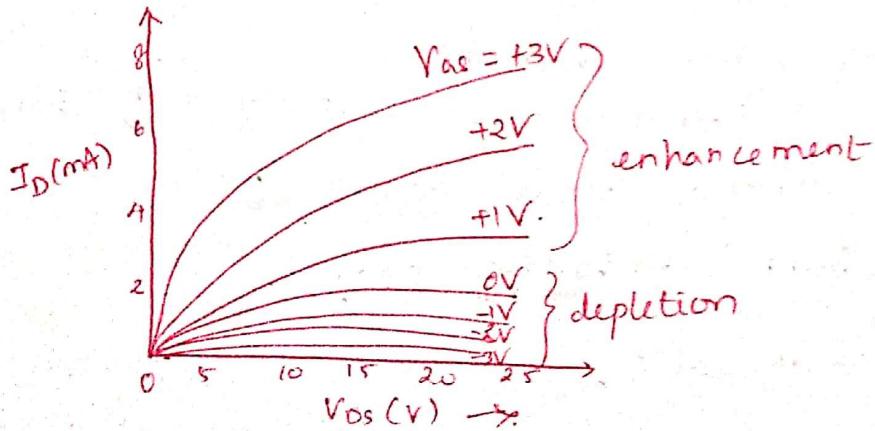
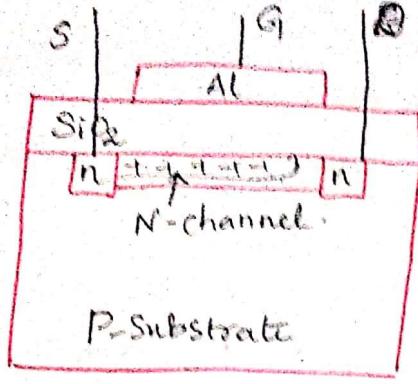


Fig: VI characteristics of MOSFET.

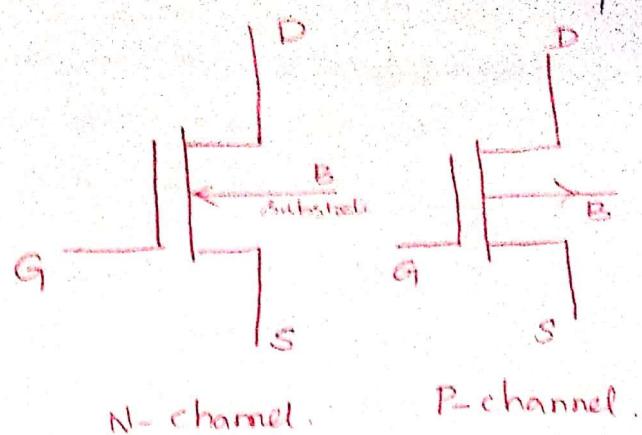
Depletion MOSFET.

Construction:-

- N-channel is diffused b/n source and drain to the basic structure of MOSFET.



N-channel depletion MOSFET.



N-channel.

P-channel.

Operation:-

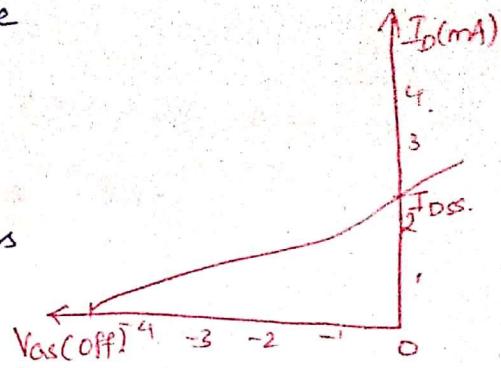
- * With $V_{GS} = 0$, Drain \rightarrow positive potential with respect to source.
 → electrons flow through the N-channel from S to D.
 But conventional current, I_D flows from D to S.
- * If gate voltage \rightarrow negative,
 → positive charge is introduced in channel through gate channel capacitor.
 → introduction of positive charge causes depletion of mobile electrons in channel.
 (S) depletion region is produced in channel.
- * Shape of depletion depends V_{GS} and V_{DS} .
 ∴ channel \rightarrow Wedge shaped.
 → When $V_{DS} \rightarrow$ increased, $I_D \rightarrow$ increases and it becomes practically constant at a certain value of V_{DS} .
 (S) Pinch-off voltage.
- * $I_D \rightarrow$ saturated beyond pinch-off voltage.
- * Induced positive charges make the channel less conductive,
 → I_D drops as $V_{GS} \rightarrow$ negative.

depletion MOSFET \rightarrow may be operated in an enhancement mode.

By applying positive voltage to gate.

* Also called "dual gate MOSFET"

* Curve of I_D vs V_{GS} for constant V_{DS} is called transfer characteristics of MOSFET.



MOSFET

\rightarrow transverse electric field applied across insulating layer.

\rightarrow gate leakage current, $10^{-12} A$

i/p resistance is high, 10^{10} to $10^{15} \Omega$.

\rightarrow operated in depletion & enhancement mode.

\rightarrow easy to fabricate

* MOSFET's are mostly used in digital VLSI circuits.

JFET

\rightarrow applied across PN junctions

$\rightarrow 10^{-9} A$, i/p resistance, $10^8 \Omega$.

\rightarrow operated only in depletion mode.

\rightarrow difficult.

Threshold Voltage:-

\rightarrow applied gate voltage required to create the inversion layer charge.

\rightarrow applied gate voltage required to achieve threshold inversion point.

Capacitance of device, $C = \frac{dQ}{dV}$

Channel Length Modulation

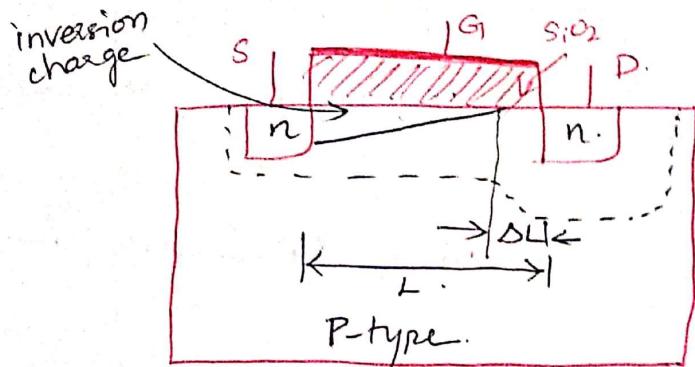
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In deriving current relations, the channel is assumed constant.

* But, when MOSFET is biased in saturation region,

→ depletion region at drain extends into channel.

↳ reduces channel length.



n-channel MOSFET.

Ideal drain current (I_D).

Actual drain current (I_D')

$$I_D' = \left(\frac{L}{L - \Delta L} \right) \cdot I_D.$$

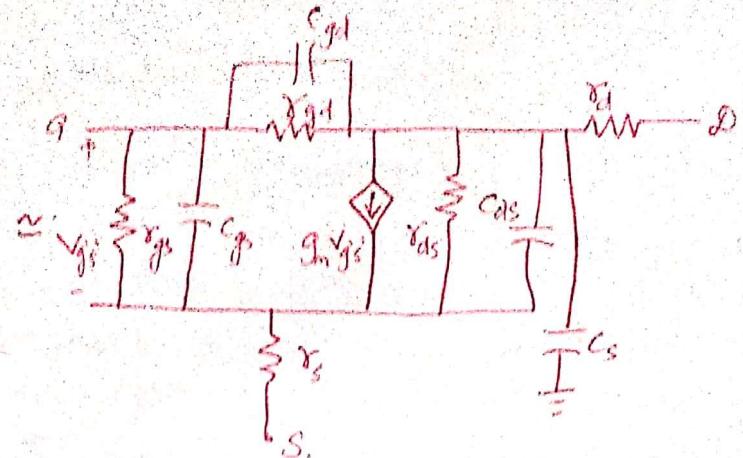
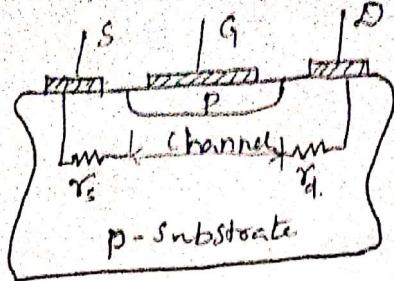
$I_D \rightarrow$ Inversely proportional 'L'.

* The change in the effective channel length and the corresponding change in drain current is called channel length modulation.

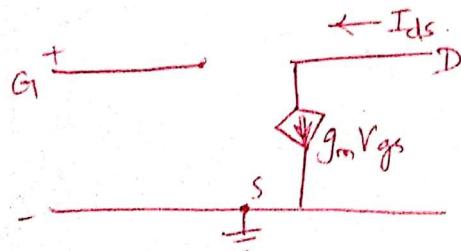
* Small-signal output impedance at the drain terminal can be defined as,

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D'}$$

Equivalent circuit of JFET



- V_{gs}' → Internal gate-to-source voltage that controls I_D .
- * r_{gs} , C_{gs} → gate-to-source diffusion resistance & capacitance.
- * Gate-to-Source → reverse biased.
- * Gate-to-Drain → reverse biased.
- * r_{ds} → drain resistance as a function of channel length modulation effect.
- r_s → drain resistance as a function of channel length modulation effect.
- C_{ds} → drain-to-source parasitic capacitance.
- C_s → drain-to-substrate capacitance.



- * diffusion resistance \rightarrow infinite
- series resistance \rightarrow zero.
- * At low frequency,
 $C \rightarrow$ open circuits.

→ small circuit drain current is,

$$I_{ds} = g_m \cdot V_{gs} \quad \text{--- (1)}$$

→ effect of source series resistance can be determined using,

$$I_{ds} = g_m \cdot V_{gs}' \quad \text{--- (2)}$$

(a) $I_{ds} = \left(\frac{g_m}{1 + g_m r_s} \right) \cdot V_{gs} = g_m' V_{gs} \quad \text{--- (3)}$

$$V_{gs} = V_{gs}' (1 + g_m r_s)$$

$$g_m' = \frac{V_{gs}}{(1 + g_m r_s)}$$

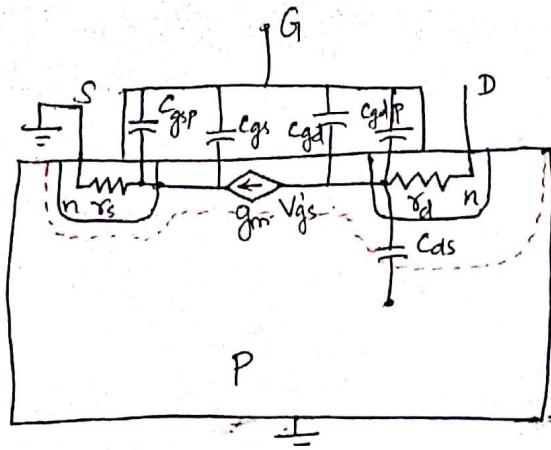
Frequency limitation factors,

1. channel transit time ($t_{tr} = \frac{L}{V_s}$)

2. Capacitance charging time.

Equivalent Circuit of MOSFET.

* Both source and substrate \rightarrow grounded.



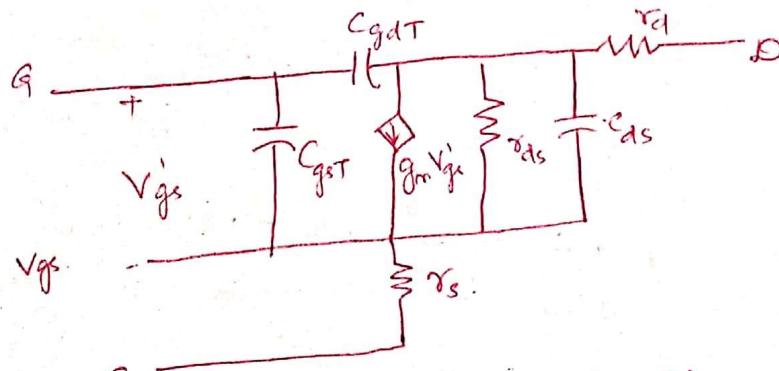
* C_{gs} & C_{gd} \rightarrow gate-to-source and gate-to-drain capacitances.

* C_{gsp} & C_{gdp} \rightarrow parasitic capacitances.

* C_{ds} \rightarrow drain-to-substrate capacitance.

* R_{SS} R_D \rightarrow Source and drain series resistances.

n-channel MOSFET.



V'_gs \rightarrow internal gate-to-source voltage that controls I_D .

C_{gsT}, C_{gdT} \rightarrow total capacitances.

γ_{ds} \rightarrow slope of I_D vs V_{DS} .

Fig: Small signal equivalent circuit.

* Drain current is given by,

$$I_D = g_m \cdot V'_{gs}$$

\rightarrow relation b/w V_{gs} and V'_{gs} is,

$$V_{gs} = V'_{gs} + (g_m \cdot V'_{gs}) \cdot r_s = (1 + g_m \cdot r_s) \cdot V'_{gs}$$

$$\therefore I_D = \left(\frac{g_m}{1 + g_m \cdot r_s} \right) \cdot V_{gs} = g_m \cdot V_{gs}$$

FINFET

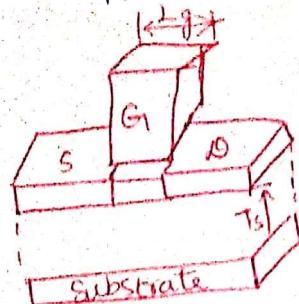
→ new multi-gate or trigate arch. \Rightarrow "FinFET"

fin \rightarrow narrow channel.

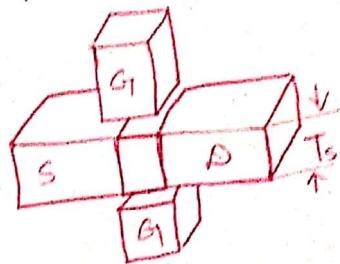
Technology:

→ reduce leakage current by keeping the gate capacitance in closer proximity to whole of the channel.

* two possible structures proposed.



Ultra-thin body (UTB)

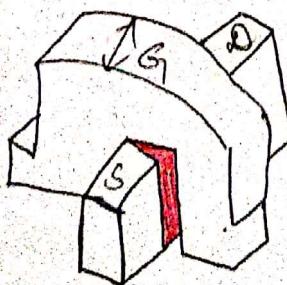


Dual gate (DG).

- * Rotating the DG structure, which has potential to provide the lowest gate leakage current.
- enables easier manufacturing.

- * Modern FinFETs are 3D structures.

- excellent control of conducting channel by gate
- very little current is allowed to leak
- allows of use of lower threshold voltage.
- optimal switching speeds and power.



Adv.

- Improved frequency performance
- Reduced capacitance
- Higher drive current
- Noise minimized

Drawbacks

- Poor thermal response
- Bulk Pn size.

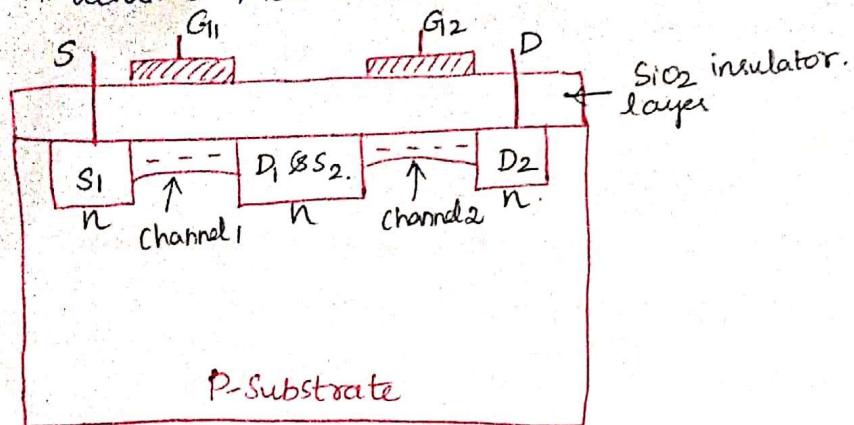
APP

1. Ring oscillators
2. Current Mirrors
3. OP-AMPS

DUAL-GATE MOSFET

→ N-channel enhancement type, dual insulated gate FET.

* utilises MOS construction.



→ has tetrode configuration.

↳ both gates control the current.

→ used for small-signal devices in RF applications.

→ reduces gain loss.

Maximum Ratings ($T = 25^\circ\text{C}$)

<u>Parameter</u>	<u>Symbol</u>	<u>Ratings</u>	<u>Unit</u>
Drain-source voltage	V_{DS}	10	V
Drain-current	I_D	30	mA
Gate 1 current	I_{G1}	± 10	mA
Total power dissip.	P_{total}	200	mW.
Storage temp.	T_S	$-65 \leq 150$	°C
Junction temp.	T_j	150	°C

Features

→ Two AGC amplifiers in a single package

→ Integrated gate protection diodes.

→ High AGC range, high gain, low noise.

App.

→ I/P stage for UHF & VHF tuners

→ communication equipments.

Adv

1. Reduction of I_{off} .

2. high current drive capability

3. Better uniformity of silicon channel thickness

Disadv

1. fabrication is difficult

2. Front and back gate cannot be independently biased.

UNIT-III

CURRENT EQUATION FOR JFET

- * Derivation of ideal drain current equation for JFET in depletion mode is complex and a good approx. is made to I-V characteristics for deriving drain current when the JFET is biased in saturation region.

* Unlike BJT, there is no linear relationship b/w input and output quantities for JFET.

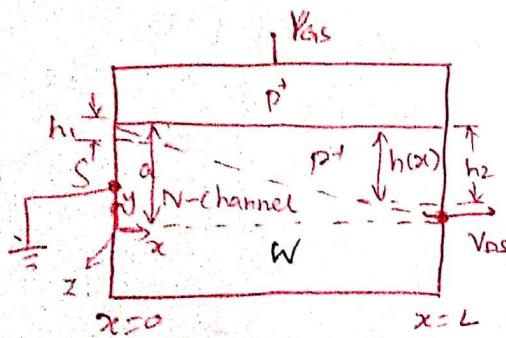
* The relationship b/w I_D and V_{GS} is,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 \quad \text{--- (1)}$$

where,

$I_{DSS} \rightarrow$ saturation current when $V_{GS} = 0$.

* An N-channel JFET is considered with geometry.



* differential resistance of channel at a point x in the channel, by considering half of the two-sided symmetrical geometry, is given by,

$$dR = \frac{\rho dx}{A(x)} \quad \text{--- (2)}$$

Where,

$\rho \rightarrow$ resistivity.

$A \rightarrow$ cross-sectional area.

* By neglecting minority carrier holes in N-channel, the channel resistivity is given by,

$$\rho = \frac{1}{\epsilon \mu_n N_D} \quad \text{--- (3)}$$

* Cross-sectional area is given by,

$$A(x) = (a - h(x))W \quad \text{--- (4)}$$

Substitute, ③ & ④ in ②, the differential resistance of channel is given by,

$$dR = \frac{dx}{\epsilon \mu_n N_D (a - h(x)) W} \quad ②$$

* differential voltage across a differential length 'dx' can be written as,

$$dV(x) = I_{D1} \cdot dR \quad ③$$

where, $I_{D1} \rightarrow$ constant through channel.

Substitute, ③ in ⑥, we get

$$dV(x) = \frac{I_{D1} \cdot dx}{\epsilon \mu_n N_D W (a - h(x))} \quad ⑦$$

$$\text{Therefore, } I_{D1} \cdot dx = \epsilon \mu_n N_D W (a - h(x)) \cdot dV(x) \quad ⑧$$

* Depletion width $h(x)$ is given by,

$$h(x) = \left\{ \frac{2q(V(x) + V_{bi} - V_{ds})}{e N_D} \right\}^{1/2} \quad ⑨$$

where, $V(x) \rightarrow$ Potential in channel due to V_{ds} .

Solving for $V(x)$ in ⑨ and differentiating $V(x)$ w.r.t $h(x)$

we get,

$$dV(x) = \frac{e N_D \cdot h(x) \cdot dh(x)}{\epsilon} \quad ⑩$$

Substitute ⑩ in ⑧, drain current through dx can be written as,

$$I_{D1} \cdot dx = \frac{\mu_n (e N_D)^2}{\epsilon} [a h(x) dh(x) - h(x)^2 \cdot dh(x)] \quad ⑪$$

* Drain current I_{D1} can then be obtained by integrating

⑪ along the channel length. Assuming Current and mobility are constant through channel, the drain current is given by,

$$I_{D1} = \frac{\mu_n (eN_D)^2 W}{2L} \left\{ \int_{h_1}^{h_2} a \cdot h \cdot dh - \int_{h_1}^{h_2} h^2 dh \right\} - \textcircled{12}$$

$$I_{D1} = \frac{\mu_n (eN_D)^2 W}{2L} \left\{ \frac{a}{2} (h_2^2 - h_1^2) - \frac{1}{3} (h_2^3 - h_1^3) \right\} - \textcircled{13}$$

For JFET, h_2 is depletion width at drain terminal is given by,

$$h_2 = \left[\frac{2\varepsilon(V_{DS} + V_{bi} - V_{GS})}{eN_D} \right]^{1/2} - \textcircled{14}$$

and h_1 is depletion width at source terminal,

$$h_1 = \left[\frac{2\varepsilon(V_{bi} - V_{GS})}{eN_D} \right]^{1/2} - \textcircled{15}$$

and pinch off voltage is given by.

$$V_{po} = \frac{ea^2 N_D}{2\varepsilon} - \textcircled{16}$$

where,
a → channel thickness.

Using $\textcircled{14}$, $\textcircled{15}$ & $\textcircled{16}$, $\textcircled{13}$ can be written as

$$I_{D1} = \frac{\mu_n (eN_D)^2 \cdot W a^3}{2\varepsilon L} \left\{ \frac{V_{DS}}{V_{po}} - \frac{2}{3} \left[\frac{V_{DS} + V_{bi} - V_{GS}}{V_{po}} \right]^{3/2} + \frac{2}{3} \left[\frac{V_{bi} - V_{GS}}{V_{po}} \right]^{3/2} \right\} - \textcircled{17}$$

* Pinch-off current I_{p1} for JFET is given by,

$$\boxed{I_{p1} = \frac{\mu_n (eN_D)^2 \cdot W a^3}{6\varepsilon L}}$$

* Using above eqn., drain current ($\textcircled{17}$) can be written as,

$$I_{D1} = I_{p1} \left\{ 3 \left(\frac{V_{DS}}{V_{po}} \right) - 2 \left[\frac{V_{DS} + V_{bi} - V_{GS}}{V_{po}} \right]^{3/2} + 2 \left[\frac{V_{bi} - V_{GS}}{V_{po}} \right]^{3/2} \right\} - \textcircled{18}$$

Eq. $\textcircled{18}$ is valid for $0 \leq |V_{GS}| \leq |V_{p1}|$ and $0 \leq |V_{DS}| \leq V_{DS}(\text{sat})$.

Eqn. ⑯ is the current voltage relationship for one sided n-channel JFET in non-saturation region.

* For two sided symmetrical JFET, the total drain current would be

$$I_{D2} = 2 I_{D1}$$

Eqn. ⑯ can be written as,

$$I_{D1} = G_{o1} \left\{ V_{DS} - \frac{2}{3} \sqrt{\frac{1}{V_{po}}} \left[(V_{DS} + V_{bi} - V_{Gis})^{3/2} - (V_{bi} - V_{Gis})^{3/2} \right] \right\} \quad - ⑯$$

where,

$$G_{o1} = \frac{\mu_n (eN)^2 Wa^3}{2 \epsilon_s L V_{po}} = \frac{e \mu_n \cdot N_d W a}{L} = \frac{3 I_{p1}}{V_{po}} \quad - ⑰$$

Channel Conductance is defined as,

$$g_d = \left. \frac{\partial I_{D1}}{\partial V_{DS}} \right|_{V_{DS} \rightarrow 0} \quad - ⑱$$

Taking derivative of eqn. ⑯, w.r.t. V_{DS} ,

$$g_d = \left. \frac{\partial I_{D1}}{\partial V_{DS}} \right|_{V_{DS} \rightarrow 0} = G_{o1} \left\{ 1 - \left(\frac{V_{bi} - V_{Gis}}{V_{po}} \right)^{1/2} \right\} \quad - ⑲$$

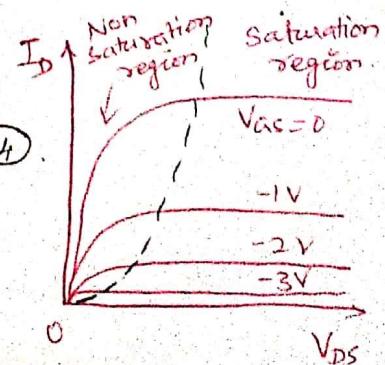
$g_d \rightarrow$ Controlled by gate voltage.

* Drain \rightarrow pinched off, for n-channel JFET when

$$V_{DS} = V_{DS(\text{sat})} = V_{po} - (V_{bi} - V_{Gis}) \quad - ⑳$$

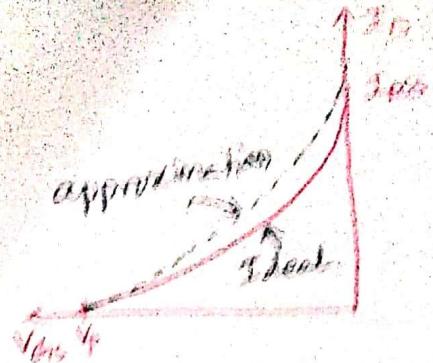
In saturation region, saturation drain current is,

$$I_{D1(\text{sat})} = I_{p1} \left\{ 1 - 3 \left(\frac{V_{bi} - V_{Gis}}{V_{po}} \right) \left[1 - \frac{2}{3} \sqrt{\frac{V_{bi} - V_{Gis}}{V_{po}}} \right] \right\} \quad - ㉑$$



* In saturation region, drain current is given to a good approximation,

$$I_D = I_{DSS} \left(1 - \frac{V_{DS}}{V_P} \right)^2$$



CURRENT EQUATIONS FOR MOSFET

→ relation b/w drain current and gate-to-source voltage, and drain-to-source voltage

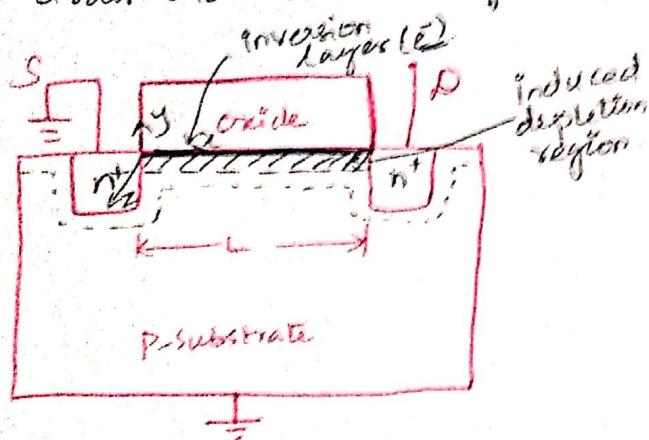


Fig: Geometry of a MOSFET.

* By Ohm's law, $J_x = \sigma E_x \quad \text{--- (1)}$

channel conductivity, $\sigma = e \mu_n n(y)$

where,
 $n(y) \rightarrow$ electron concentration.

* Total current is found by integrating J_x over the cross sectional area in y and z directions. Then,

$$I_x = \iint_{yz} J_x \cdot dy \cdot dz \quad \text{--- (2)}$$

we may write, $\sigma_0 = - \int e \cdot n(y) \cdot dy \quad \text{--- (3)}$

$\sigma_0 \rightarrow$ inversion layer charge per unit area and is a negative quantity.

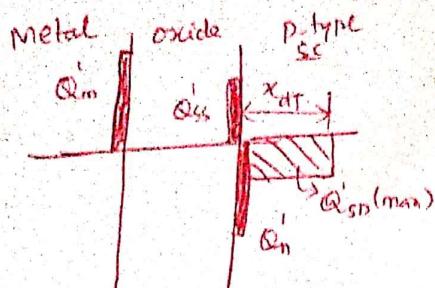
Assumption

1. Current in channel is due to drift only.
2. no current through gate oxide.
3. carrier mobility in channel is constant.
4. equivalent charge density at oxide-interface.

Eqn. ② becomes,

$$I_a = -W \mu_n Q'_n E_x - ④$$

- * Two concepts we will use in the I-V derivation are charge neutrality and Gauss's law.



Charge distribution in n-channel E-MOSFET.

* Using concept of neutrality,

$$Q_m + Q_{ss} + Q_{nt} + Q_{sd}^{(\max)} = 0 - ⑤$$

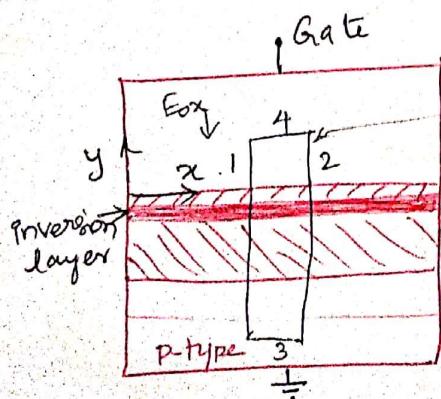
* Inversion layer charge and induced charge will be negative for this n-channel device.

* Gauss law can be written as,

$$\oint_S E_n dS = Q_T - ⑥$$

$Q_T \rightarrow$ total charge.

* Gauss law will be applied to closed surface.



Geometry for applying Gauss law.

* Consider surface 1 & 2,

$E_x \rightarrow$ constant along channel,

* E -field by surface 1 & 2 cancel each other.

* Surface 3 is in neutral p-region, so E -field is zero.

* Surface 4 is the only surface that contributes ⑥.

* Taking into account the direction of E -field in oxide,

⑥ becomes,

$$\oint_S E_n dS = -\epsilon_{ox} E_{ox} W dx = Q_T - ⑦$$

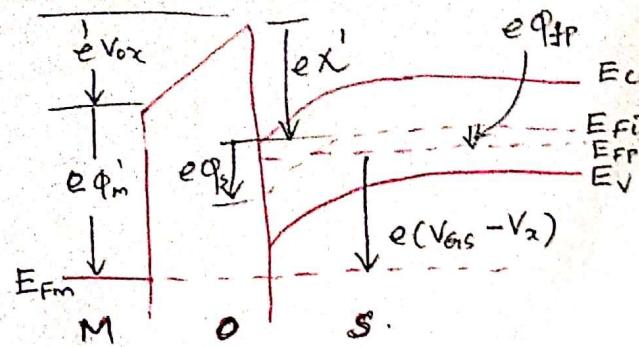
Total charge enclosed is,

$$Q_t = (Q_{ss} + Q_n + Q_{SD}(\max)) \cdot W \cdot dx \quad \textcircled{③}$$

Combining eqns. ② & ③, we have,

$$-E_{ox} \cdot E_{ox} = Q_{ss} + Q_n + Q_{SD}(\max) \quad \textcircled{④}$$

Now, we need expression for E_{ox} .



Ex: Energy band diagram through
MOS structure at point x

* Fermi level in P-type SC, is E_{FP} and fermilevel in the metal is E_{Fm} .

We have,

$$E_{FP} - E_{Fm} = e(V_{Gs} - V_x) \quad \textcircled{⑤}$$

Considering potential barriers, we can write,

$$V_{Gs} - V_x = (\Phi_m' + V_{ox}) - \left(x' + \frac{E_g}{2} - \Phi_s + \Phi_{fp} \right) \quad \textcircled{⑥}$$

* which can also be written as,

$$V_{Gs} - V_x = V_{ox} + 2\Phi_{fp} + \Phi_{ms} \quad \textcircled{⑦}$$

where, $\Phi_{ms} \rightarrow$ metal-SC work function difference
and $\Phi_s = 2\Phi_{fp}$ for inversion condition.

* The electric field in oxide is,

$$E_{ox} = \frac{V_{ox}}{t_{ox}} \quad \textcircled{⑧}$$

Combining eqns ①, ②, ⑦, we find that,

$$-E_{ox} E_{ox} = -\frac{E_{ox}}{t_{ox}} [(V_{Gs} - V_x) - (\Phi_{ms} + 2\Phi_{fp})]$$

$$= (Q_{ss} + Q_n + Q_{SD}(\max)) \quad \textcircled{⑨}$$

Inversion charge density, Q_n' from ⑨ can be

Substituted into eqn. ④

We obtain,

$$I_x = -W\mu_n C_{ox} \cdot \frac{dV_x}{dx} [(V_{GS} - V_x) - V_T] \quad (15)$$

where, $E_x = -\frac{dV_x}{dx}$ and $V_T \rightarrow$ threshold voltage.

* Now integrate (15) over length of channel,

we have,

$$\int_0^L I_x dx = -W\mu_n C_{ox} \int_{V_x(0)}^{V_x(L)} [(V_{GS} - V_T) - V_x] dV_x \quad (16)$$

* We assuming, I_D enters drain terminal and is a constant along the entire channel length.

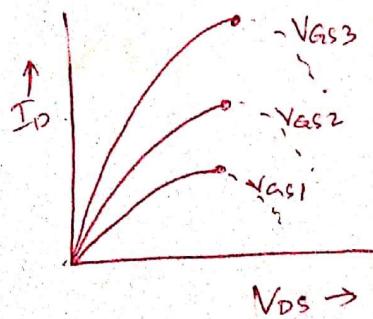
Letting $I_D = -I_x$, (16) becomes,

$$I_D = \frac{W\mu_n C_{ox}}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (17)$$

(17) is valid for $V_{GS} \geq V_T$ and for $0 \leq V_{DS} \leq V_{DS}(\text{sat})$.

* We can find the value of V_{DS} at peak current value from

$$\frac{\partial I_D}{\partial V_{DS}} = 0.$$



* Using (17), peak current occurs when

$$V_{DS} = V_{GS} - V_T \quad (18)$$

* V_{DS} is $V_{DS}(\text{sat})$, the point at which saturation occurs.

For $V_{DS} > V_{DS}(\text{sat}) \Rightarrow I_D$ is constant.

$$I_{D(\text{sat})} = \frac{W\mu_n C_{ox}}{2L} [2(V_{GS} - V_T)V_{DS}(\text{sat}) - V_{DS}^2(\text{sat})] \quad (19)$$

Using (18) for $V_{DS}(\text{sat})$,

$$(19) \Rightarrow I_{D(\text{sat})} = \frac{W\mu_n C_{ox}}{2L} (V_{GS} - V_T)^2 \quad (20)$$