UNIT - II BJT

NPN and PNP Configurations and their characteristics, Early Effect, current Equations, input and output characteristics of CE, CB, CC, h-parameter model, Hybrid - π model, Eber's moll model.

2.1 INTRODUCTION:-

A Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name Bipolar. The BJT is analogous to the vaccum triode and its comparatively small in size. It is used in amplifier and oscillator circuits and as a switch in digital circuits. It has wide application in computers, satellites and other modern communication systems.

In Shortly:

* Transistor is a three terminal device : Base, emitter and collector.

* It can be operated in three configurations : Common Base (CB), Common Collector (CC), Common Emitter (CE)

* According to configurations, it can be used for voltage as well as current amplification.

* Amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance.

* This concept of transfer of resistance "Transfer-Resis-tor" = Transistor.

2.2 TYPES OF TRANSISTORS :-

According to the charge carriers of current conduc-tions. transistors is classified into two types.

Transistors [Based on charge carriers].

- UJT
- BJT

1. UJT :-

→ Unipolar Junction Transistor

→ The current conduction is only due to one type of charge carriers. (ie) majority charge carriers.

2. BJT :-

→ Bipolar Junction Transistor.

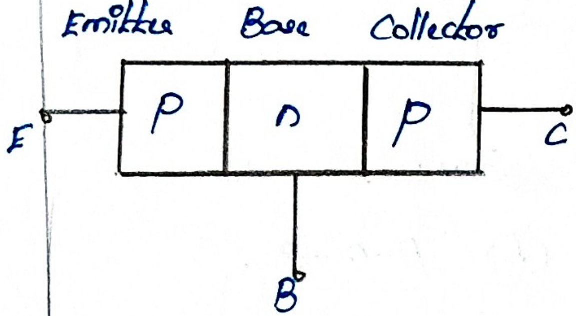
→ The Current Conduction is due to both type of charge carriers i.e holes and electrons.

→ output current is Controlled by input current and hence it is a "Current Controlled device"

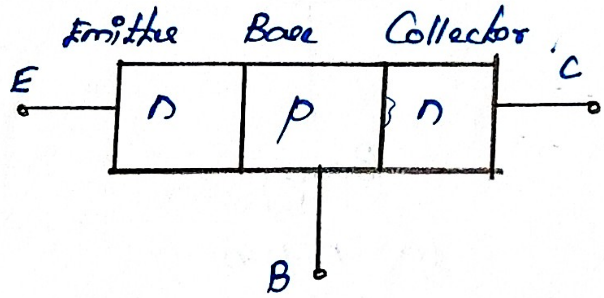
2.3 BJT - CONSTRUCTION :-

→ According to the arrangements of materials P, n type materials. BJT can clasified into types of two.

1. npn type   2. pnp type.



pnp type



npn type.

→ npn transistor is formed by Sandwiching a Single p-region between two n-regions.

→ pnp transistor is formed by Sandwiching a Single n-region between two p-regions.

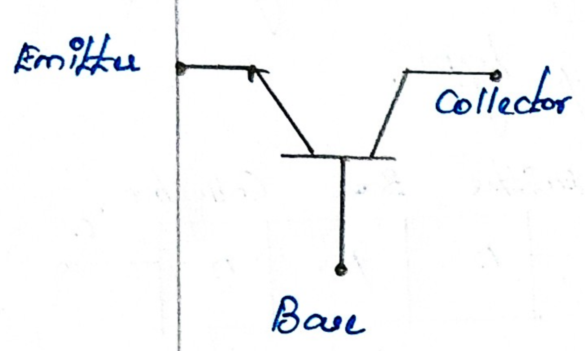
→ There are three terminals in both npn and pnp transistors are :-

1) Base
2) Emitter
3) Collector.

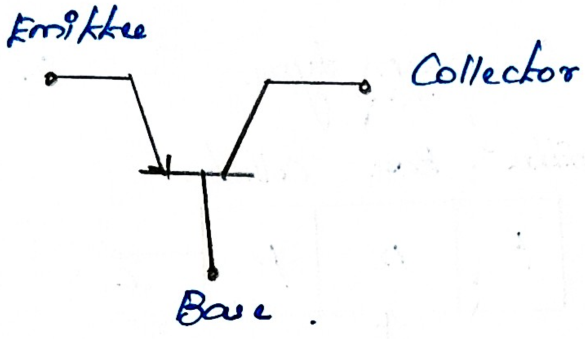
→ Middle region is base, which is very thin and lightly doped.

→ Emitter and collector regions are heavily doped. But the doping level in emitter is slightly greater than that of collector. So collector is moderately doped

2.3.1 TRANSISTOR SYMBOLS :



(a) n-p-n



(b) p-n-p.

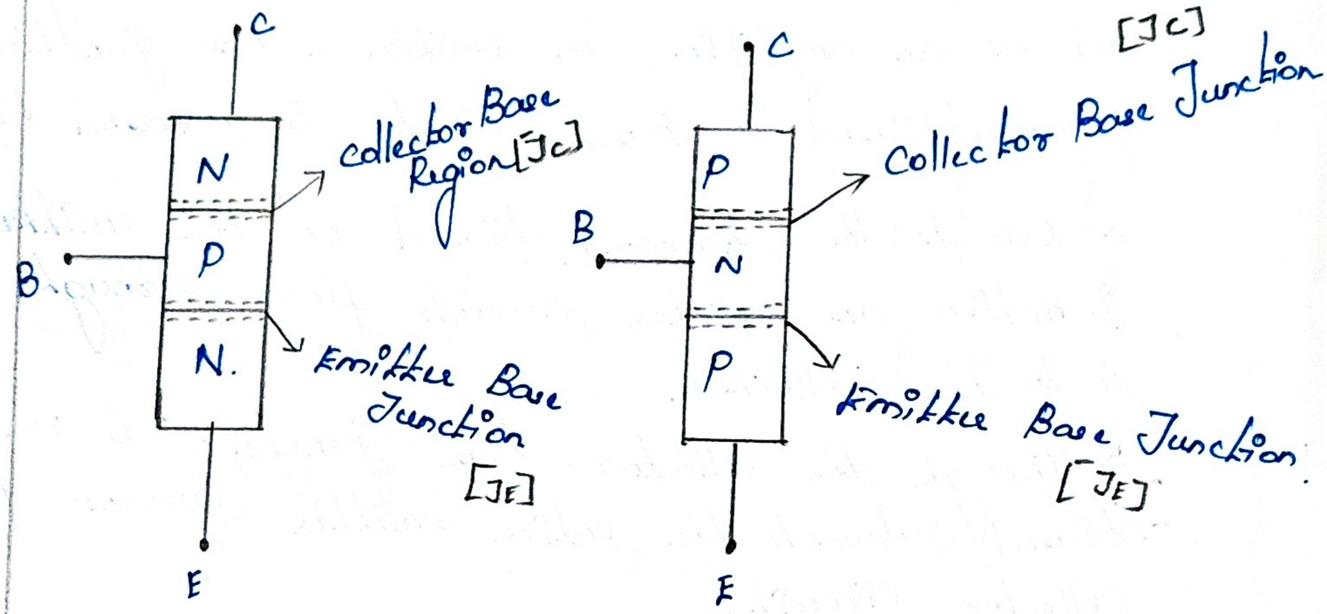
→ The arrow on the emitter indicates the conventional current which is opposite to the direction of electron current in emitter (or) the direction of current flow when the emitter base junction is forward biased.

→ Emitter is heavily doped so that it can inject a large number of charge carriers in to the base.

→ Base is very thin and also lightly doped. It passes most of the injected charge carriers from the emitter in to the collector.

→ Collector is moderately doped.

2.3.2 JUNCTIONS OF TRANSISTORS :-



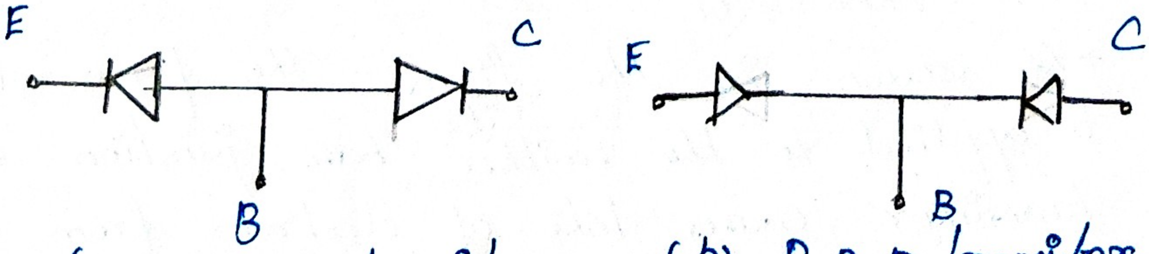
→ A BJT has two P-N Junctions.

→ One Junction is between emitter and base is called as emitter base junction. (or) Emitter Junction (J_E).

→ Another Junction is between collector and base is Called as Collector base junction (or) Collector Junction (J_C)

2.3.3. DIODE EQUIVALENT STRUCTURE OF TRANSISTOR :-

A transistor can be Considered as 2 P-N Junction diodes connected as back to back manner.



(a) n-p-n transistor. (b) p-n-p transistor.

Two-diode transistor analogy.

2.3.4 TRANSISTOR BIASING :-

→ To bias the transistor in its active region (i.e) act as an amplifier, the emitter - base junction is forward biased & Base - Collector is reversed biased.

→ Due to the forward biased on the emitter base junction an emitter current flows through the base in to the collector.

→ Though the collector - base junction is reverse biased, almost the entire emitter current flows the collector circuit.

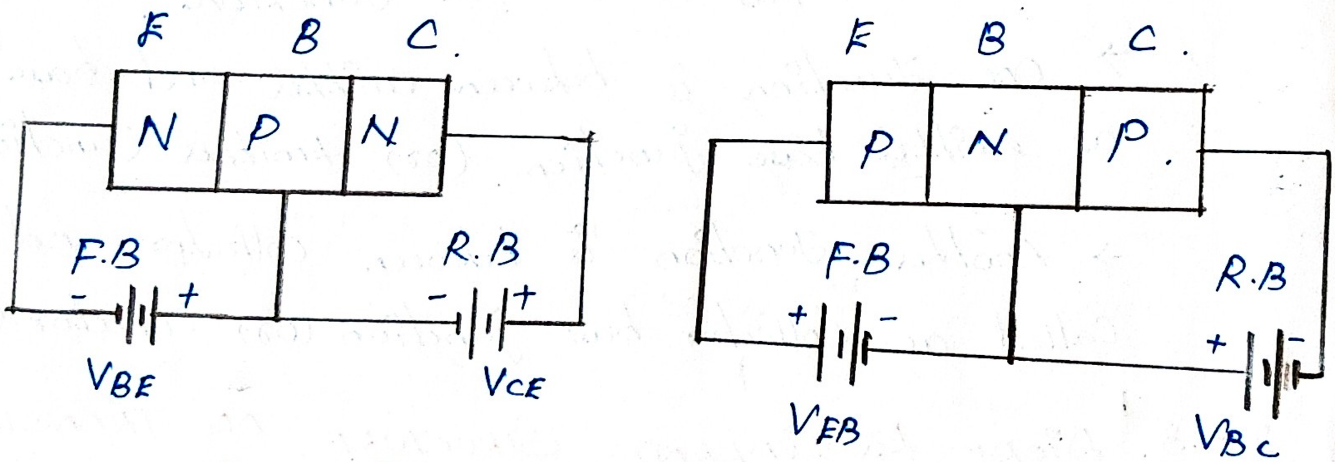


Fig - Transistor biasing (a) NPN transistor.
(b) PNP transistor.

2.3.5 OPERATIONS OF TRANSISTORS :-

NPN TRANSISTOR :-

→ As shown in the figure, the forward bias is applied to the emitter base junction of an NPN transistor causes lots of electrons from emitter region to crossover to the base region.

→ As the base is lightly doped with p-type impurity the number of holes in the base region is very small and hence the number of electrons that combines with holes in the p-type base region is also very small.

→ Hence a few electrons combines with holes to constitute a base current I_B. The remaining electrons (more than 95%) crossover into the collector region to constitute a collector current I_C. I_c.

→ Thus the base and collector current summed up gives the emitter current. (ie).

$$I_E = -(I_c + I_B).$$

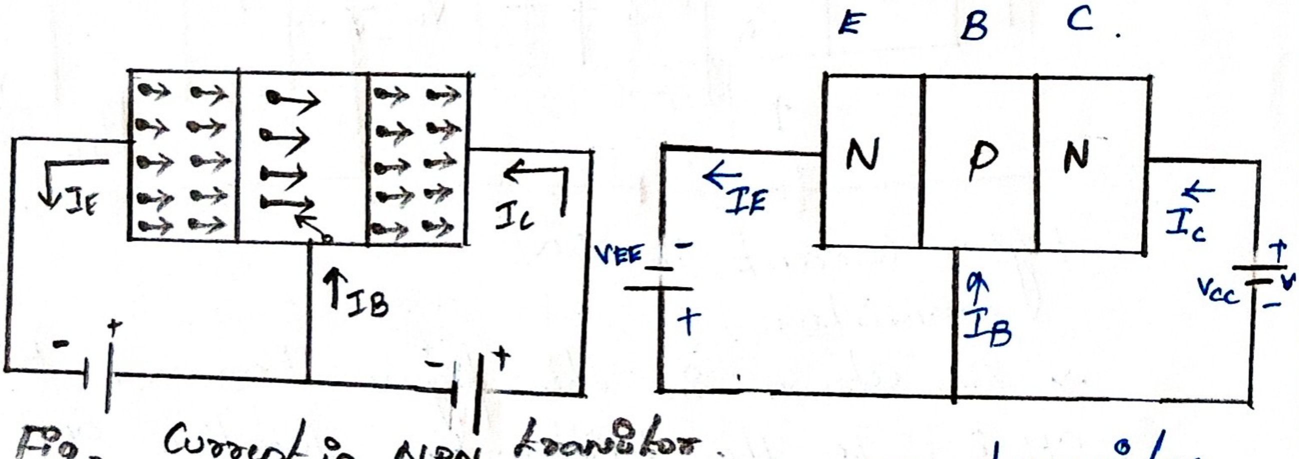


Fig- Current in NPN transistor.

→ In the external circuit of NPN transistor, the magnitudes of the emitter current I_E, the collector current I_c and the base current I_B are related by

$$I_E = I_c + I_B.$$

$\therefore I_C = I_{C\,majority} + I_{CO\,minority}$

→ $I_{CO\,minority}$ ⇒ minority current component called the leakage current. [I_C current with emitter terminal open - I_{CO}]

→ $I_{C\,majority}$ ⇒ Injected collector current due to majority carrier crossing the collector base junction.

OPERATION OF PNP TRANSISTOR :-

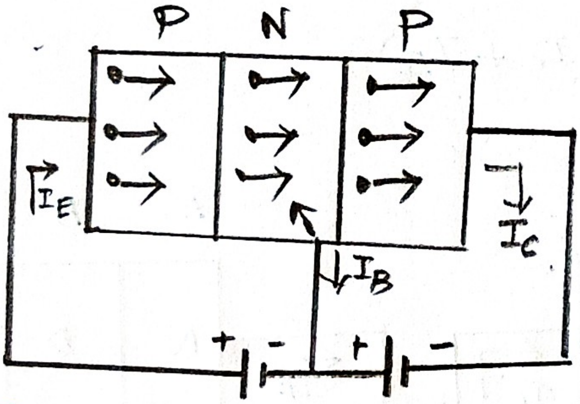
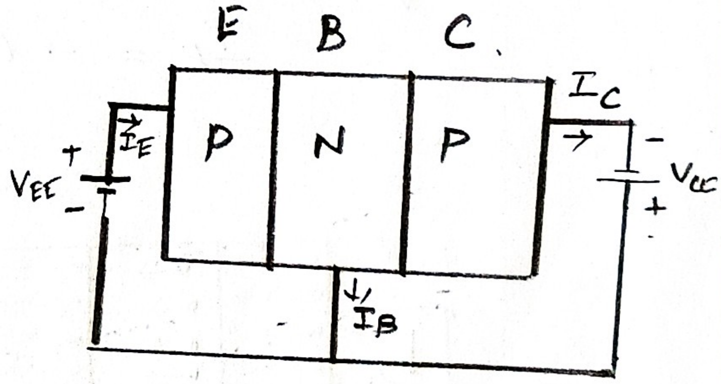


Fig (a) Current in PNP transistor



→ As shown in the figure Forward Bias is applied to the Emitter - Base Junction and Reverse Bias is applied to the Collector - Base Junction.

→ When Forward Bias is applied to Emitter - Base Junction causes a lot of holes move from emitter region to base region.

→ As the base is lightly doped the number of electrons (e^-) in this base region is very small.

→ Hence a few holes combined with electrons to constitute a base current I_B.

→ The remaining holes (more than 95%) cross over into the collector region to constitute a collector current I_C.

→ Thus the collector current and base current when summed up give the emitter current.

$$\therefore I_E = -(I_C + I_B).$$

→ In the external circuit of PNP bipolar junction transistor, the magnitudes of the emitter current I_E, the collector current I_C the base current I_B and the are related by

$$I_E = I_C + I_B.$$

2.3.6. OPERATING REGIONS AND BIAS CONDITIONS :-

The transistor can be operated in any of the mode / regions.

Region of operation	Base-Emitter (B-E) Junction	Base - collector (B-C) Junction	Application.
Saturation	F.B	F.B	BJT as switch
Cut off	R.B	R.B	BJT as switch
Forward Active	F.B	R.B	BJT as Amplifier
Inverse active	R.B	F.B	BJT in digital circuits

2.4 Types of Configurations :

→ When a transistor is to be connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal and third terminal is common to the input and output.

→ Depending upon the input, output and common terminal, a transistor can be connected in three configurations.

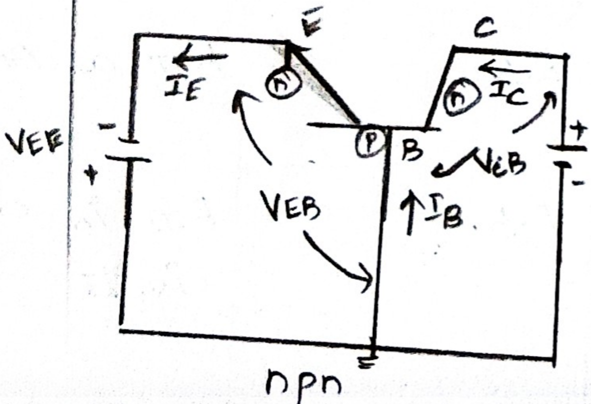
They are

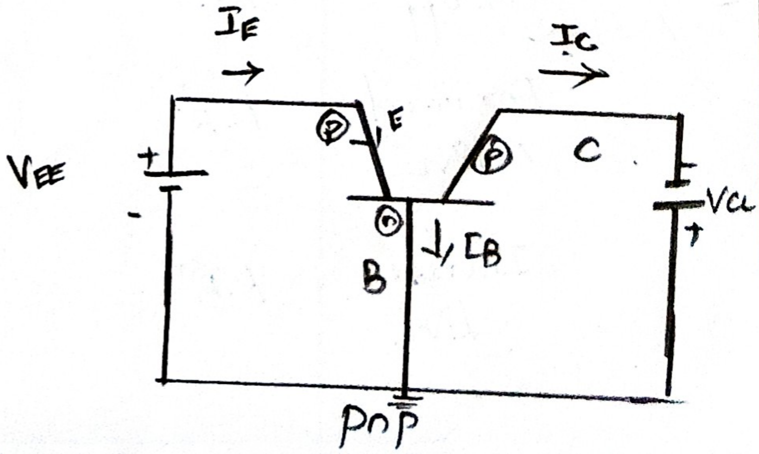
(i) Common Base (CB) Configuration
(ii) Common Emitter (CE) Configurations
(iii) Common Collector (CC) Configurations.

2.4.1. Common Base (CB) configurations :

→ This configuration is also called as grounded base configuration.

→ In this configuration emitter is the input terminal, collector is the output terminal and base is the common terminal.





2.4.1.1 Transistor characteristics:-

In general transistor has input and output characteristics for all the three CB, CC, CE Configurati-ons.

Static characteristics of NPN transistor in CB Configurations:-

a) Input characteristics:-

→ These curves give the relationship between input current and input voltage for a given output voltage.

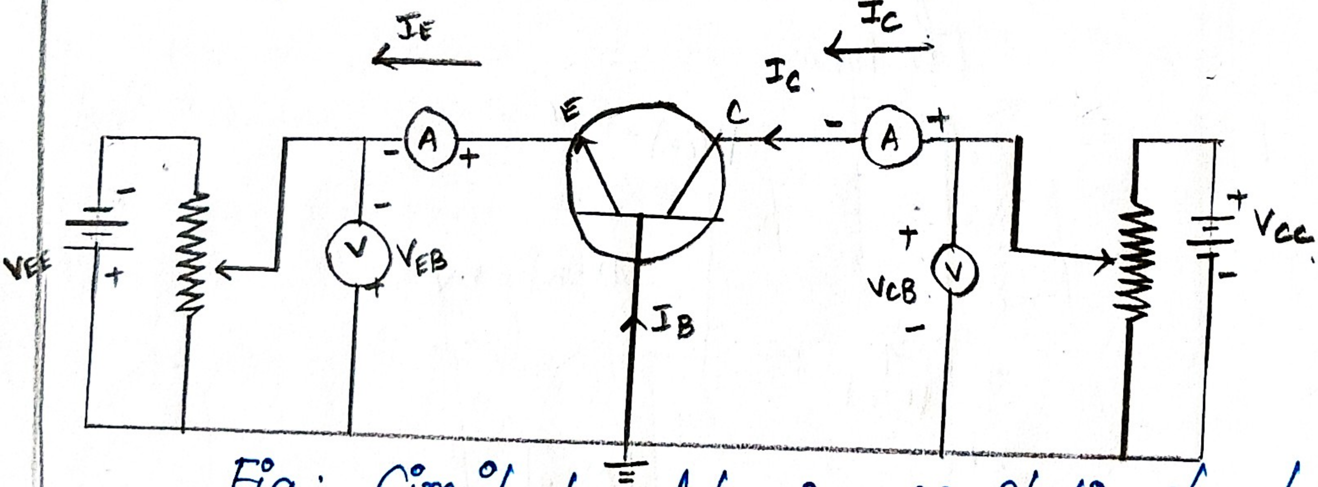


Fig: Circuit to determine CB Static characteristics.

→ To determine the input characteristics, the collector to base voltage (V_{CB}) is kept constant at zero, then V_{EB} is increased in steps and the corresponding emitter current (I_E) values are noted.

→ This procedure is repeated for higher fixed values of V_{CB}.

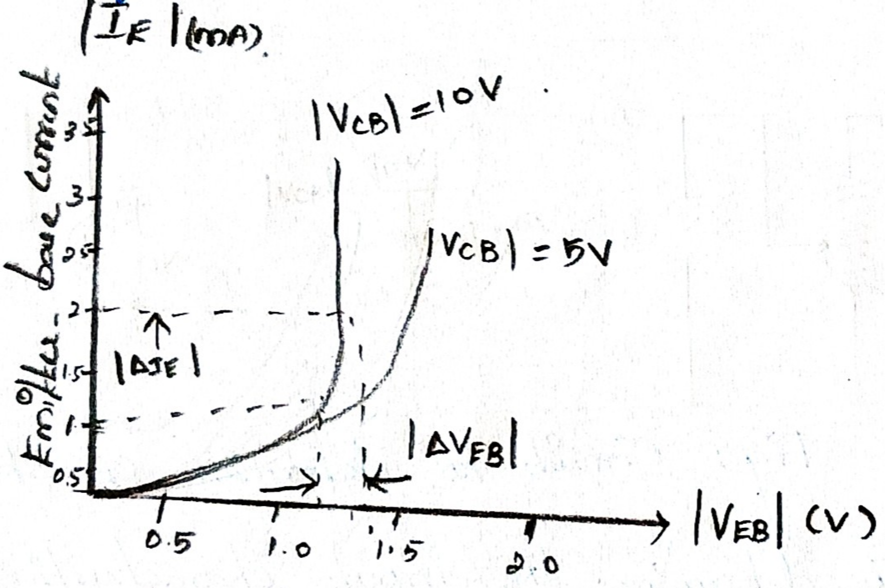
→ A graph is drawn between I_E and V_{EB} at constant V_{CB}.

→ when V_{CB} is zero, emitter-base junction behaves as a forward biased diode. So, that the I_E increases rapidly with small increase in V_{EB}. Thus the input resistance (r_i) is very small.

→ when V_{CB} is increased, keeping V_{EB} constant, the width of the base region will decrease.

→ It reduces the chances of recombinations of electrons with the holes in the base region.

→ Hence, I_E current increases, the curve shift towards left as V_{CB} is increased.



Emitter - Base Voltage.

→ For a fixed V_{EB}, I_E increases when V_{CB} is increased.

→ The dynamic i/p resistance is a ratio of change in emitter - base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector - base voltage (V_{CB}).

i/p impedance = $h_{ib} = r_i = \frac{\Delta V_{BE}}{\Delta I_B}\Big|_{V_{CB} = \text{constant}}$.

Output characteristics :-

→ To determine the output characteristics, the I_E is kept constant by adjusting the V_{EE}

→ Then V_{CB} is increased in equal steps and I_C is noted.

→ This procedure is repeated for different fixed values of I_E

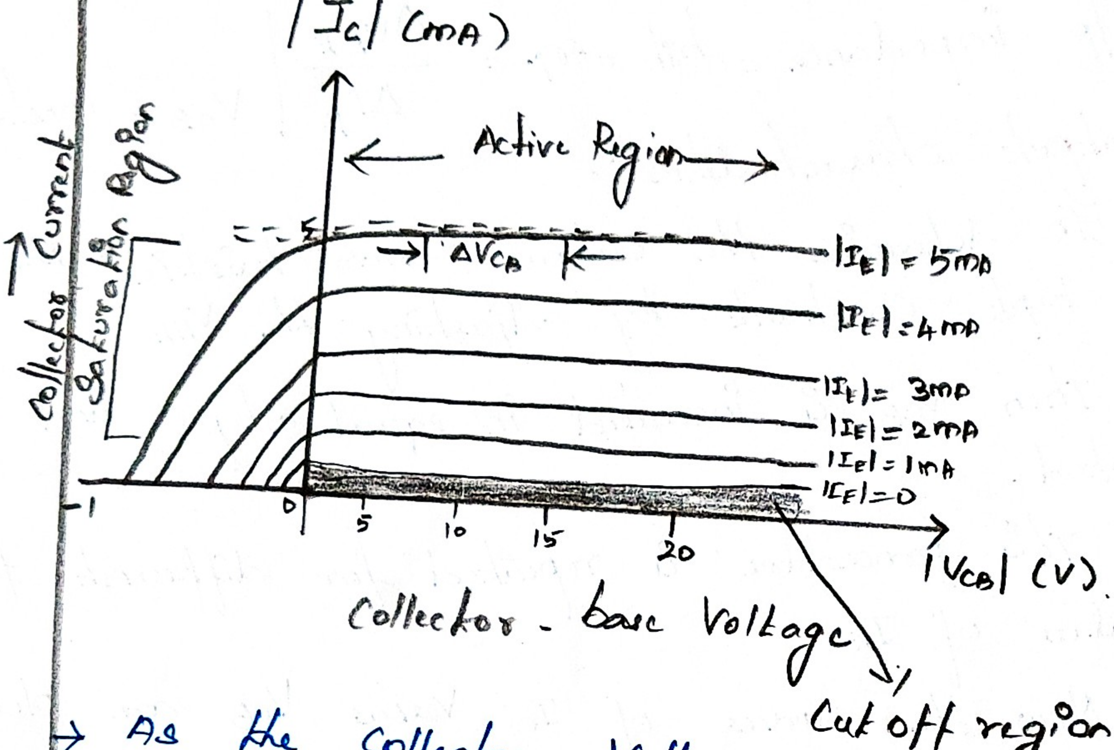
→ Now the curves of I_C versus V_{CB} are plotted for constant I_E

→ From the characteristics, it is seen that for a constant I_E, I_C is independent of V_{CB} and the curves are parallel to the axis V_{CB}.

→ I_C flows even when V_{CB} is equal to zero

→ As the Emitter - Base Junction is Forward Biased, the majority carriers i.e electrons from the emitter are injected into the base region.

→ Due to the action of internal potential barrier of the reversed biased collector- Base Junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.



→ As the collector voltage V_{CC} is made to increase the Reverse Bias, the depletion region width between collector and base tends to increase, with the result that effective width of the base decrease.

→ The dependency of base - width on collector to base voltage is known as "Early Effect (or) Base width modulation."

→ For extremely large voltages, the effective base width may be reduced to zero. causing breakdown in the transistor.

→ This phenomenon is called "punch through (or) Reach through".

→ The output characteristics has three regions Active, cutoff and Saturation.

a) Active Region :-

→ $J_E \rightarrow$ F.B , $J_C \rightarrow$ RB

→ $I_C \simeq I_E$ and transistor works as an amplifier I_C is almost constant.

$$\left.\begin{array}{l}\text{dynamic o/p}\\\text{Resistance, } R_o\end{array}\right\} = \left.\frac{\text{change in } V_{CB}}{\text{change in } I_C}\right|_{I_E = \text{Constant}}$$

$$R_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{constant}}.$$

$$\frac{1}{R_o} = h_{ob} = \text{o/p admittance}.$$

→ I_C independent of V_{CB} and transistor can be said to work as constant-current Source. This provides very high dynamic o/p resistance.

b) Saturation Region :-

→ J_E & J_C both are Forward Biased

→ I_C is independent of I_E

→ I_C decreases rapidly as V_{CB} becomes more negative.

c) Cut off Region :-

→ The Region below the curve $I_E = 0$ is known as cut off region, where I_C is nearly zero and both J_E & J_C are reverse biased.

→ DC current gain α_{dc} (or) α (or) Large Signal current gain of CB configuration.

$$\therefore \alpha_{dc} = \frac{I_C}{I_E} = \frac{\text{Collector current}}{\text{Emitter Current}} = \frac{\text{o/p current}}{\text{I/p current}}.$$

$$\therefore I_C = I_{C\,majority} + I_{CBO\,minority}$$

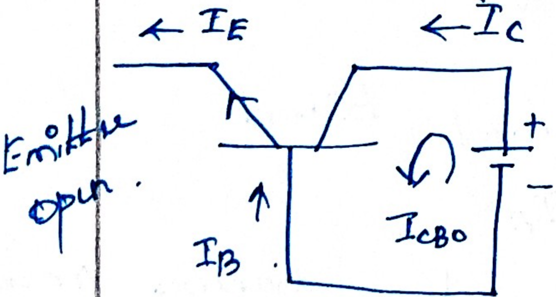
$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha I_E + I_{CBO} \qquad [I_C < I_E]$$

↳ Reverse Saturation Current, (negligibly Small) (or) Leakage current.

→ Kl.K.T

$I_E = I_B + I_C$



→ I_{CO} is order of nA for Si & order of mA for Ge.

↳ I_{CBO} is temperature Sensitive and it doubles for every 10°c rise in temperature.

↳ α 0.90 to 0.995 it is always <1.

→ Thickness of base Larger, Smaller the values of α.

→ AC current gain (or) current amplification factor (or) Common base short ckt current gain (or) small signal current gain (or) h_{fb}.

(or) forward current gain.
$$\alpha_{ac} = \frac{\text{change in output current}}{\text{Change in i/p current}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{Constant}}$$

→ For all practical purposes, dc current gain is equal to ac current gain ($\alpha_{dc} \simeq \alpha_{ac}$).

CB Transistor parameters (or) Hybrid parameters :- (or) h- parameters :-

→ The slope of the CB characteristics will give the following 4 transistor parameters.

a) Input impedance (h_{ib}).

$$h_{ib} = \left.\frac{\text{Change in (i/p) emitter Voltage}}{\text{change in (i/p) emitter current}}\right|_{\substack{\text{(o/p) Collector-base voltage} \\ V_{CB} = \text{Constant}}}$$

$$\Rightarrow \quad h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} = \text{Constant}}$$

⇒ It is the slope of CB i/p characteristics I_E Versus V_{EB}.

→ h_{ib} value ranges from $20\,\Omega$ to $50\,\Omega$.

b) Output admittance (h_{ob}).

$$h_{ob} = \frac{\text{change in (o/p) collector current}}{\text{change in (o/p) collector voltage}} \Bigg| \begin{array}{l}\text{i/p emitter} \\ \text{current} \\ I_E = \text{constant}\end{array}$$

$$\Rightarrow h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}} \Bigg| I_E = \text{Constant}.$$

→ It is the slope of CB o/p characteristics I_C versus V_{CB}.

→ h_{ob} value ranges from 0.1 to 10 μ℧

c) Forward current gain (h_{fb}).

$$h_{fb} = \frac{\text{change in (o/p) collector current}}{\text{change in (i/p) emitter current}} \Bigg| \begin{array}{l}\text{(o/p) collector} \\ \text{-base voltage} \\ V_{CB} = \text{constant}\end{array}$$

$$\Rightarrow h_{fb} = \frac{\Delta I_C}{\Delta I_E} \Bigg| V_{CB} = \text{Constant}.$$

⇒ It is the slope of I_C Vs I_E

⇒ h_{fb} varies from 0.9 to 1.0.

d) Reverse Voltage gain (h_{rb}).

$$h_{rb} = \frac{\text{change in (i/p) emitter voltage}}{\text{change in (o/p) collector voltage}} \Bigg| \begin{array}{l}\text{(i/p)} \\ \text{emitter} \\ \text{current} \\ I_E = \text{Constant}\end{array}$$

$$\Rightarrow h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \Bigg| I_E = \text{Constant}$$

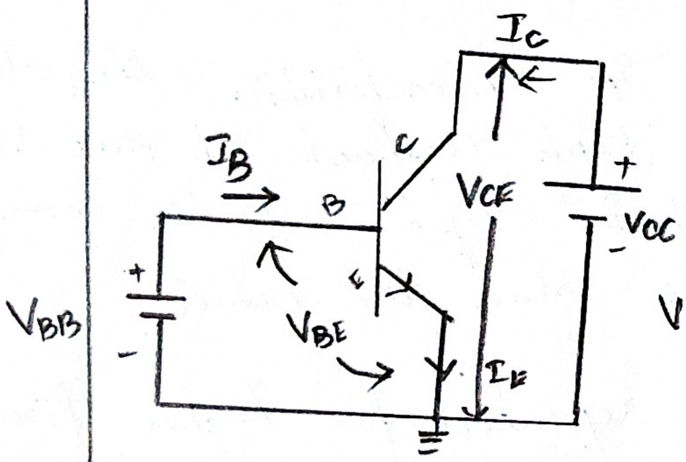
→ It is the slope of V_{EB} Vs V_{CB} curve.

→ Typical value of h_{rb} is order of 10^{-5} to 10^{-4}

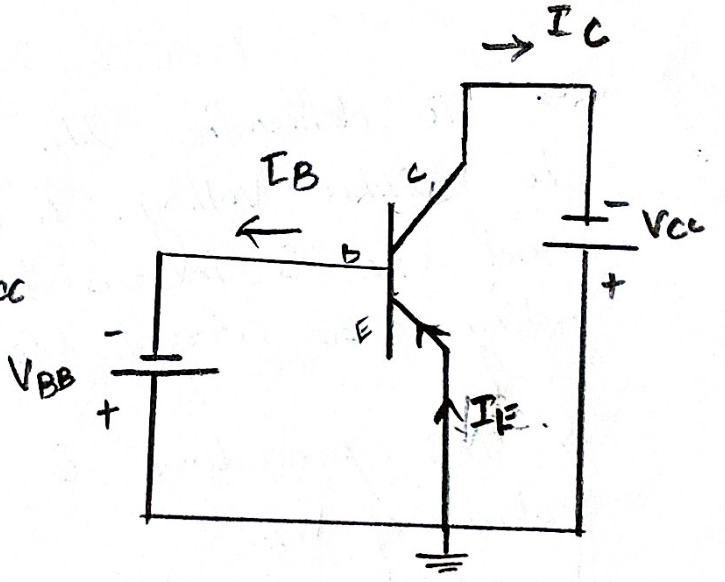
2.4.2 CE configurations :- (CE)

→ This is also called grounded emitter configuration.

→ In this configuration, base is the i/p terminal, collector is the o/p terminal and emitter is the common terminal.

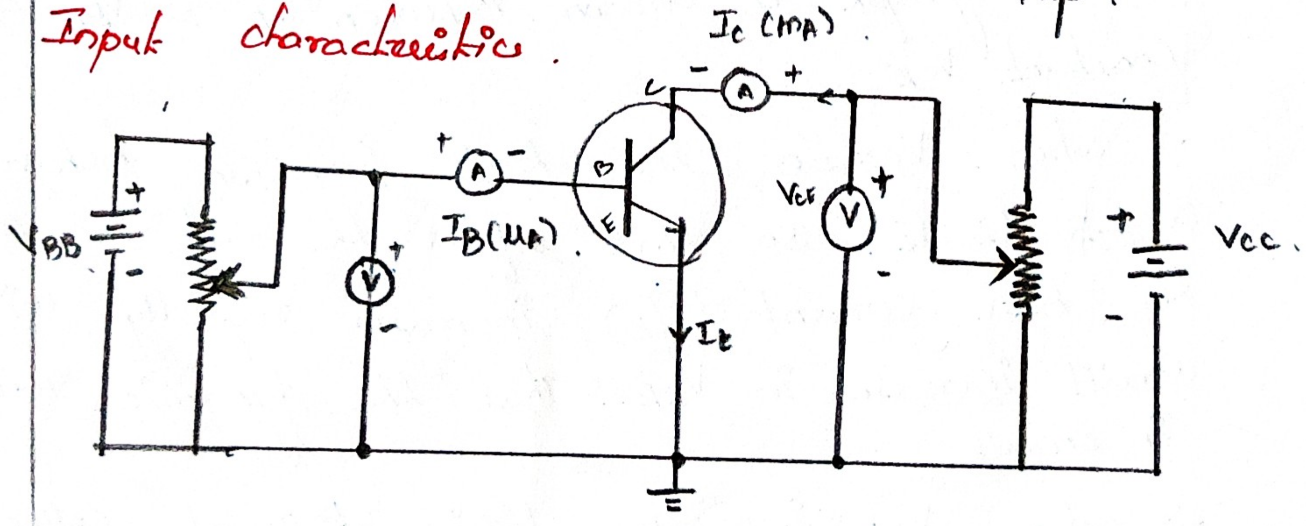


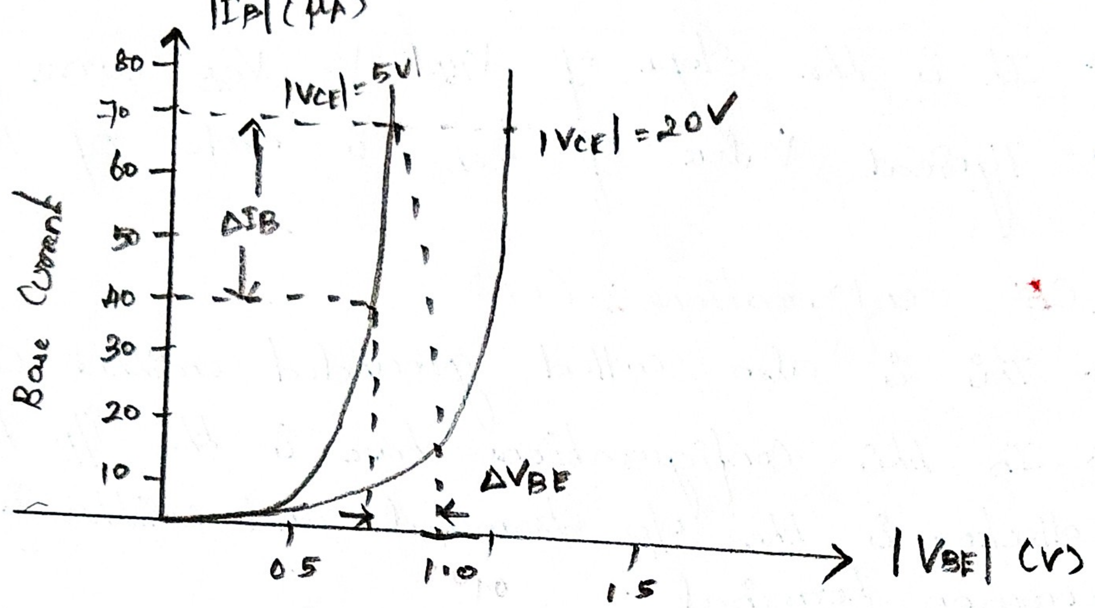
npn.



Pnp.

Input characteristics.





→ To determine the i/p characteristics, the collector to emitter voltage is kept constant at zero volt and V_{BE} is increased in steps and the correspon-ding base current (I_B) values are noted.

→ This procedure is repeated for higher fixed values of V_{CE}

→ The graph is drawn between I_B & V_{BE} at constant V_{CE}

→ When $V_{CE} = 0$, the E-B junction behaves as a F.B diode. So that, after the cut in voltage, the base current (I_B) increases rapidly with small increase in V_{BE}. Thus the dynamic resistance is small.

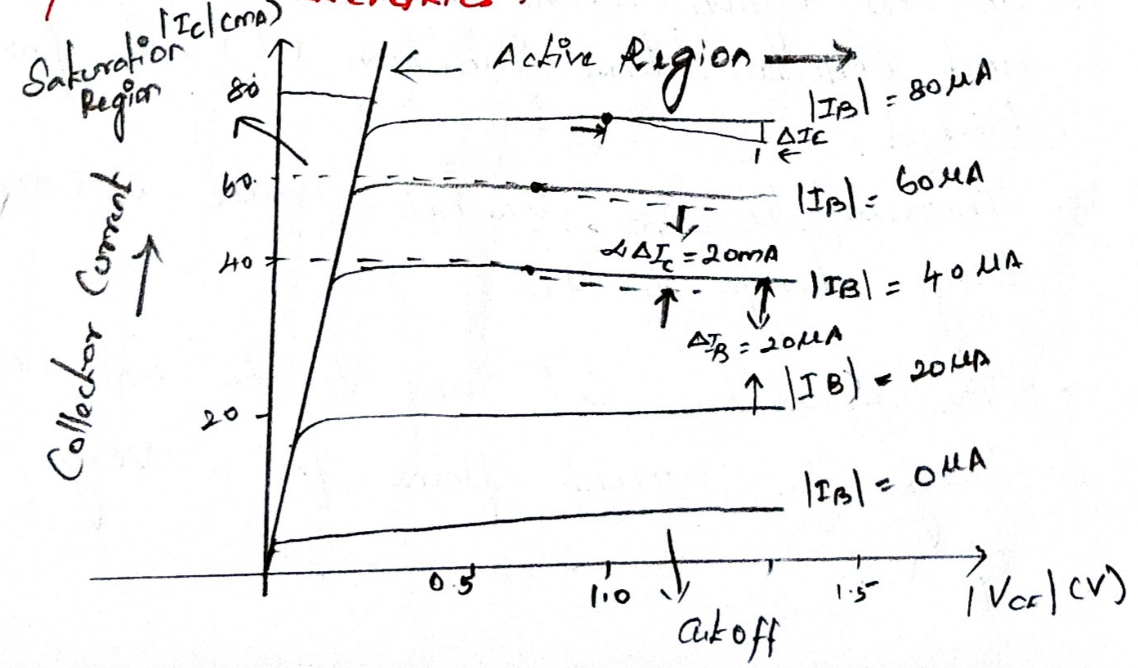
→ When V_{CE} is increased (i.e) R.B at collector emitter ~~Base~~ junction is increased the width of the ~~Base~~ depletion region at the R.B collector-emitter junction will increase.

- → Hence the effective width of base will decrease.
- → So, it reduces the chances of recombination of electrons in the emitter with the holes in base region.
- → ∴ Base current (I_B) decreases. The curve shifts towards right as V_{CE} increases. For a fixed value of V_{BE}, I_B decreases as V_{CE} is increased.
- → The dynamic i/p resistance is ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}).

$$\text{i/p impedance} = h_{ie} = r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{Constant}}$$

- → The value of r_i in CE configuration is greater than the value of r_i in CB configuration.

Output characteristics :-



→ To determine the output characteristics, I_B is kept constant by adjusting V_{CC}

→ Then V_{CE} is increased in equal steps and I_C is noted.

→ I_C reaches to a saturation value when V_{CE} is about 1V

→ When V_{CE} is increased further. I_C is slightly increase and I_B decrease.

→ When I_B is zero, a small I_C current exists. This is called leakage current. (I_{CEO}).

→ For all practical purpose, I_C is zero when $I_B = 0$ Under this conditions the transistor is said to be cut off.

→ The o/p characteristics may be divided into three regions: Saturation, Active and cutoff

a) Saturation Region :

→ In this region both emitter-base junction (J_E) and collector-base junction (J_C) are forward Biased.

→ Increase in I_B does not cause a corresponding large change in I_C

→ The transistor is said to be 'ON' condition i.e. large I_C current flows for a very low value of V_{CE}

b) Cut off Region :-

→ The Region below the curve for $I_B = 0$ is called as cutoff Region. In this region both J_E, J_C are Reverse biased.

→ I_C becomes almost zero and V_{CE} almost equals to V_{CC}.

→ The transistor is said to be in OFF condition.

(c) Active Region :-

→ In this region, J_E is FB and J_C is RB

→ The central region where curves are uniform in spacing and slope is called active region.

→ In this transistor is to be used as linear amplifier, it should be operated in active region.

$$\text{dynamic o/p resistance, } R_o = \left.\frac{\text{change in } V_{CE}}{\text{change in } I_C}\right|_{I_B = \text{constant}}$$

$$\Rightarrow R_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant}}.$$

$$\frac{1}{R_o} = h_{oe} = \text{o/p admittance}.$$

DC current gain β_{dc} (or) β (or) Large Signal current gain of CE configuration.

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{\text{Collector current}}{\text{Base current}}$$

AC current gain (or) Current amplification factor β (or) Small signal current gain (or) h_{fe} (or) forward current gain.

$$\beta_{ac} = \frac{\text{change in o/p current}}{\text{change in i/p current}} = \left.\frac{\Delta I_C}{\Delta I_B}\right| V_{CE} = \text{constant.}$$

Relationship between α, β:

W.k.T

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{---} \quad (1)$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{---} \quad (2)$$

$$\Delta I_E = \Delta I_B + \Delta I_C \quad \text{---} \quad (3)$$

from (3)

$$\Delta I_B = \Delta I_E - \Delta I_C \quad \text{---} \quad (4)$$

Sub eqn (3) in (1)

$\Delta I_E = \Delta I_B + \Delta I_C$ in (1)

$$\alpha = \frac{\Delta I_C}{\Delta I_B + \Delta I_C}.$$

∴ Numerator and Denominator divided by I_B

$$\alpha = \frac{\Delta I_C / \Delta I_B}{1 + \Delta I_C / \Delta I_B} \Rightarrow \boxed{\alpha = \frac{\beta}{1+\beta}}$$

$\boxed{\text{where } \Delta I_C/\Delta I_B = \beta}$

lllly sub (4) in (2)

$$\Delta I_E - \Delta I_C = \Delta I_B \text{ in } (2)$$

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}.$$

∴ Numerator and denominator divided by ΔI_E

$$\beta = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta E - \Delta I_C}{\Delta I_E}} = \frac{\Delta I_C / \Delta I_E}{1 - \frac{\Delta I_C}{\Delta I_E}}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \quad \boxed{\text{where } \alpha = \Delta I_C / \Delta I_E}$$

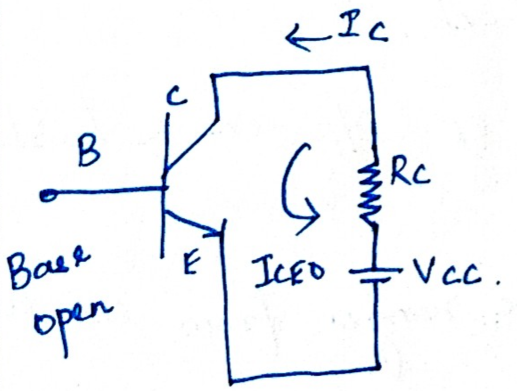
Leakage current:

→ when the base is open, a leakage current flows from emitter to collector terminal. It is denoted by ICEO.

$$\boxed{I_{CEO} = I_{CBO} + \beta I_{CBO} = (1+\beta) I_{CBO}}.$$

∴ Total collector current $I_C = \beta I_B + I_{CEO}$.

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$



∴ I_{CEO} →

O → Base open

CE → collector to emitter leakage current (or) Reverse saturation current.

Transistor parameters (or) CE hybrid parameters: (h- parameters):

→ The slope of the CE characteristics will give the following 4 transistor parameters.

a) Input Impedance (h_{ie}).

$$h_{ie} = \left.\frac{\text{change in (i/p) base Voltage}}{\text{change in (i/p) base current}}\right| \text{(o/p) collector Voltage } V_{CE} = \text{Constant}$$

$$\Rightarrow h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{Constant}}.$$

⇒ It is the slope of CE i/p characteristics I_B Vs V_{BE}.

⇒ h_{ie} range from 500 to 2000 Ω k

(b) output admittance (h_{oe})

$$h_{oe} = \left.\frac{\text{change in (o/p) collector Current}}{\text{change in (o/p) Collector Voltage}}\right| \text{(i/p) base current, } I_B = \text{Constant}.$$

$$\Rightarrow h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B = \text{Constant}}.$$

→ It is the slope of CE o/p characteristics I_C Vs V_{CE}.

→ Typical values of h_{oe} ranges from 0.1 to 10 μ℧

c) Forward current gain (h_{fe}):

$$h_{fe} = \frac{\text{change in (o/p) collector current}}{\text{change in (i/p) base current}} \Bigg|_{\substack{\text{(o/p) collector voltage} \\ V_{CE} = \text{constant.}}}$$

$$\Rightarrow h_{fe} = \frac{\Delta I_C}{\Delta I_B}\Bigg|_{V_{CE} = \text{constant.}}$$

→ It is the slope of I_C Vs I_B curve.

→ Typical value of h_{fe} varies from 20 to 200

d) Reverse Voltage gain (h_{re}).

$$h_{re} = \frac{\text{change in (i/p) base voltage}}{\text{change in (o/p) collector voltage}}\Bigg|_{I_B = \text{constant}}$$

$$\Rightarrow h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\Bigg|_{I_B = \text{constant}}$$

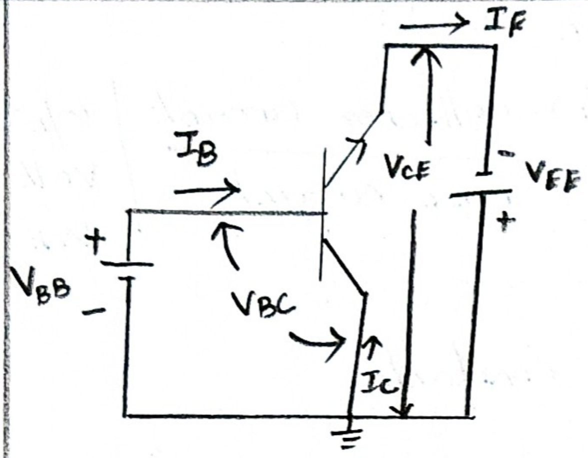
→ It is the slope of V_{BE} Vs V_{CE} curve

→ Typical value of h_{re} is the order of 10^{-5} to 10^{-4}.

2.4.3. CC Configuration:

→ This is also called grounded collector configurati

→ In this configuration, base is the input terminal, emitter is the o/p terminal, collector is the common terminal.



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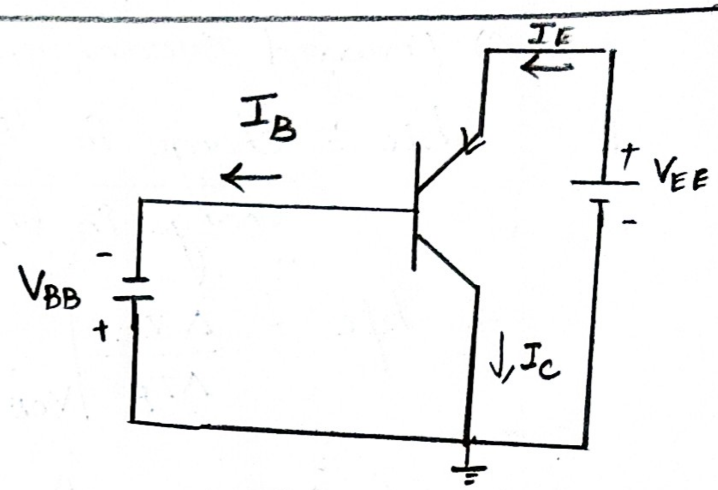

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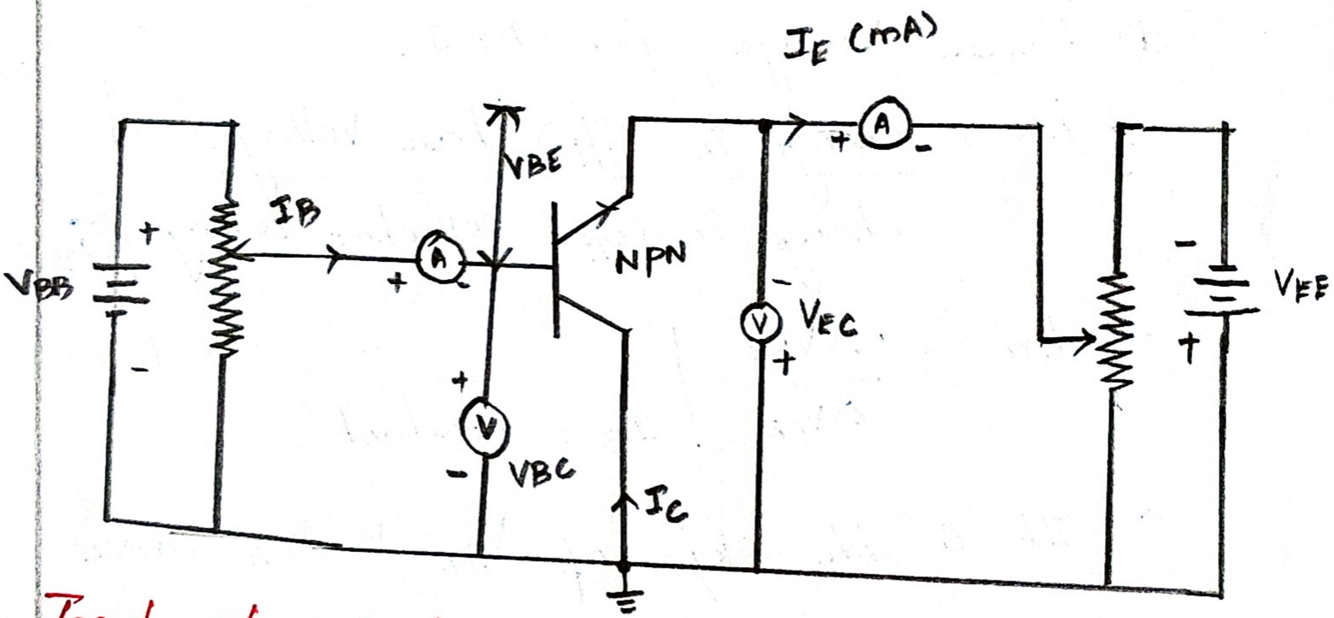
Transistor characteristics :-

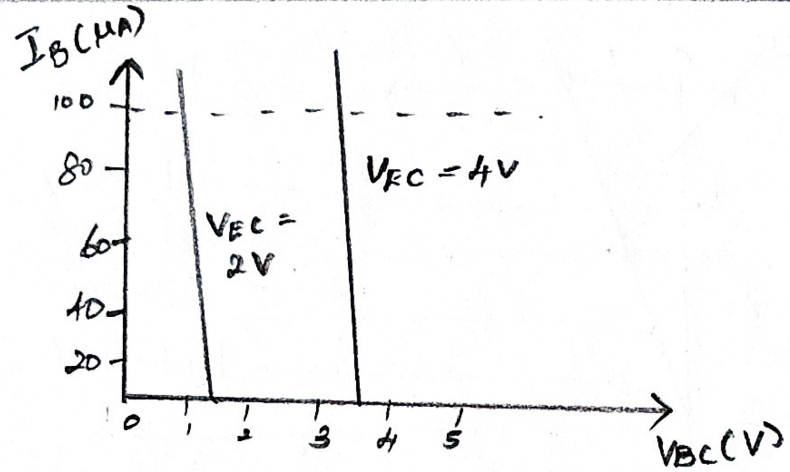


Input characteristics :-

→ To determine the i/p characteristics, V_{EC} is kept constant and V_{BC} is increased in equal steps and the corresponding increase in I_B is noted

→ This procedure is repeated for higher fixed values of V_{EC}

→ The graph is drawn between I_B + V_{BC} at constant V_{EC}.



→ i/p impedance $= h_{ic} = r_i = \left.\dfrac{\Delta V_{BC}}{\Delta I_B}\right| V_{EC} = \text{constant}$.

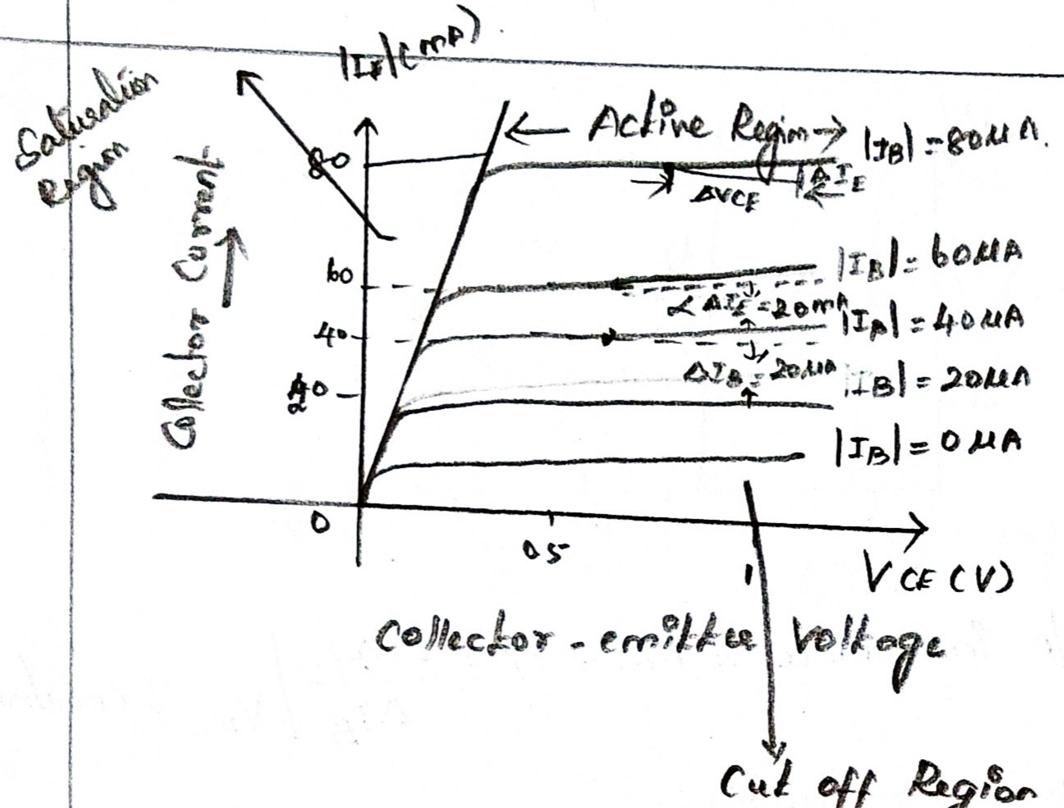
Output characteristics :-

→ To determine the o/p characteristics, I_B is kept constant and V_{CE} is increased in equal steps and the corresponding I_E is noted.

→ This procedure is repeated for different fixed value of I_B

→ Graph is drawn between I_E Vs V_{EC} at constant I_B

→ I_C is approximately equal to I_E, the CC o/p characteristics are practically similar to those of CE o/p characteristics.



→ In this configuration, i/p is applied between base and collector and o/p is taken from emitter and collector.

→ This CC configuration is also known as Emitter follower configurations.

→ The o/p resistance $R_o = \left.\dfrac{\text{change in } V_{EC}}{\text{change in } I_E}\right|_{I_B = \text{Constant}}$

$$R_o = \left.\frac{\Delta V_{EC}}{\Delta I_E}\right|_{I_B = \text{Constant}}.$$

Transistor parameters (or) CC hybrid parameters (or) h- parameters.

→ The slope of the CC characteristics will give 4 transistor parameters.

Transistor parameters (or) CC hybrid parameters (or) h- parameters.

The slope of the CC characteristics will give the following 4 transistor parameters.

a) Input Impedance (h_{ic})

$$h_{ic} = \frac{\text{change in (i/p) base Voltage}}{\text{change in (i/p) base current}} \Bigg| \begin{array}{l}\text{o/p collector voltage} \\ V_{EC} = \text{Constant}\end{array}$$

$$\Rightarrow h_{ic} = \frac{\Delta V_{BC}}{\Delta I_B} \Bigg|_{V_{EC} = \text{Constant}}$$

→ It is the slope of CC i/p characteristics I_B Vs V_{BC}.

b) output Admittance (h_{oc})

$$\Rightarrow h_{oc} = \frac{\text{change in (o/p) emitter current}}{\text{change in (o/p) collector Voltage}} \Bigg| \begin{array}{l}\text{i/p base current} \\ I_B = \text{Constant}\end{array}$$

$$h_{oc} = \frac{\Delta I_E}{\Delta V_{EC}} \Bigg|_{I_B = \text{Constant}}.$$

→ It is the slope of CC o/p characteristics I_E Vs V_{EC}.

c) Forward Current gain (h_{fc}).

$$h_{fc} = \frac{\text{change in (o/p) emitter Current}}{\text{change in (i/p) base current}} \Bigg| \begin{array}{l}\text{o/p Collector voltage} \\ V_{CE} = \text{Constant}\end{array}$$

$$h_{fc} = \frac{\Delta I_E}{\Delta I_B}\Big|_{V_{CE} = \text{Constant}}$$

→ It is the slope of I_C Vs I_B Curve.

d) Reverse Voltage gain (h_{rc})

$$h_{rc} = \frac{\text{change in (i/p) base Voltage}}{\text{change in (o/p) emitter Voltage}}\Big|_{\text{(i/p) base current } I_B = \text{Constant}}$$

$$h_{rc} = \frac{\Delta V_{BC}}{\Delta V_{EC}}\Big|_{I_B = \text{Constant}}$$

→ Slope of V_{BC} Vs V_{CE} Curve.

DC current gain γ_{dc} (or) γ (or) Large Signal current gain of CC configuration.

$$\gamma = \frac{I_E}{I_B} = \frac{\text{emitter current}}{\text{Base current}}$$

AC current gain γ_{ac} (or) current amplification factor γ (or) Small Signal current gain (or) h_{fc} (or) forward gain

$$\gamma_{ac} = \frac{\text{change in o/p current}}{\text{Change in i/p current}}\Big|_{V_{CE} = \text{Constant}}$$

$$= \frac{\Delta I_E}{\Delta I_B}\Big|_{V_{CE} = \text{Constant}}$$

Relationship b/w α, β and γ

$$\gamma = \frac{I_E}{I_B} \quad — (1)$$

W.K.T

$$I_E = I_B + I_C$$

$$\therefore I_B = I_E - I_C \quad — (2)$$

Sub (2) in (1)

$$\gamma = \frac{I_E}{I_E - I_C} \quad — (3)$$

÷ numerator and denominator by I_E

$$\gamma = \frac{I_E/I_E}{I_E/I_E - I_C/I_E} \quad — (4)$$

$$= \frac{1}{1 - I_C/I_E}$$

$$\left[\because \alpha = \frac{I_C}{I_E}\right]$$

$$\boxed{\gamma = \frac{1}{1-\alpha}} \quad — (5)$$

$$\left[\because \alpha = \frac{\beta}{1+\beta}\right]$$

Sub $\alpha = \beta/_{1+\beta}$ in (5)

$$\gamma = \frac{1}{1 - \beta/_{1+\beta}} = \frac{1}{\frac{1+\cancel{\beta}-\cancel{\beta}}{1+\beta}} = \frac{1}{\frac{1}{1+\beta}}$$

$$\boxed{\gamma = 1+\beta}$$

Note:· CE configuration is most widely used in amplifier circuits

1) provides both voltage gain and current gain
2) provides high power gain
3) Can be cascaded efficiently

Comparison of CB, CE and CC configurations:.

S.No	characteristics	CB Config	CE Config	CC config
1.	I/p Resistance (R_i)	Very Low (20Ω)	Low (1kΩ)	High (500kΩ)
2.	O/p Resistance (R_o)	Very high (1MΩ)	High (40kΩ)	Low (50Ω)
3.	I/p current	I_E	I_B	I_B
4.	O/p current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter & base	Base & Emitter	Base & Collector.
6.	Leakage current	Small	Large	Large.
7.	O/p voltage taken between	Collector & base	Collector & emitter	Emitter & Collector.
8.	Current Amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$.

S.No	Characteristics	CB Config	CE Config	CC config.
9.	Current gain (Ai)	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
10.	Voltage gain (Av)	Medium	Medium	Less than unity
11.	Application	As a i/p stage of multistage amplifier and for high frequency application.	provides both voltage and current gain greater than unity and hence it is widely used in audio signal amplification.	For impedance matching.

Reach through (or) punch through

⇒ According to Early effect, the depletion region width of junction Jc increases with increased Collector - Junction voltage. Hence width of the base will be reduced (or) reached to zero.

⇒ It affects both i/p and o/p characteristics of a transistor.

⇒ It is possible to raise the punch through voltage by increasing the doping concentration in the base but this automatically reduces the emitter efficiency.

⇒ punch through takes place at a fixed voltage b/w collector and base and is not dependent on circuit configuration, where as

→ Multiplication takes place at different voltages depending upon the circuit configuration.

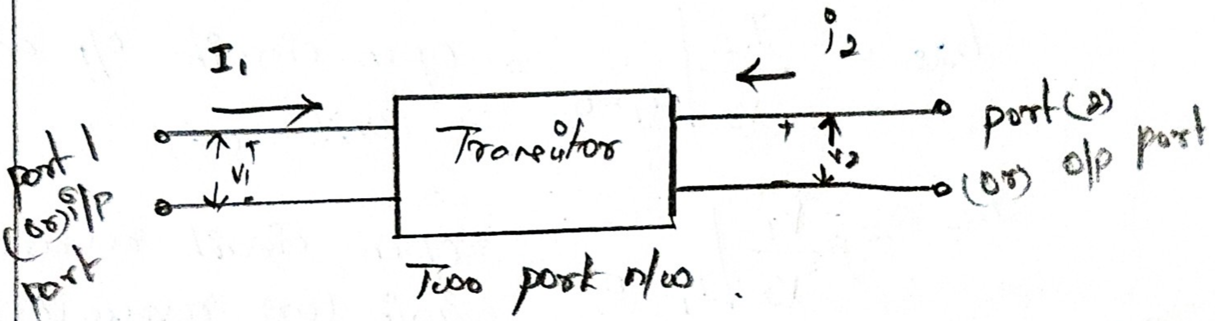
→ The voltage limit of a particular transistor is determined by either of the two types of break down whichever occurs at lower voltage.

→ A transistor can be treated as a two port network

→ The terminal behaviour of any 2-port n/w can be specified by the terminal voltages V_1 & V_2 at ports 1 & 2 respectively

→ Currents I_1, I_2 entering ports 1 & 2 respectively.

→ Out of 4 variables V_1, V_2, I_1, I_2, two can be selected as independent variables (I_1, V_2) and the remaining two (V_1, I_2) can be expressed in terms of these independent variables.



Two port n/w.

→ The h-parameter representation is widely utilised in modelling of transistors.

→ Hence both short circuit and open circuit terminal condition are used

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$\therefore V_1 = h_{11} I_1 + h_{12} V_2$

$I_2 = h_{21} I_1 + h_{22} V_2$

$h_{11}, h_{12}, h_{21}, h_{22}$ are hybrid parameters.

when $V_2 = 0$, (ie) with open o/p port short circuited.

$$\therefore h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = \text{Short circuit i/p impedance.}$$

[Unit Ω]

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = \text{Short circuit Forward current gain (or) Forward transistor ratio.}$$

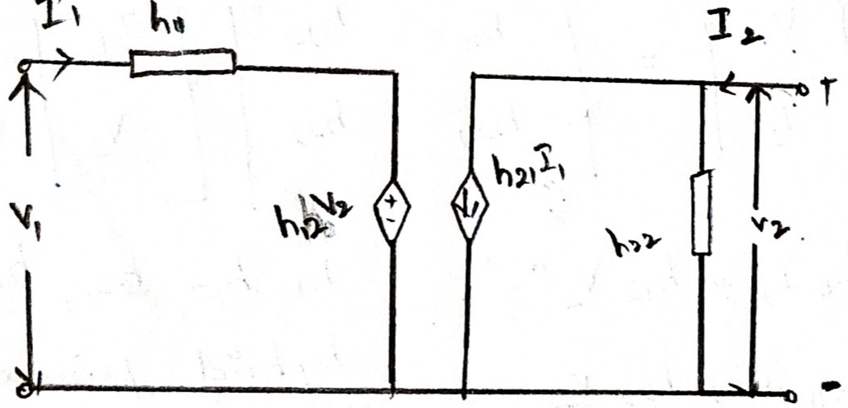
when $I_1 = 0$, ie with i/p port open Circuited.

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = \text{open circuit o/p admittance}$$

(Unit ℧)

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} =$$ open circuit reverse Voltage gain (or) reverse transfer ratio.

→ As the dimension (Ω, ℧, dimensionless) are not a Like ie they are hybrid in nature, these parameters are called hybrid parameters.



Equivalent Circuit of h-parameter model.

→ $h_{12}V_2$ is the Voltage Controlled Source and $h_{21}I_1$ is the Current Controlled Source.

→ The alternative Subscript notations recommended by IEEE commonly used are

$i = 11 = $ i/p

$o = 22 = $ o/p

$f = 21 = $ forward transfer

$r = 12 = $ reverse transfer.

→ Second Subscript to designate the type of configuration 'e' for CE, 'b' for CB and 'c' for CC.

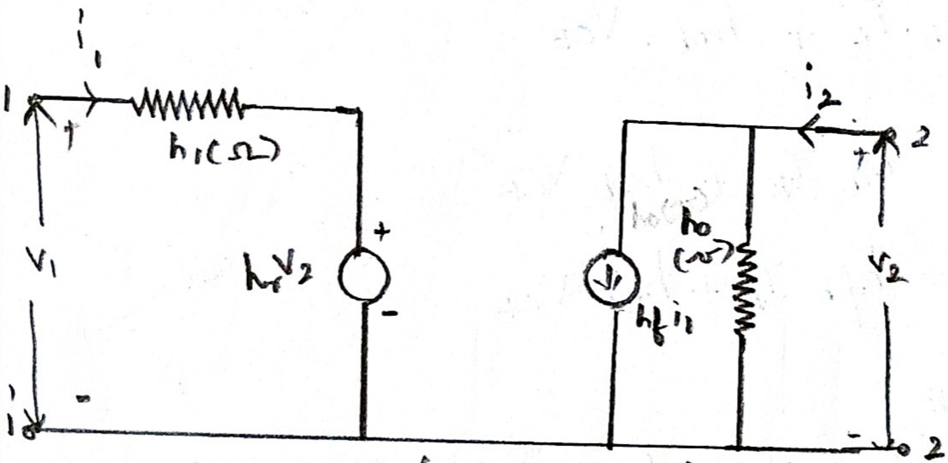
Ex:

$h_{ie} = h_{11e}$ = Short ckt i/p impedance

$h_{oe} = h_{22e}$ = open ckt o/p admittance.

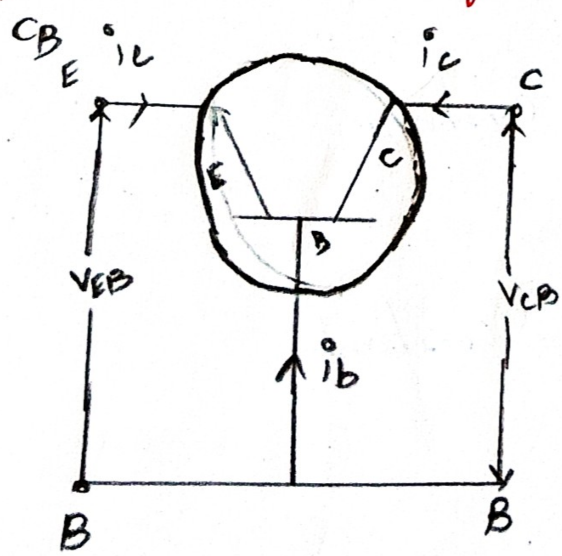
$h_{fe} = h_{21e}$ = Short ckt forward current gain

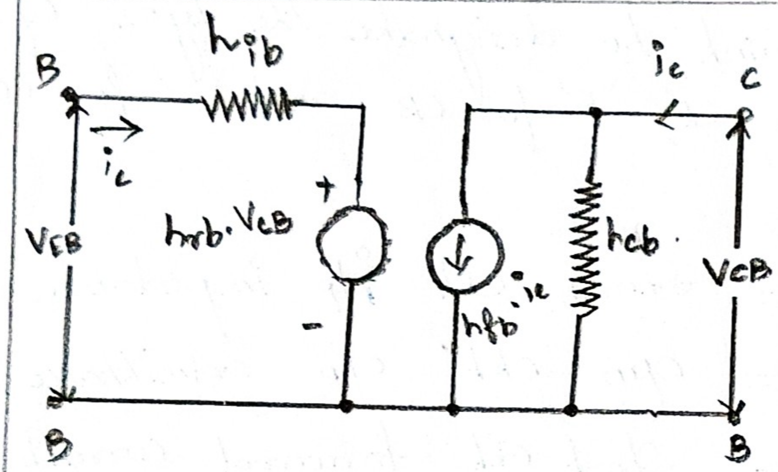
$h_{re} = h_{12e}$ = open ckt reverse Voltage gain.



h-parameter model for two port network

a) h-parameter model for CB Configuration:





$$V_{EB} = h_{ib} \cdot i_e + h_{rb} \cdot V_{CB}$$

$$i_c = h_{fb} \cdot i_e + h_{ob} \cdot V_{CB}$$

$$\Rightarrow \quad V_{BE} = h_{ib} I_E + h_{rb} V_{CB}$$

$$I_C = h_{fb} I_E + h_{ob} V_{CB}$$

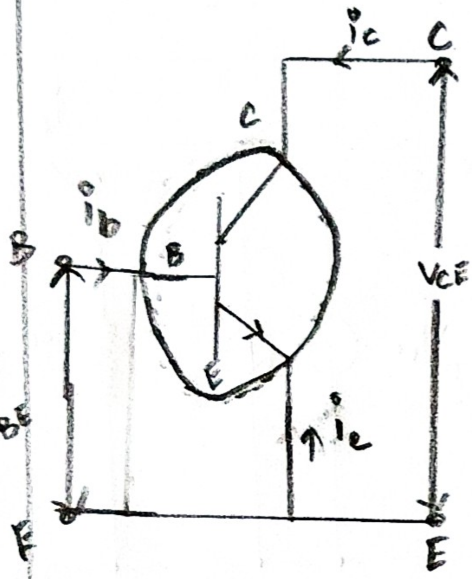
$$h_{ib} = \left. \frac{V_{BE}}{I_E} \right|_{V_{CB} = \text{Constant}}$$

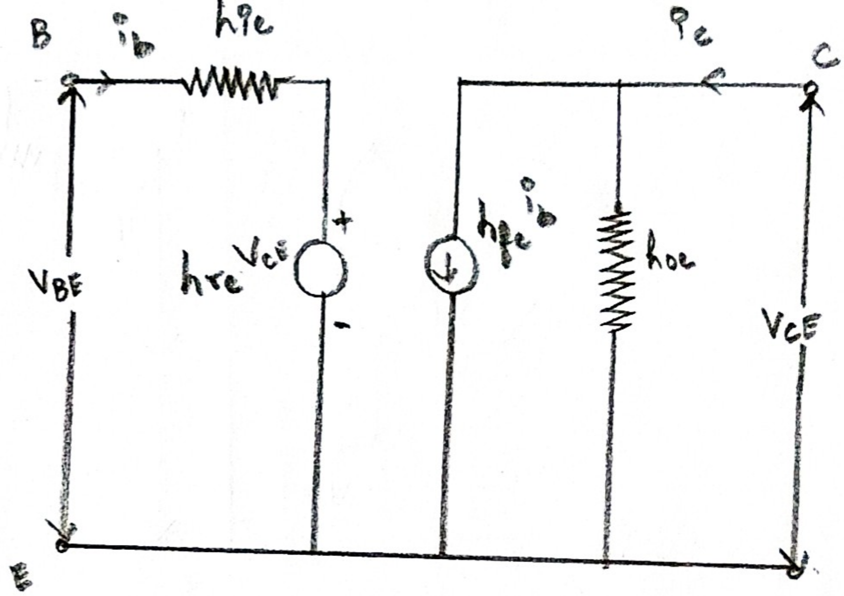
$$h_{rb} = \left. \frac{V_{BE}}{V_{CB}} \right|_{I_E = \text{Constant}}$$

$$h_{fb} = \left. \frac{I_C}{I_E} \right|_{V_{CB} = \text{Constant}}$$

$$h_{ob} = \left. \frac{I_C}{V_{CB}} \right|_{I_E = \text{Constant}}$$

b) h- parameter model for CE configuration:.





$$V_{BE} = h_{ie} I_B + h_{re} V_{CE}$$

$$I_C = h_{fe} I_B + h_{oe} V_{CE}$$

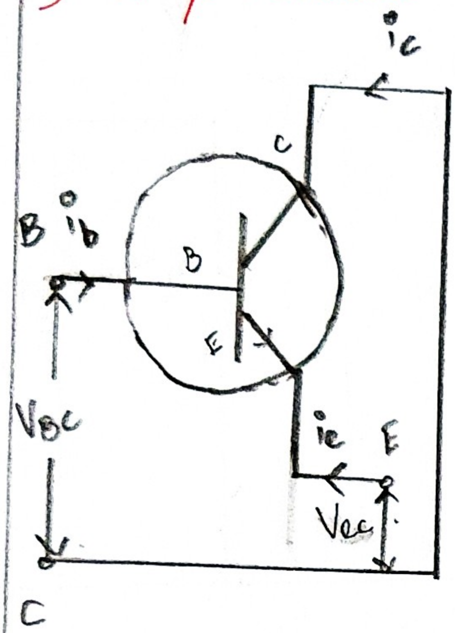
Input Impedance $h_{ie} = \left.\frac{V_{BE}}{I_B}\right|_{V_{CE} = \text{Constant}}$

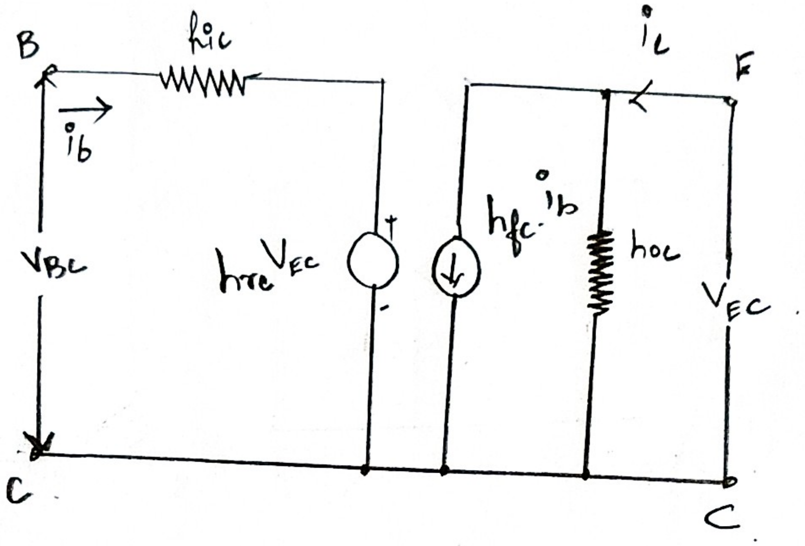
Output Admittance $h_{oe} = \left.\frac{I_C}{V_{CE}}\right|_{I_B = \text{Constant}}$

Reverse Voltage gain $h_{re} = \left.\frac{V_{BE}}{V_{CE}}\right|_{I_B = \text{constant}}$.

Forward current gain $h_{fe} = \left.\frac{I_C}{I_B}\right|_{V_{CE} = \text{Constant}}$.

c) h-parameter model for CC configurations.





$$V_{BC} = h_{ic} I_B + h_{rc} V_{EC}$$

$$I_E = h_{fc} I_B + h_{oc} V_{EC}.$$

Input impedance

$$h_{ic} = \frac{V_{BC}}{I_B}\bigg|_{V_{EC} = \text{constant}}$$

output Admittance

$$h_{oc} = \frac{I_E}{V_{EC}}\bigg|_{I_B = \text{constant}}$$

forward current gain

$$h_{fc} = \frac{I_E}{I_B}\bigg|_{V_{EC} = \text{constant}}$$

Reverse Voltage gain

$$h_{rc} = \frac{V_{BC}}{V_{EC}}\bigg|_{I_B = \text{consta}}$$

Typical h-parameter Value for a transistor.

Parameter	CB	CE	CC
h_i	$22\ \Omega$	$1,100\ \Omega$	$1,100\ \Omega$
h_r	2.5×10^{-4}	2.5×10^{-4}	1
h_f	-0.98	50	-51
h_o	$0.49\ \mu A/V$	$25\ \mu A/V$	$25\ \mu A/V$.

h parameter Conversion table

CE to CB conversion formulae	CE to CC conversion formulae
$h_{ib} = \dfrac{h_{ie}}{1+h_{fe}}$	$h_{ic} = h_{ie}$
$h_{rb} = \dfrac{h_{ie}\,h_{oe}}{1+h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re} \simeq 1$
$h_{fb} = \dfrac{-h_{fe}}{1+h_{fe}}$	$h_{fc} = -(1+h_{fe})$.
$h_{ob} = \dfrac{h_{oe}}{1+h_{fe}}$	$h_{oc} = h_{oe}$.