CSC/ECE 506: Architecture of Parallel Computers

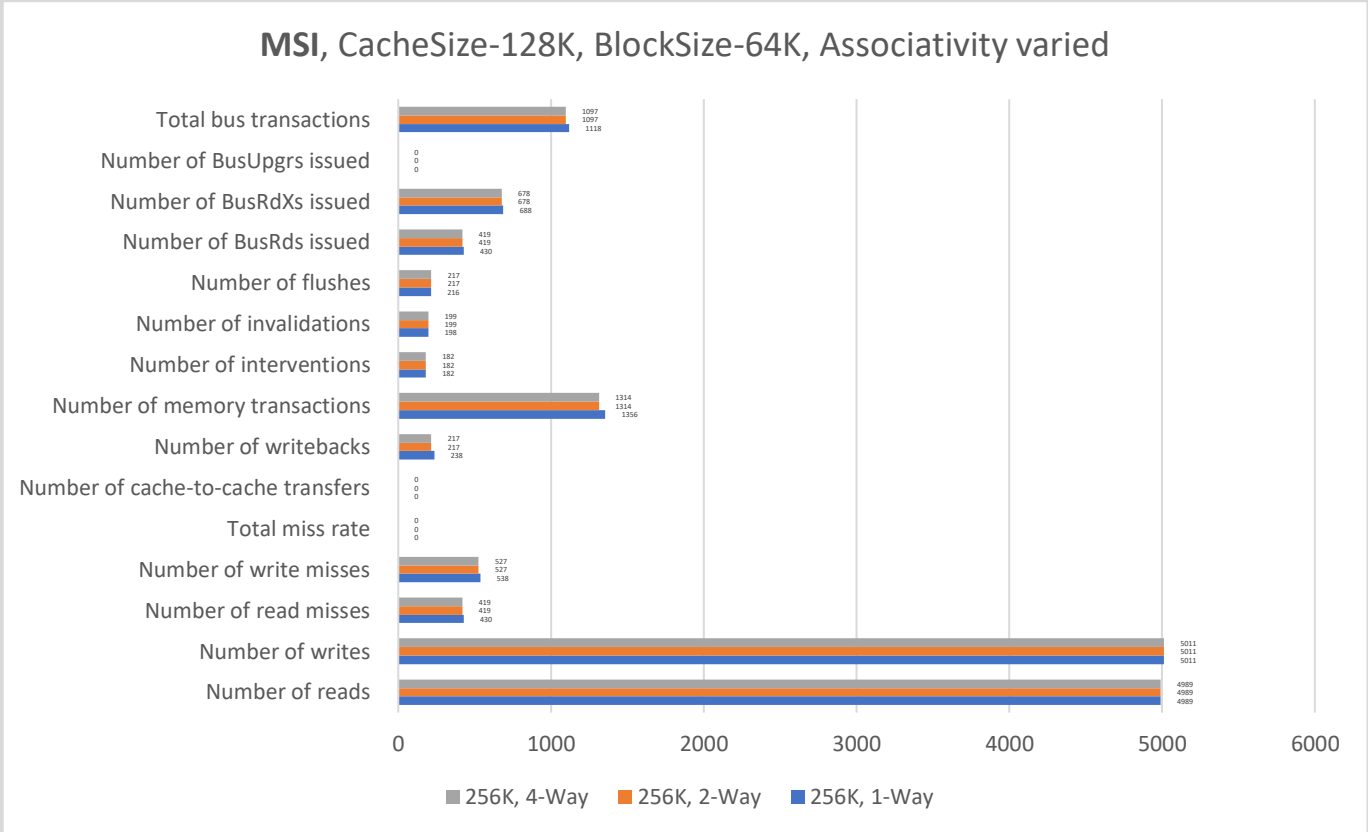
Program 3: Bus-Based Cache Coherence Protocols

Prajakta K Jadhav: pkjadhav, 200375352 **Shivani M Patel: spatel48, 200370667**

1.MSI Protocol: Following table and bar-charts specifies MSI protocol application for cache coherence when cache associativity and cache block size are varied

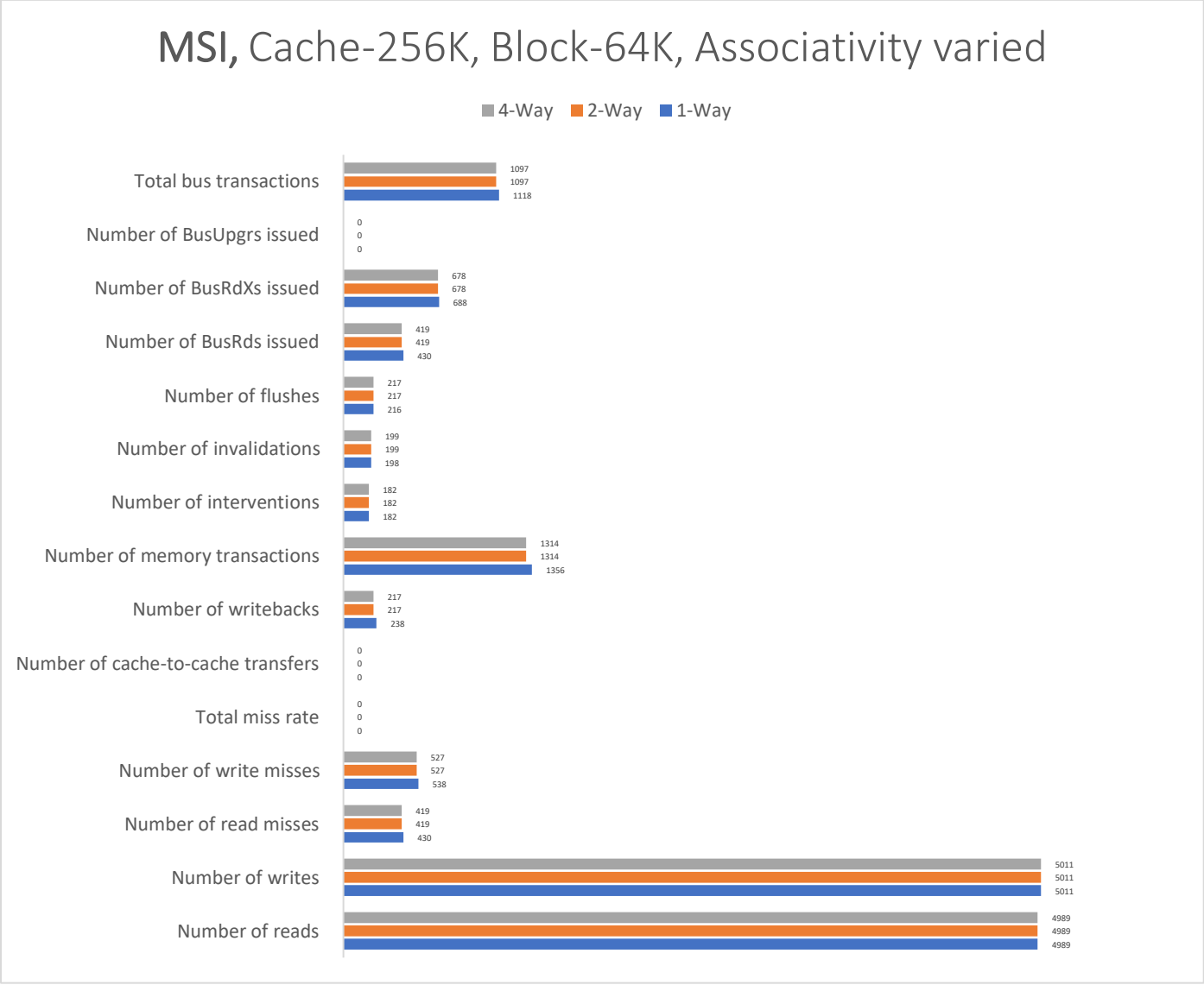
Configuration 1

MSI, Associativity varied				
Cache Size		**128K**		
Cache Block Size		**64K**		
Sr. No.	Parameters	128K, 1-Way	128K, 2-Way	128K, 4-Way
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	430	424	419
4	Number of write misses	538	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	0	0	0
7	Number of writebacks	238	220	217
8	Number of memory transactions	1356	1322	1314
9	Number of interventions	182	182	182
10	Number of invalidations	198	199	199
11	Number of flushes	216	217	217
12	Number of BusRds issued	430	424	419
13	Number of BusRdXs issued	688	678	678
14	Number of BusUpgrs issued	0	0	0
15	Total bus transactions	1118	1102	1097



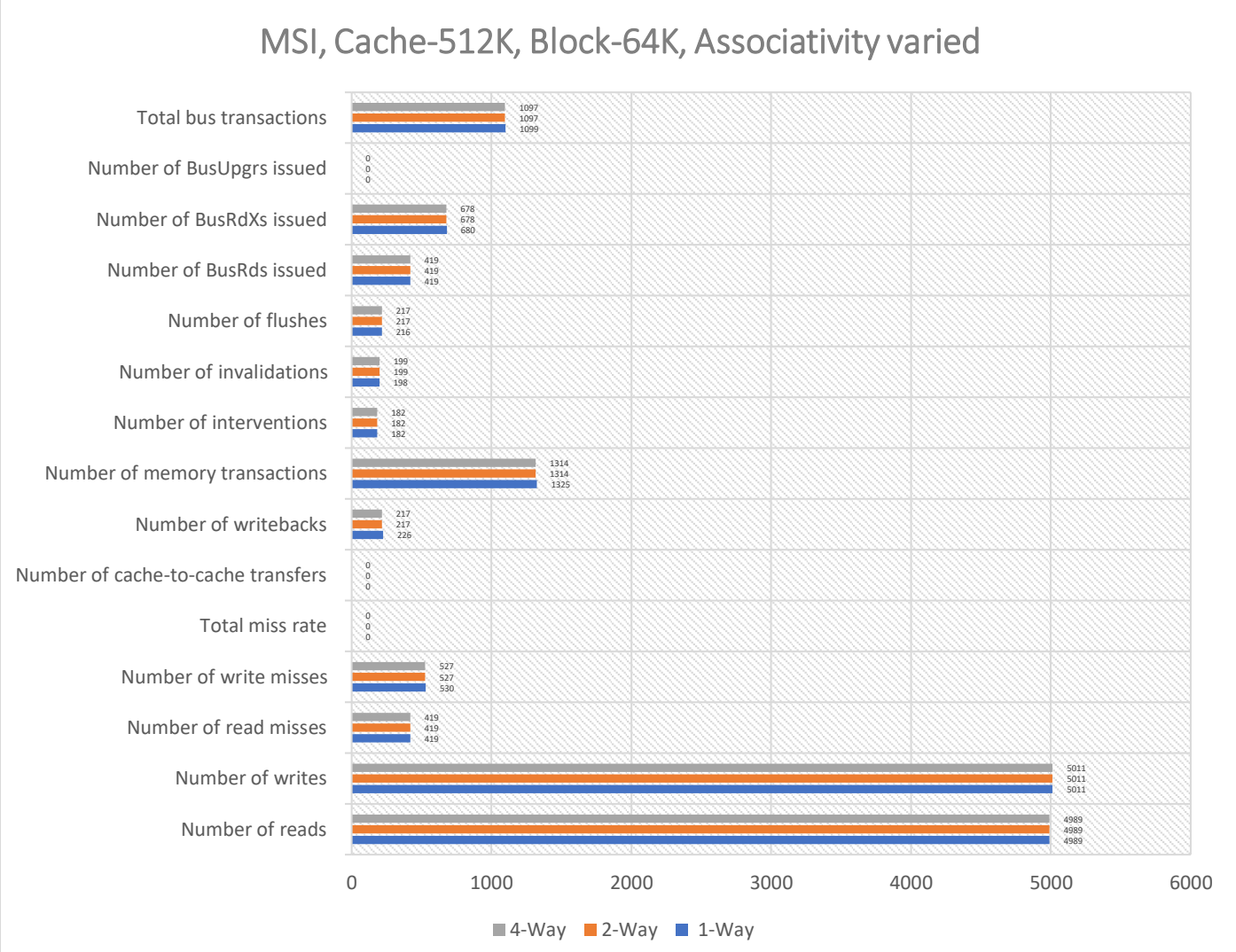
Configuration 2

MSI, Associativity varied				
Cache Size		**256K**		
Cache Block Size		**64K**		
Sr. No.	Parameters	1-Way	2-Way	4-Way
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	430	419	419
4	Number of write misses	538	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	0	0	0
7	Number of writebacks	238	217	217
8	Number of memory transactions	1356	1314	1314
9	Number of interventions	182	182	182
10	Number of invalidations	198	199	199
11	Number of flushes	216	217	217
12	Number of BusRds issued	430	419	419
13	Number of BusRdXs issued	688	678	678
14	Number of BusUpgrs issued	0	0	0
15	Total bus transactions	1118	1097	1097



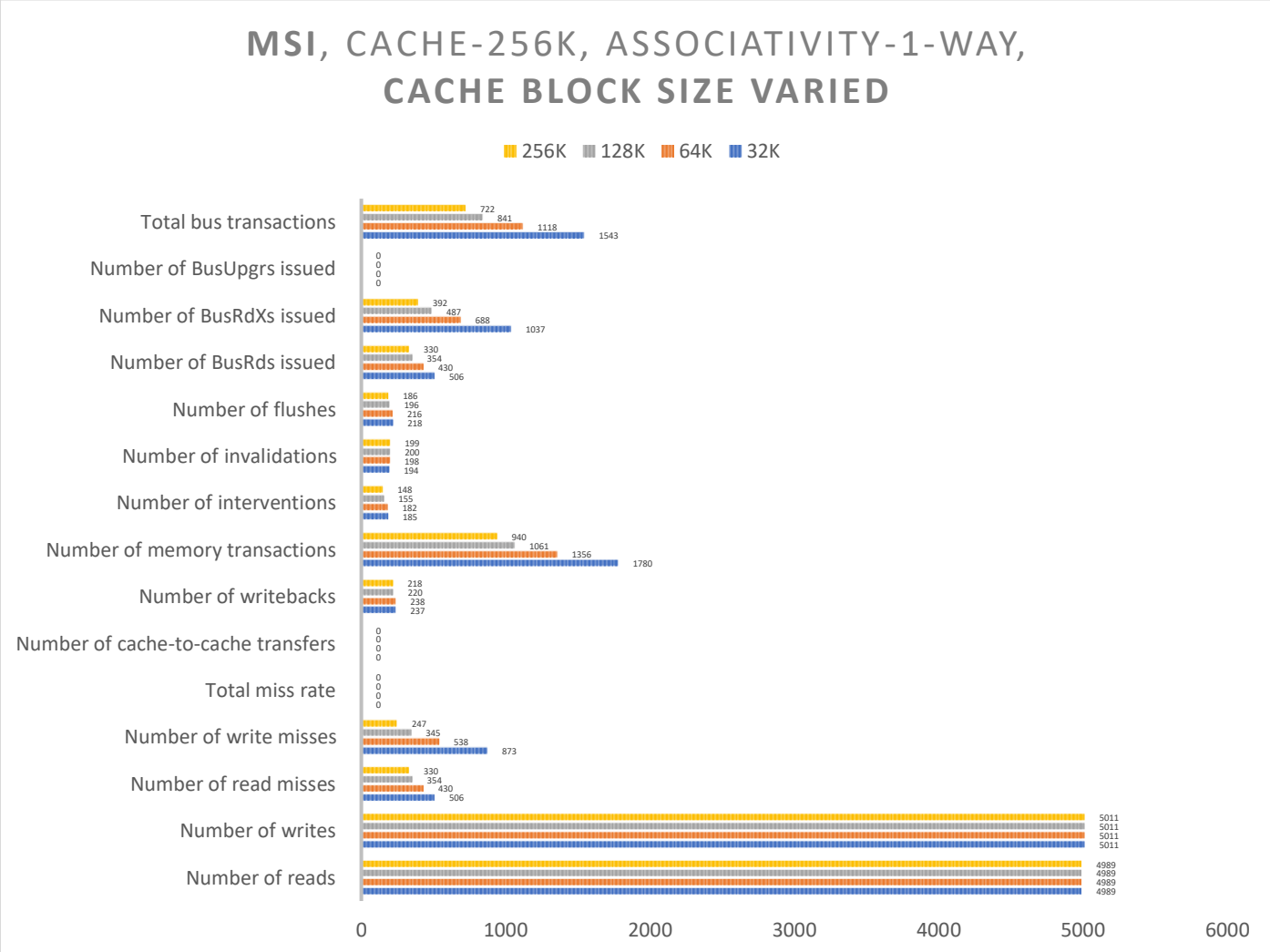
Configuration 3

MSI, Associativity varied				
Cache Size		**512K**		
Cache Block Size		**64K**		
Sr. No.	Parameters	1-Way	2-Way	4-Way
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	419	419	419
4	Number of write misses	530	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	0	0	0
7	Number of writebacks	226	217	217
8	Number of memory transactions	1325	1314	1314
9	Number of interventions	182	182	182
10	Number of invalidations	198	199	199
11	Number of flushes	216	217	217
12	Number of BusRds issued	419	419	419
13	Number of BusRdXs issued	680	678	678
14	Number of BusUpgrs issued	0	0	0
15	Total bus transactions	1099	1097	1097



Configuration 4

MSI, Cache Block Size varied					
Cache Size		**256K**			
Associativity		**1-Way**			
Sr. No.	**Parameters**	**32K**	**64K**	**128K**	**256K**
1	Number of reads	4989	4989	4989	4989
2	Number of writes	5011	5011	5011	5011
3	Number of read misses	506	430	354	330
4	Number of write misses	873	538	345	247
5	Total miss rate	nan	nan	nan	nan
6	Number of cache-to-cache transfers	0	0	0	0
7	Number of writebacks	237	238	220	218
8	Number of memory transactions	1780	1356	1061	940
9	Number of interventions	185	182	155	148
10	Number of invalidations	194	198	200	199
11	Number of flushes	218	216	196	186
12	Number of BusRds issued	506	430	354	330
13	Number of BusRdXs issued	1037	688	487	392
14	Number of BusUpgrs issued	0	0	0	0
15	Total bus transactions	1543	1118	841	722

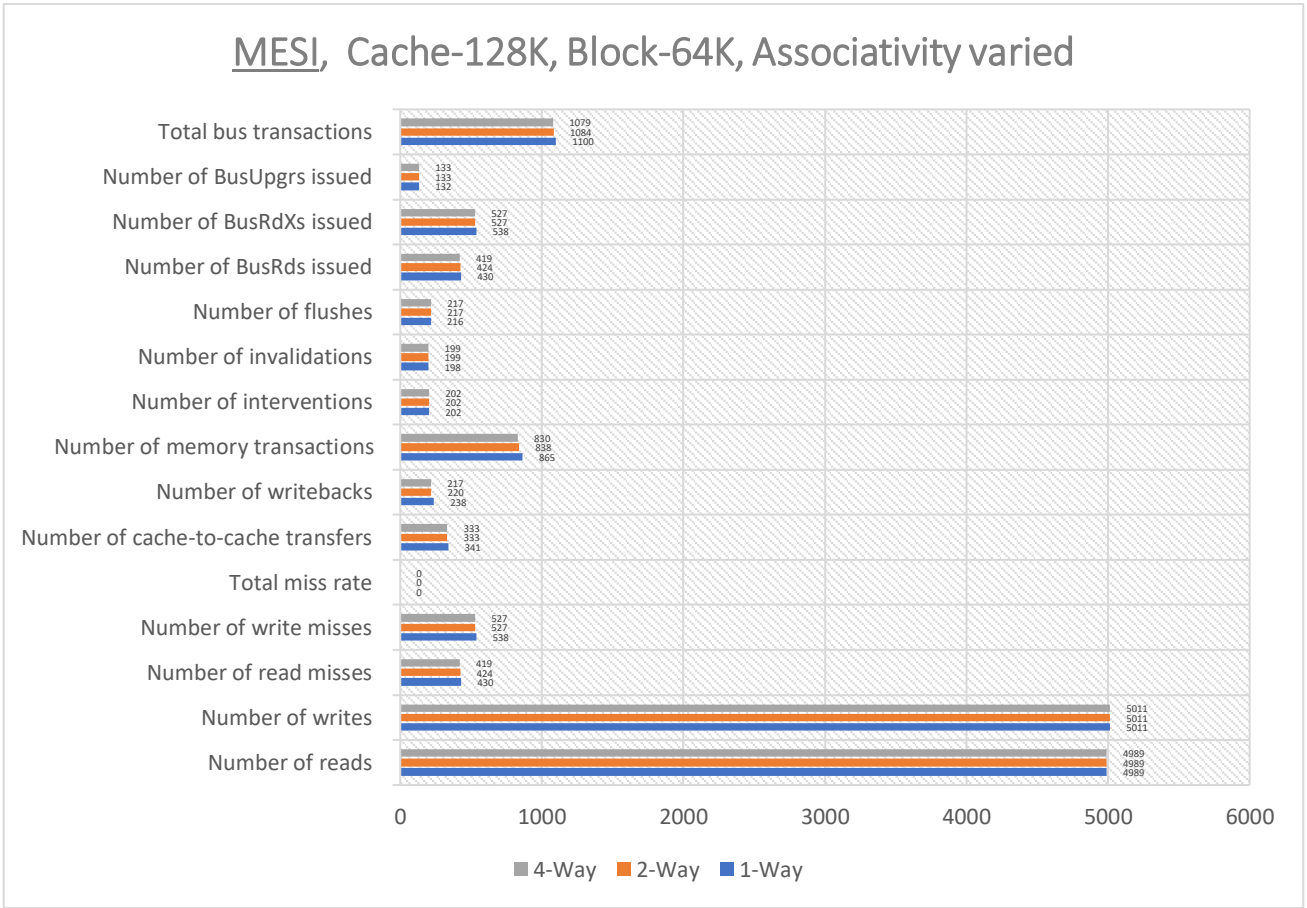


2. MESI Protocol

Following table and bar-charts specifies MESI protocol application for cache coherence when cache associativity and cache block size are varied

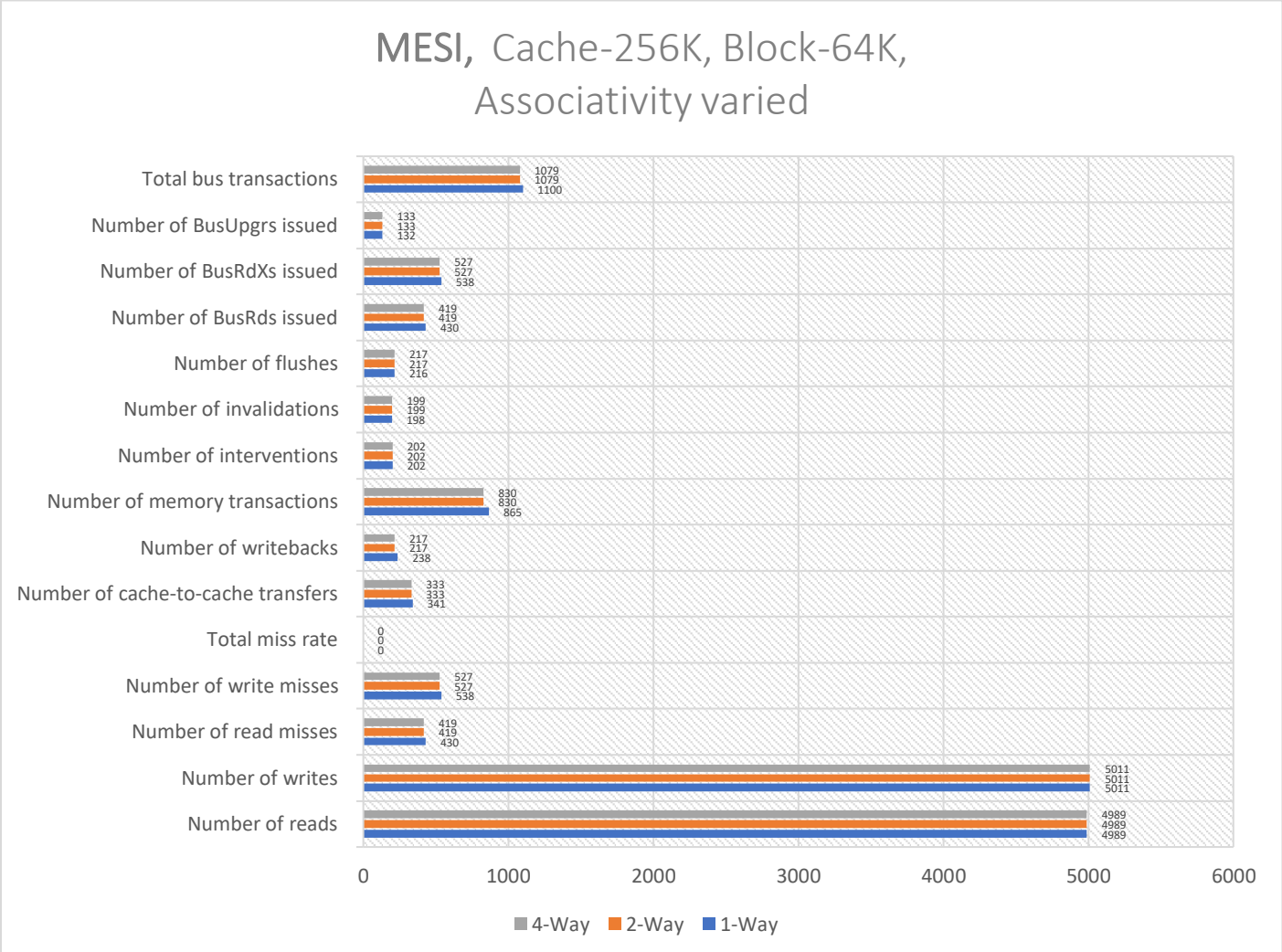
Configuration 1

MESI, Associativity varied				
Cache Size		**128K**		
Cache Block Size		**64K**		
Sr. No.	Parameters	1-Way	2-Way	4-Way
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	430	424	419
4	Number of write misses	538	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	341	333	333
7	Number of writebacks	238	220	217
8	Number of memory transactions	865	838	830
9	Number of interventions	202	202	202
10	Number of invalidations	198	199	199
11	Number of flushes	216	217	217
12	Number of BusRds issued	430	424	419
13	Number of BusRdXs issued	538	527	527
14	Number of BusUpgrs issued	132	133	133
15	Total bus transactions	1100	1084	1079



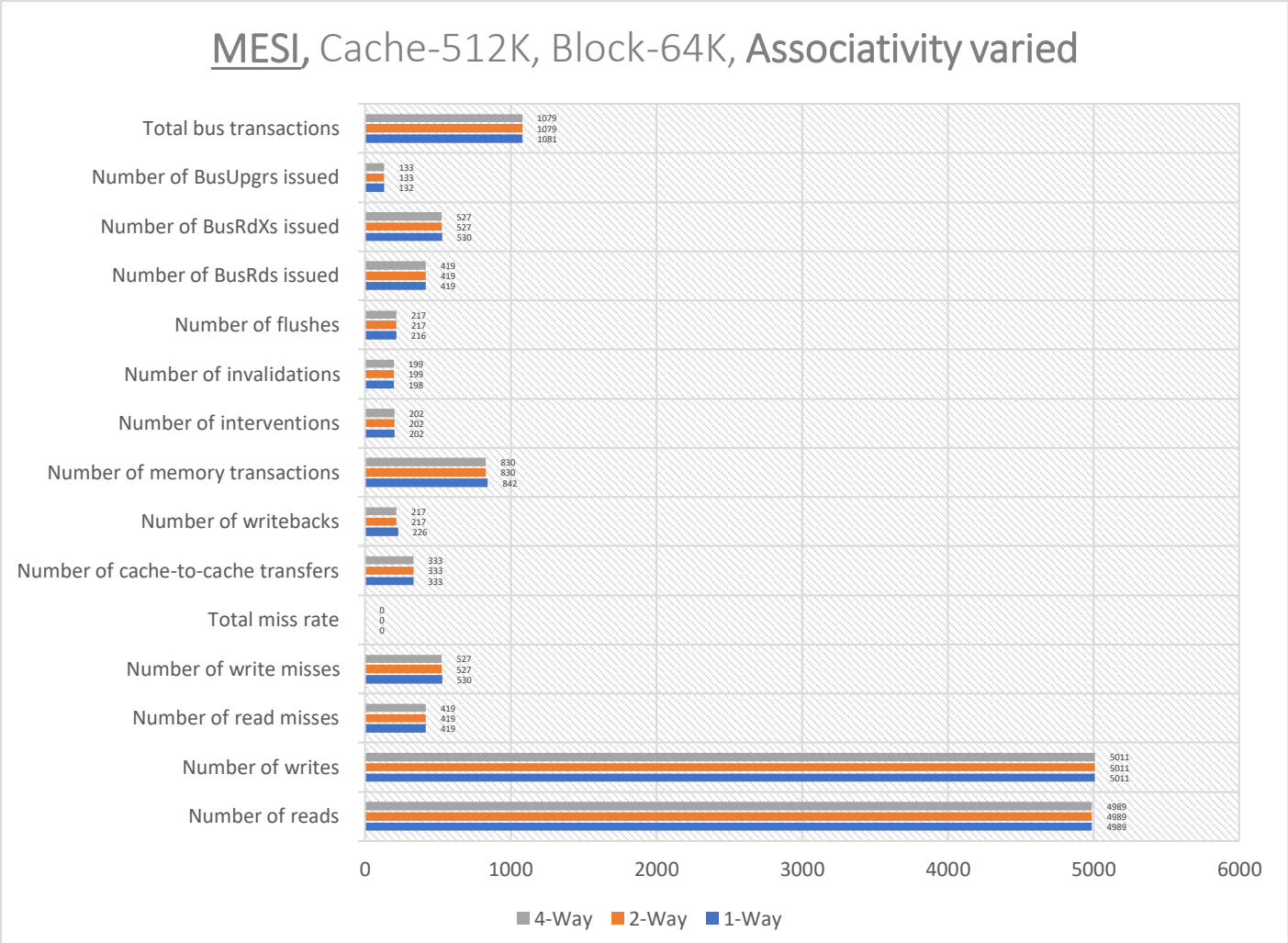
Configuration 2

MESI, Associativity varied				
Cache Size		**256K**		
Cache Block Size		**64K**		
Sr. No.	**Parameters**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	430	419	419
4	Number of write misses	538	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	341	333	333
7	Number of writebacks	238	217	217
8	Number of memory transactions	865	830	830
9	Number of interventions	202	202	202
10	Number of invalidations	198	199	199
11	Number of flushes	216	217	217
12	Number of BusRds issued	430	419	419
13	Number of BusRdXs issued	538	527	527
14	Number of BusUpgrs issued	132	133	133
15	Total bus transactions	1100	1079	1079



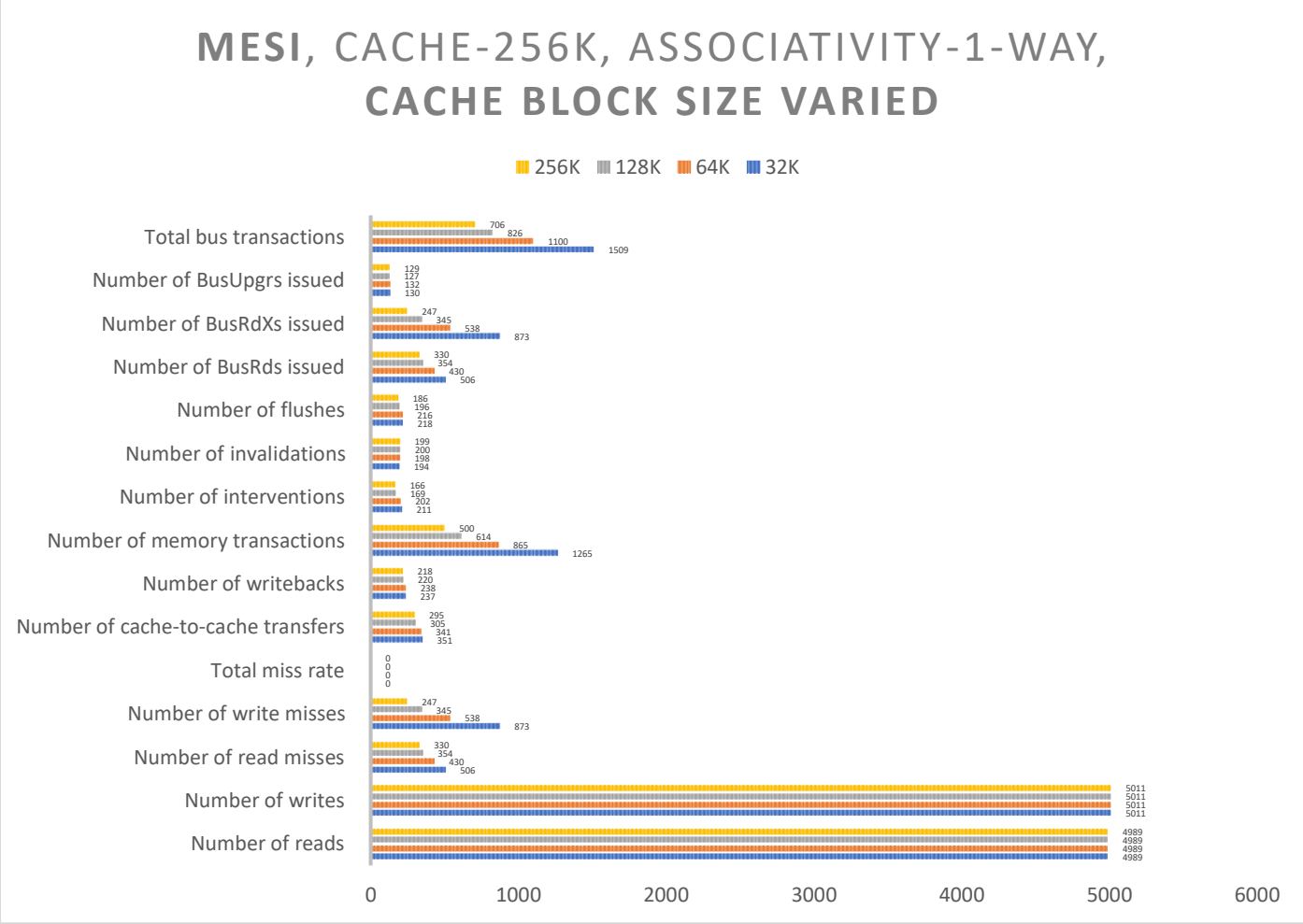
Configuration 3

MESI, Associativity varied				
Cache Size		**512K**		
Cache Block Size		**64K**		
Sr. No.	**Parameters**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	419	419	419
4	Number of write misses	530	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	333	333	333
7	Number of writebacks	226	217	217
8	Number of memory transactions	842	830	830
9	Number of interventions	202	202	202
10	Number of invalidations	198	199	199
11	Number of flushes	216	217	217
12	Number of BusRds issued	419	419	419
13	Number of BusRdXs issued	530	527	527
14	Number of BusUpgrs issued	132	133	133
15	Total bus transactions	1081	1079	1079



Configuration 4

MESI, Cache Block Size varied					
Cache Size		**256K**			
Associativity		**1-Way**			
Sr. No.	**Parameters**	**32K**	**64K**	**128K**	**256K**
1	Number of reads	4989	4989	4989	4989
2	Number of writes	5011	5011	5011	5011
3	Number of read misses	506	430	354	330
4	Number of write misses	873	538	345	247
5	Total miss rate	nan	nan	nan	nan
6	Number of cache-to-cache transfers	351	341	305	295
7	Number of writebacks	237	238	220	218
8	Number of memory transactions	1265	865	614	500
9	Number of interventions	211	202	169	166
10	Number of invalidations	194	198	200	199
11	Number of flushes	218	216	196	186
12	Number of BusRds issued	506	430	354	330
13	Number of BusRdXs issued	873	538	345	247
14	Number of BusUpgrs issued	130	132	127	129
15	Total bus transactions	1509	1100	826	706

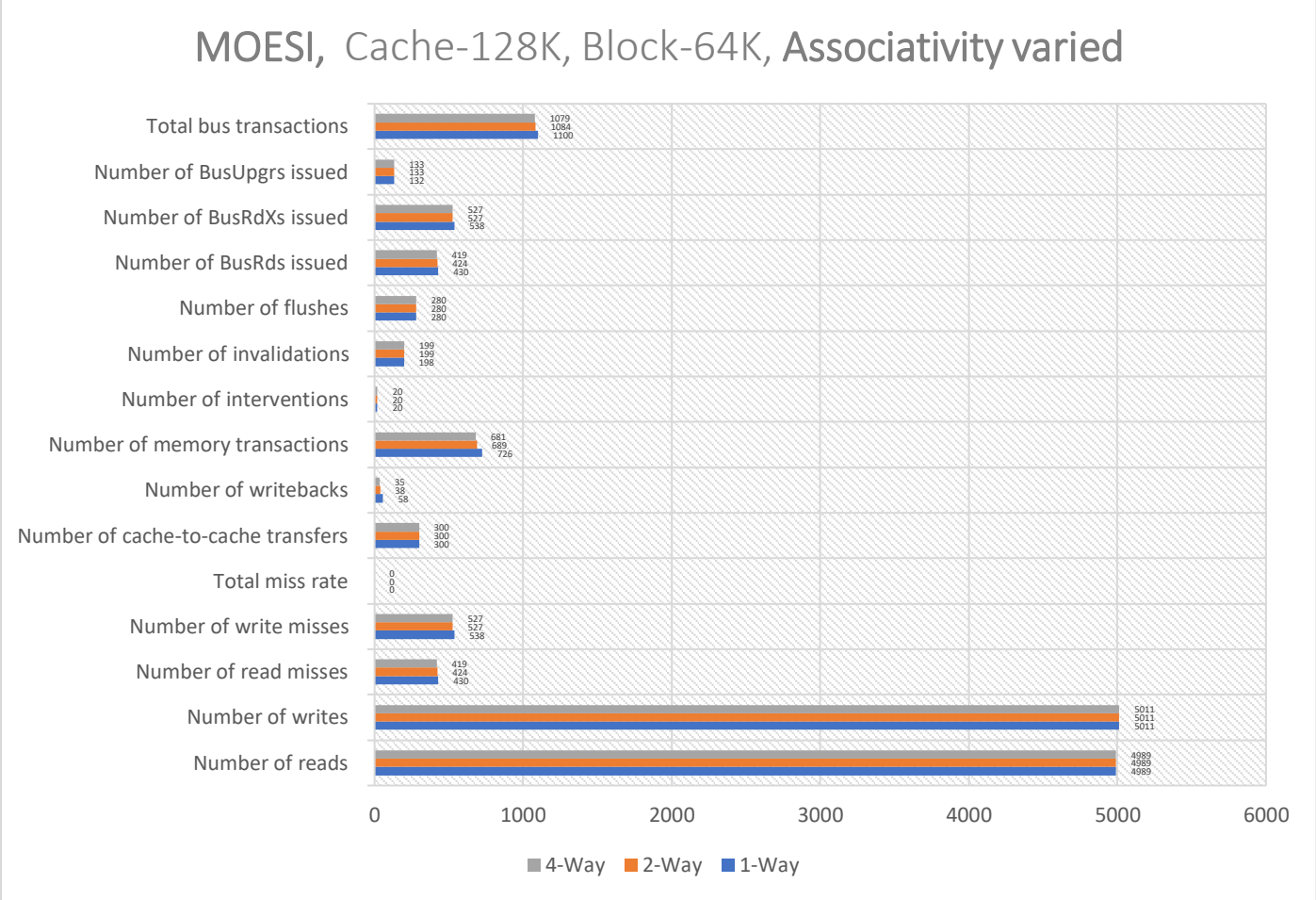


3. MOESI Protocol

Following table and bar-charts specifies MOESI protocol application for cache coherence when cache associativity and cache block size are varied

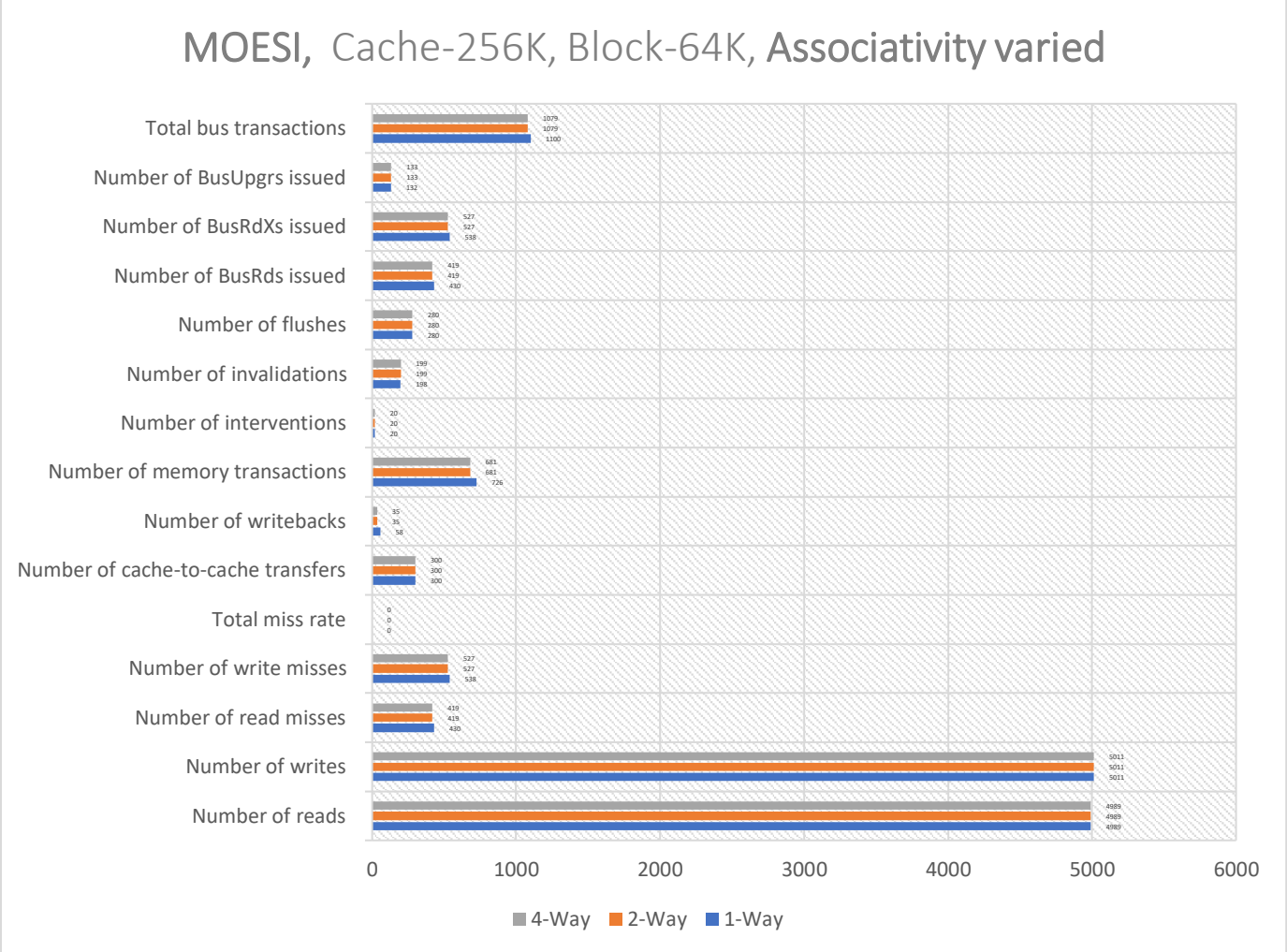
Configuration 1

MOESI, Associativity varied				
Cache Size		**128K**		
Cache Block Size		**64K**		
Sr. No.	**Parameter**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	430	424	419
4	Number of write misses	538	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	300	300	300
7	Number of writebacks	58	38	35
8	Number of memory transactions	726	689	681
9	Number of interventions	20	20	20
10	Number of invalidations	198	199	199
11	Number of flushes	280	280	280
12	Number of BusRds issued	430	424	419
13	Number of BusRdXs issued	538	527	527
14	Number of BusUpgrs issued	132	133	133
15	Total bus transactions	1100	1084	1079



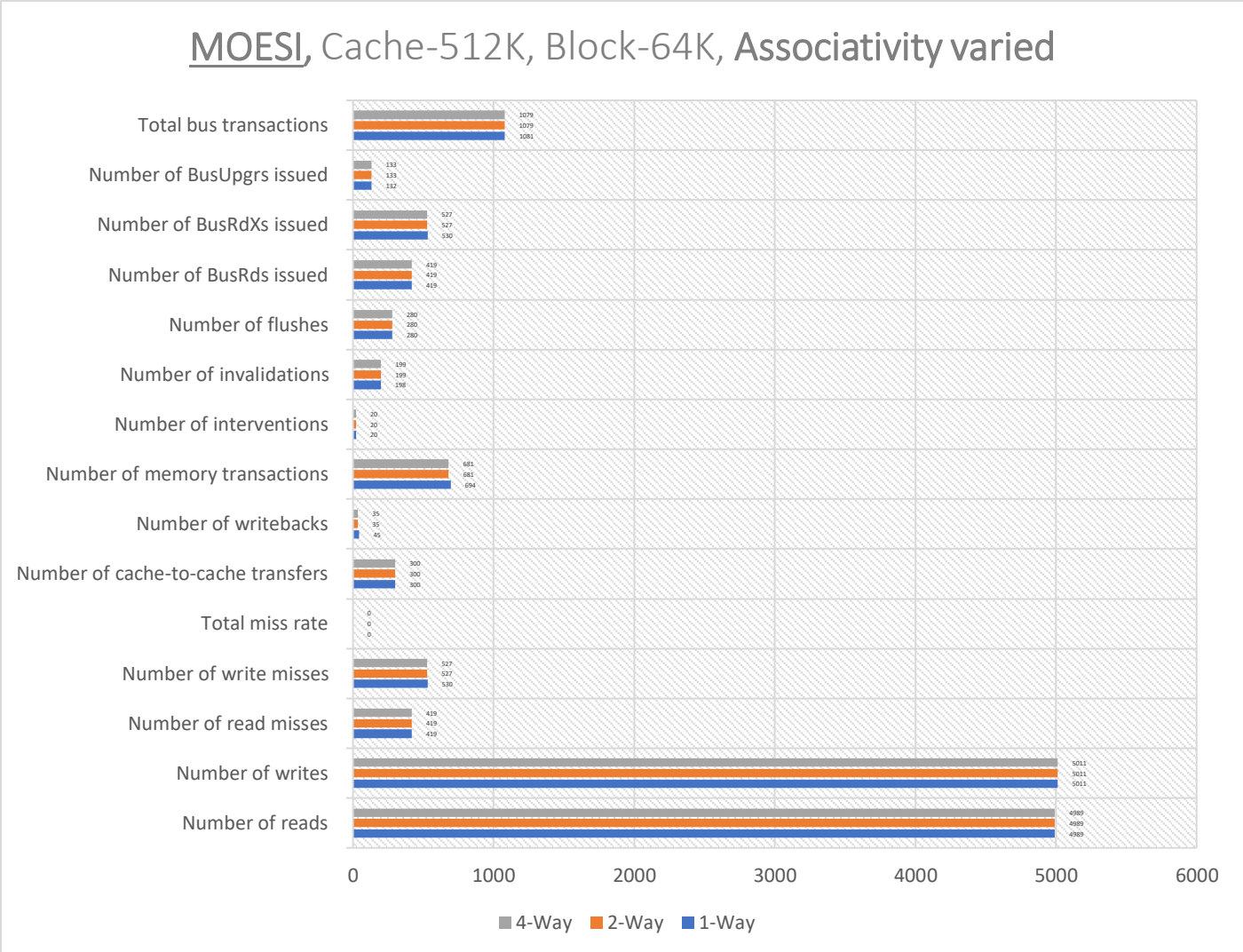
Configuration 2

MOESI, Associativity varied				
Cache Size		**256K**		
Cache Block Size		**64K**		
Sr. No.	**Parameter**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	430	419	419
4	Number of write misses	538	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	300	300	300
7	Number of writebacks	58	35	35
8	Number of memory transactions	726	681	681
9	Number of interventions	20	20	20
10	Number of invalidations	198	199	199
11	Number of flushes	280	280	280
12	Number of BusRds issued	430	419	419
13	Number of BusRdXs issued	538	527	527
14	Number of BusUpgrs issued	132	133	133
15	Total bus transactions	1100	1079	1079



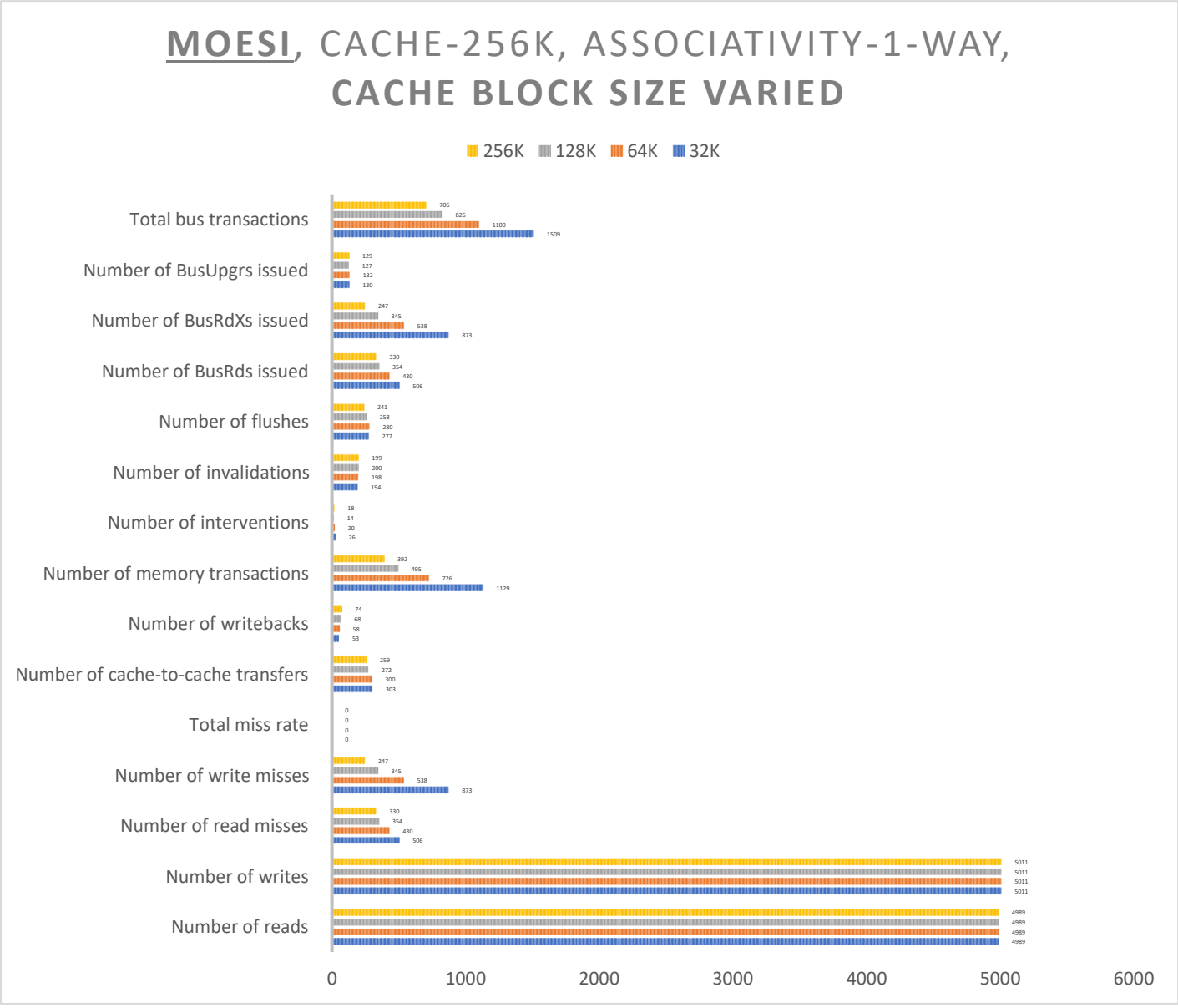
Configuration 3

MOESI, Associativity varied				
Cache Size		**512K**		
Cache Block Size		**64K**		
Sr. No.	**Parameter**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	419	419	419
4	Number of write misses	530	527	527
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	300	300	300
7	Number of writebacks	45	35	35
8	Number of memory transactions	694	681	681
9	Number of interventions	20	20	20
10	Number of invalidations	198	199	199
11	Number of flushes	280	280	280
12	Number of BusRds issued	419	419	419
13	Number of BusRdXs issued	530	527	527
14	Number of BusUpgrs issued	132	133	133
15	Total bus transactions	1081	1079	1079



Configuration 4

MOESI, Cache Block Size varied					
Cache Size		**256K**			
Associativity		**1-Way**			
Sr. No.	**Parameters**	**32K**	**64K**	**128K**	**256K**
1	Number of reads	4989	4989	4989	4989
2	Number of writes	5011	5011	5011	5011
3	Number of read misses	506	430	354	330
4	Number of write misses	873	538	345	247
5	Total miss rate	nan	nan	nan	nan
6	Number of cache-to-cache transfers	303	300	272	259
7	Number of writebacks	53	58	68	74
8	Number of memory transactions	1129	726	495	392
9	Number of interventions	26	20	14	18
10	Number of invalidations	194	198	200	199
11	Number of flushes	277	280	258	241
12	Number of BusRds issued	506	430	354	330
13	Number of BusRdXs issued	873	538	345	247
14	Number of BusUpgrs issued	130	132	127	129
15	Total bus transactions	1509	1100	826	706

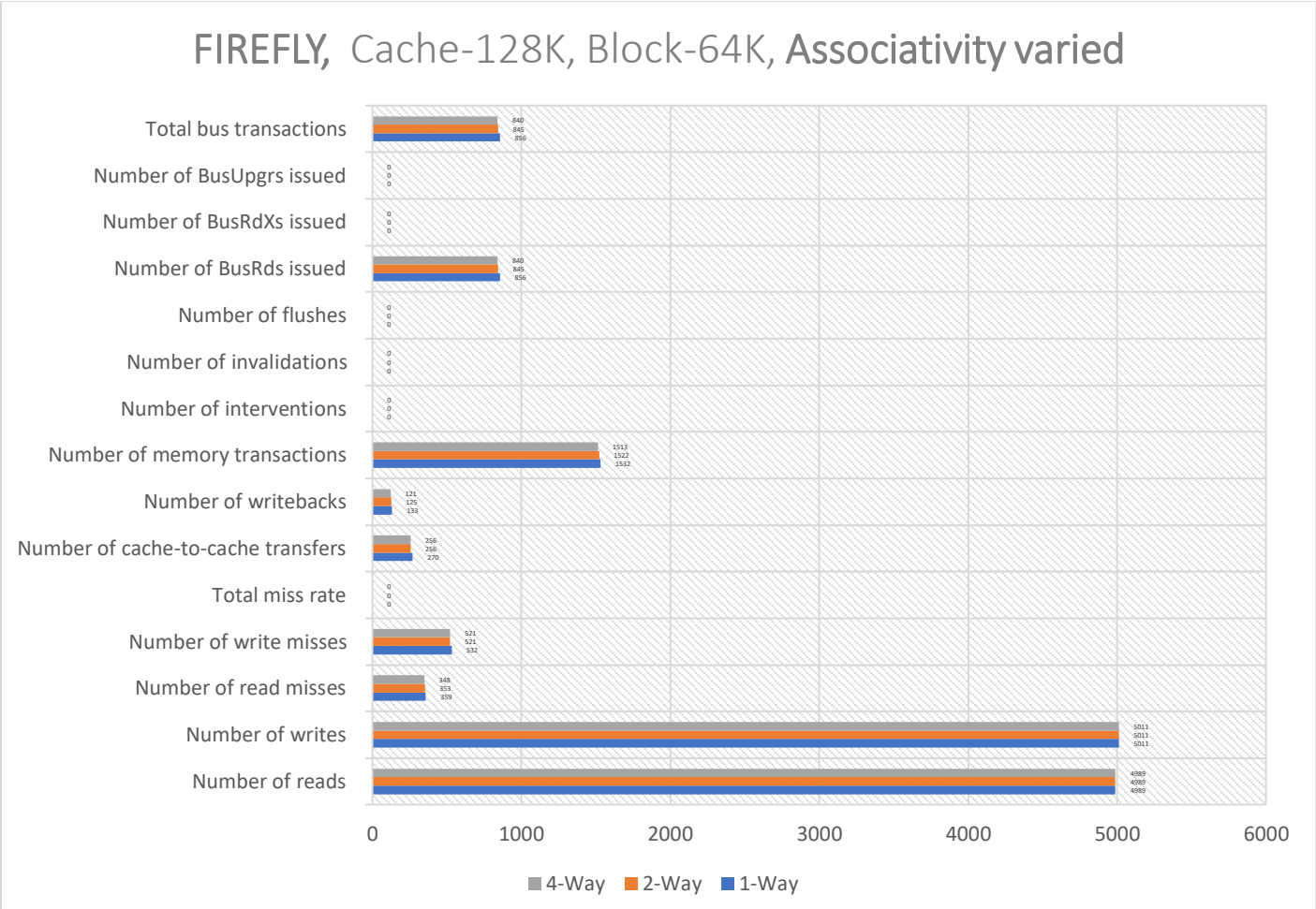


4. FIREFLY Protocol

Following table and bar-charts specifies FIREFLY protocol application for cache coherence when cache associativity and cache block size are varied

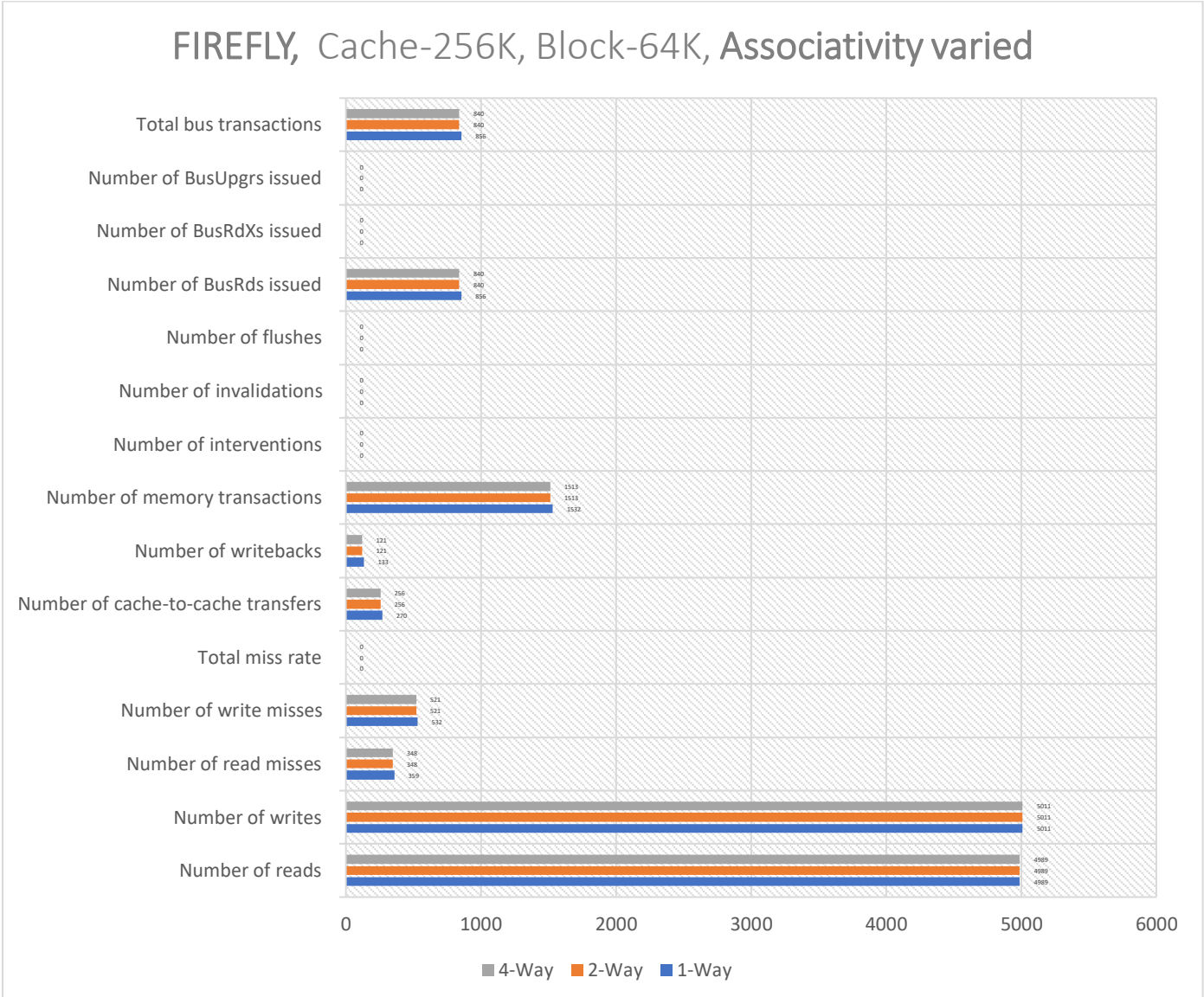
Configuration 1

FIREFLY, Associativity varied				
Cache Size		**128K**		
Cache Block Size		**64K**		
Sr. No.	**Parameters**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	359	353	348
4	Number of write misses	532	521	521
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	270	256	256
7	Number of writebacks	133	125	121
8	Number of memory transactions	1532	1522	1513
9	Number of interventions	0	0	0
10	Number of invalidations	0	0	0
11	Number of flushes	0	0	0
12	Number of BusRds issued	856	845	840
13	Number of BusRdXs issued	0	0	0
14	Number of BusUpgrs issued	0	0	0
15	Total bus transactions	856	845	840



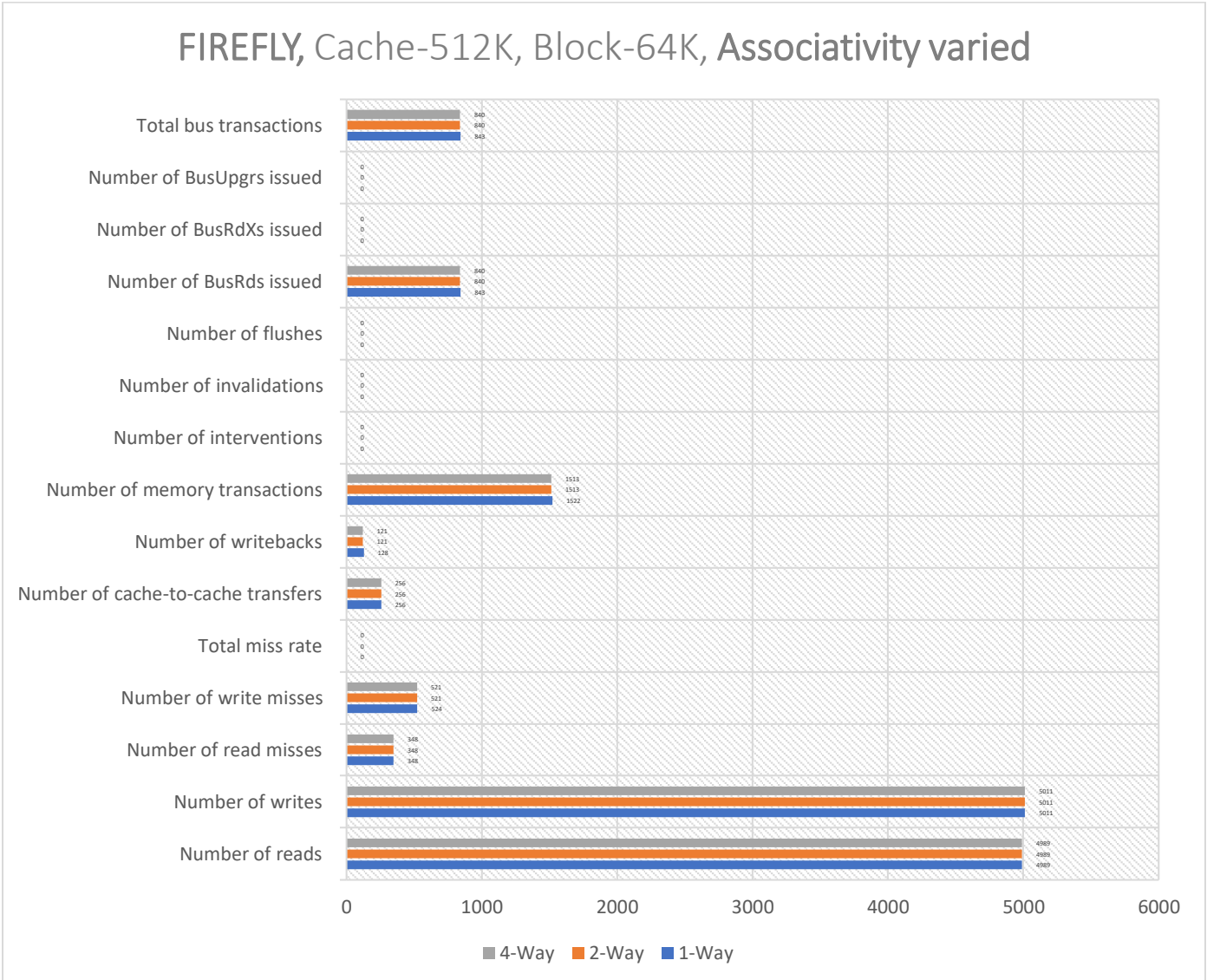
Configuration 2

FIREFLY, Associativity varied				
Cache Size		**256K**		
Cache Block Size		**64K**		
Sr. No.	**Parameters**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	359	348	348
4	Number of write misses	532	521	521
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	270	256	256
7	Number of writebacks	133	121	121
8	Number of memory transactions	1532	1513	1513
9	Number of interventions	0	0	0
10	Number of invalidations	0	0	0
11	Number of flushes	0	0	0
12	Number of BusRds issued	856	840	840
13	Number of BusRdXs issued	0	0	0
14	Number of BusUpgrs issued	0	0	0
15	Total bus transactions	856	840	840



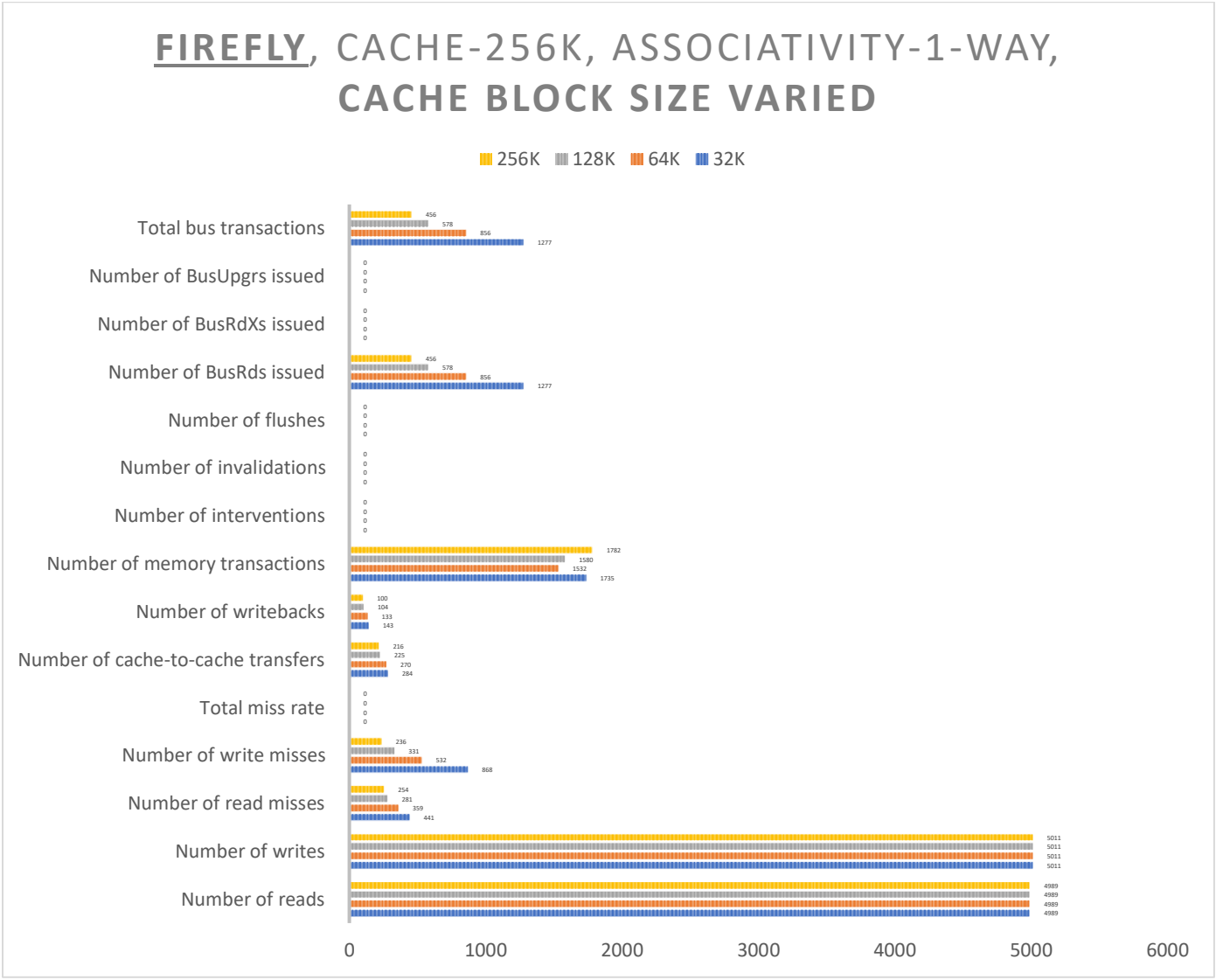
Configuration 3

FIREFLY, Associativity varied				
Cache Size		**512K**		
Cache Block Size		**64K**		
Sr. No.	**Parameters**	**1-Way**	**2-Way**	**4-Way**
1	Number of reads	4989	4989	4989
2	Number of writes	5011	5011	5011
3	Number of read misses	348	348	348
4	Number of write misses	524	521	521
5	Total miss rate	nan	nan	nan
6	Number of cache-to-cache transfers	256	256	256
7	Number of writebacks	128	121	121
8	Number of memory transactions	1522	1513	1513
9	Number of interventions	0	0	0
10	Number of invalidations	0	0	0
11	Number of flushes	0	0	0
12	Number of BusRds issued	843	840	840
13	Number of BusRdXs issued	0	0	0
14	Number of BusUpgrs issued	0	0	0
15	Total bus transactions	843	840	840



Configuration 4

FIREFLY, Cache Block Size varied					
Cache Size		**256K**			
Associativity		**1-Way**			
Sr. No.	**Parameters**	**32K**	**64K**	**128K**	**256K**
1	Number of reads	4989	4989	4989	4989
2	Number of writes	5011	5011	5011	5011
3	Number of read misses	441	359	281	254
4	Number of write misses	868	532	331	236
5	Total miss rate	nan	nan	nan	nan
6	Number of cache-to-cache transfers	284	270	225	216
7	Number of writebacks	143	133	104	100
8	Number of memory transactions	1735	1532	1580	1782
9	Number of interventions	0	0	0	0
10	Number of invalidations	0	0	0	0
11	Number of flushes	0	0	0	0
12	Number of BusRds issued	1277	856	578	456
13	Number of BusRdXs issued	0	0	0	0
14	Number of BusUpgrs issued	0	0	0	0
15	Total bus transactions	1277	856	578	456



========== Questions & Answers ==========

Question 1:

Which helps more on miss rate? Doubling the associativity? Doubling the block size? Doubling the cache size? Does it depend on which protocol is in use?

In multiprocessor, multi-cache environment, when tried to optimize cache coherency w.r.t. cache miss rate, it is observed that miss rate is reduced when cache-associativity is doubled. Independent of the protocol, improving associativity impacts more than change in the block size or cache size.

Question 2:

Does larger associativity benefit a large cache or a small cache?

Cache miss rate improves when cache size is changed from 128KB to 256KB but no significant change in miss rate when cache size changed from 256KB to 512KB .So, smaller cache size benefit from larger associativity than larger cache sizes.

Question 3:

Which protocol (MSI, MESI, MOESI, Firefly) has the most memory transactions? Which one has the least? Why?

Among all given four, with Firefly protocol, resulted memory transactions are maximum while **MOESI** results in the least memory transaction count for same sequence of code. Firefly follows clean sharing in which value in memory is updated whenever cache block is in shared state and a write happens. In MOESI, Memory Write Backs happen only when the blocks in Owner or Modified state get evicted.

Question 4:

Compare the number of read and write misses in MESI vs. MOESI. Explain your observation.

With application of MSI and MOESI Protocol, resulted total number of read misses and write misses are same in both protocol application. Read or write misses occur when a cache block is in Invalid state or not present in the cache. Because both the MSI & MOESI handle the cache read/write misses in the exact same way as both are based on invalidation principle. While, protocols based on Write Update principle, the total write miss count will be less as result of the change in data of a cache block is propagated across all caches.

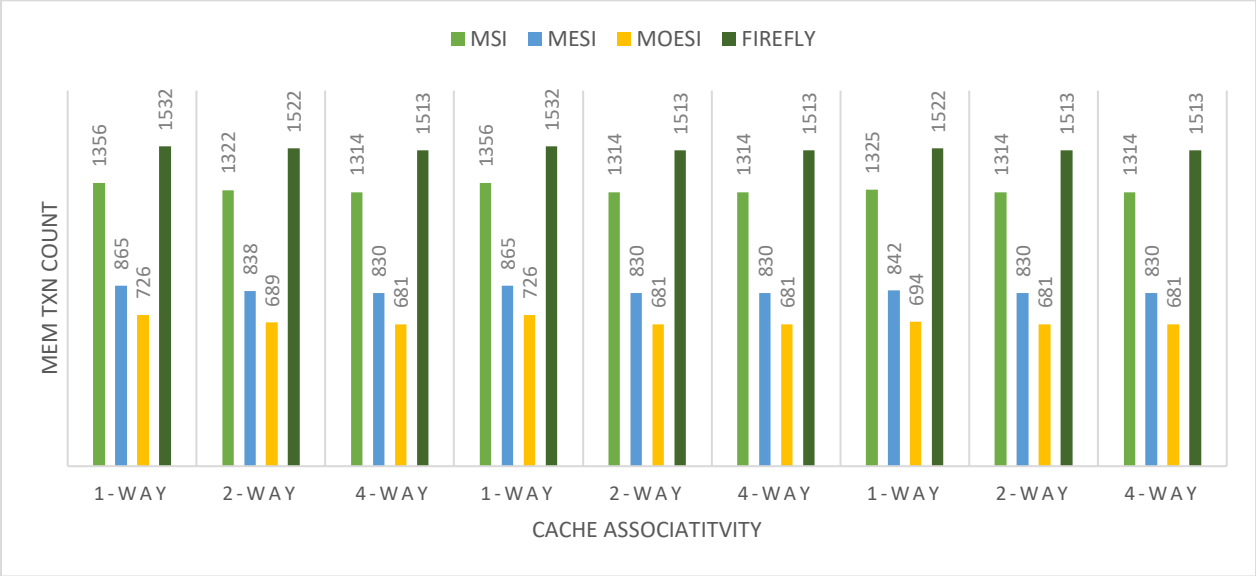
Question 5:

Compare the number of bus transactions and writebacks in MESI vs. MOESI. Explain your observation.

1. Memory Transaction Count Comparison

Parameter	**Total number of memory transactions w.r.t. associativity variation**								
Cache Block Size	64K								
Cache Size	**128K**			**256K**			**512k**		
Protocol/Associativity	1-Way	2-Way	4-Way	1-Way	2-Way	4-Way	1-Way	2-Way	4-Way
MSI	1356	1322	1314	1356	1314	1314	1325	1314	1314
MESI	865	838	830	865	830	830	842	830	830
MOESI	726	689	681	726	681	681	694	681	681
FIREFLY	1532	1522	1513	1532	1513	1513	1522	1513	1513

As can be observed in above table, MOESI has least number of memory transactions as compare to MESI and as well with other two. This is because, MOESI protocol ensure write back to memory happens only when owner of block is changed and not each time when data in that block is modified.



Also, MOESI results in lesser number of the memory txns when cache block size is increased

Parameter	**Total number of memory transactions w.r.t. Cache Block Size variation**				
Cache Size	256K				
Associativity	1-Way				
Protocol/BlockSize	32K	64K	128K	256K	Comment
MSI	**1780**	1356	1061	940	MSI has maximum when block size is least
MESI	1265	865	614	500	
MOESI	1129	726	495	**392**	MOESI has **least** when block size is max
FIREFLY	1735	1532	1580	1782	

2. Write-Back to memory count comparison

Parameter	**Total number of write backs w.r.t. associativity variation**								
Cache Block Size	64K								
Cache Size	**128K**			**256K**			**512k**		
Protocol/Associativity	1-Way	2-Way	4-Way	1-Way	2-Way	4-Way	1-Way	2-Way	4-Way
MSI	238	220	217	238	217	217	226	217	217
MESI	238	220	217	238	217	217	226	217	217
MOESI	58	38	35	58	35	35	45	35	35
FIREFLY	133	125	121	133	121	121	128	121	121

As can be observed in above table, MOESI has least number of memory write backs as compare to MESI and as well with other two. This is because, MOESI protocol ensure write back to memory happens only when owner of block is changed and not each time when data in that block is modified. Also, write backs reduces in count when cache-associativity is improved.

Question 6:

Discuss factors that appear to influence the number of cache-to-cache transfers in the MESI and MOESI protocol. Compare cache-to-cache transfers between these to protocols and explain the observation

For MOESI protocol application, cache-to-cache transfer happens only in M/O/E states but in case of MESI, it happens in shared state as well. Hence, Cache-to-cache transfers is higher in **MESI**.

(Kindly note, to create above mentioned all tables, we imported output result data of each protocol, into excel-sheet, but the data values got converted into int, and hence Total Miss Rate value is 'NaN' in each table, though we have the observed actual values (mostly all of them were between 0 to 1). But as there wasn't sufficient time to re-do all charts.)