SKITTER CIRCUIT

Skitter refers to small, rapid timing variations that can occur in digital signals, especially clock signals, within a chip or a system.

These variations are usually random and can be caused by factors like:

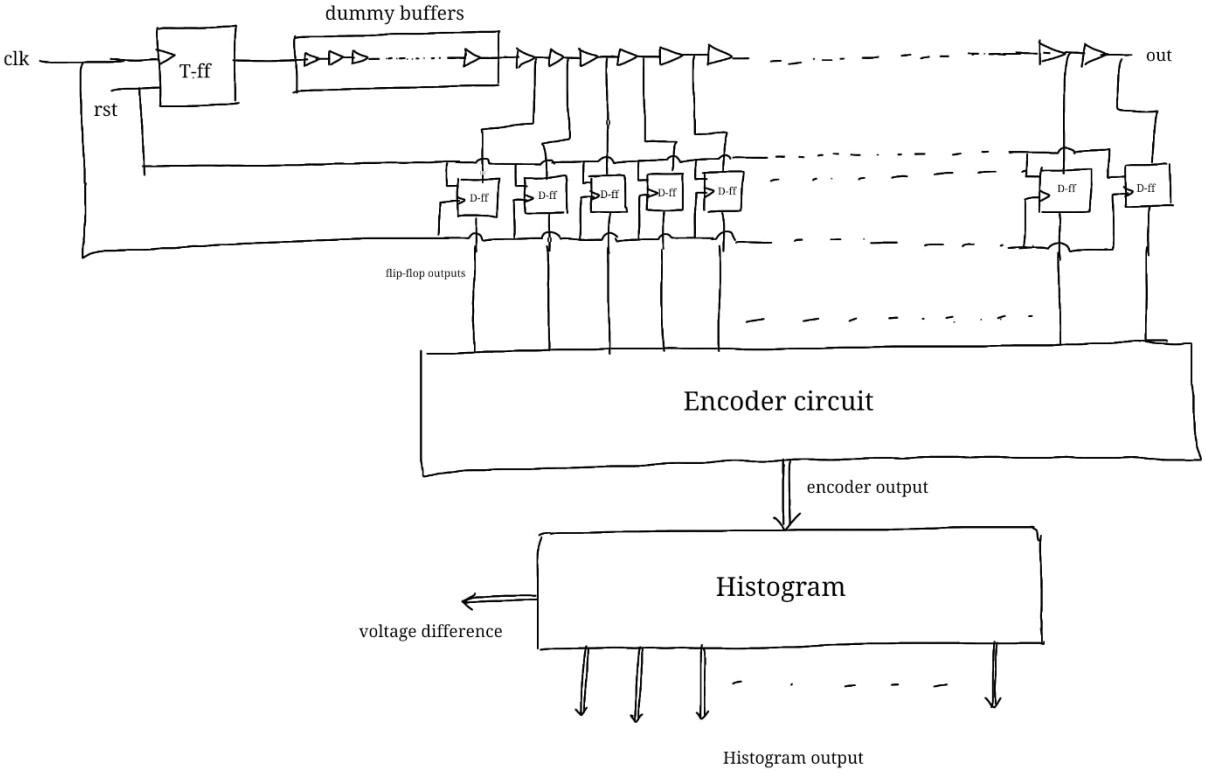
- Process variations (differences in manufacturing)
- Voltage fluctuations
- Temperature changes
- Noise

A Skitter module is used to detect or analyze timing jitter or variations in digital circuits.

It can help in monitoring voltage fluctuation by tracking how signal delay changes, Because timing delay in digital circuits depends on voltage, the circuit delay changes with voltage, it can :

- Detect when voltage drops or spikes
- Estimate the actual voltage (indirectly) based on timing delay

Block diagram:



Calculating the delay values of single buffer stage for different Voltages: (In NGSPICE)

0.8v:

Buffer stage	Rise delay	Fall delay	Average delay	Expected delay	delay per stage	Error
1	8.17E-11	9.30E-11	8.74E-11	8.74E-11	8.74E-11	1.00
5	4.41E-10	4.91E-10	4.66E-10	4.37E-10	9.31E-11	1.07
10	8.88E-10	9.87E-10	9.37E-10	8.74E-10	9.37E-11	1.07
15	1.33E-09	1.48E-09	1.41E-09	1.31E-09	9.39E-11	1.07
20	1.78E-09	1.98E-09	1.88E-09	1.75E-09	9.40E-11	1.08
22	**1.96E-09**	**2.18E-09**	**2.07E-09**	**1.92E-09**	**9.40E-11**	**1.08**
23	2.05E-09	2.28E-09	2.16E-09	2.01E-09	9.40E-11	1.08
25	2.23E-09	2.48E-09	2.35E-09	2.18E-09	9.41E-11	1.08
30	2.67E-09	2.97E-09	2.82E-09	2.62E-09	9.41E-11	1.08

0.9v:

Buffer stages	Rise delay	Fall delay	Average delay	Expected delay	delay per stage	Error
1	7.05E-11	7.69E-11	7.37E-11	7.37E-11	7.37E-11	1.00
5	3.73E-10	3.89E-10	3.81E-10	3.69E-10	7.62E-11	1.03
10	7.50E-10	7.80E-10	7.65E-10	7.37E-10	7.65E-11	1.04
15	1.13E-09	1.17E-09	1.15E-09	1.11E-09	7.65E-11	1.04
20	1.50E-09	1.56E-09	1.53E-09	1.47E-09	7.66E-11	1.04
25	1.88E-09	1.95E-09	1.92E-09	1.84E-09	7.66E-11	1.04
27	**2.03E-09**	**2.11E-09**	**2.07E-09**	**1.99E-09**	**7.66E-11**	**1.04**
28	2.11E-09	2.18E-09	2.15E-09	2.06E-09	7.66E-11	1.04
30	2.26E-09	2.34E-09	2.30E-09	2.21E-09	7.66E-11	1.04

1v :

Buffer stages	Rise delay	Fall delay	Average delay	Expected delay	delay per stage	Error
1	6.47E-11	6.64E-11	6.56E-11	6.56E-11	6.56E-11	1.00
5	3.29E-10	3.28E-10	3.29E-10	3.28E-10	6.57E-11	1.00
10	6.60E-10	6.56E-10	6.58E-10	6.56E-10	6.58E-11	1.00
15	9.91E-10	9.83E-10	9.87E-10	9.83E-10	6.58E-11	1.00
20	1.32E-09	1.31E-09	1.31E-09	1.31E-09	6.57E-11	1.00
25	1.65E-09	1.64E-09	1.64E-09	1.64E-09	6.57E-11	1.00
30	**1.98E-09**	**1.96E-09**	**1.97E-09**	**1.97E-09**	**6.57E-11**	**1.00**
35	2.31E-09	2.29E-09	2.30E-09	2.29E-09	6.57E-11	1.00
40	2.64E-09	2.62E-09	2.63E-09	2.62E-09	6.57E-11	1.00

1.1v:

Buffer stages	Rise delay	Fall delay	Average delay	Expected delay	delay per stage	Error
1	6.16E-11	5.84E-11	6.00E-11	6.00E-11	6.00E-11	1.00
5	3.00E-10	2.92E-10	2.96E-10	3.00E-10	5.92E-11	0.99
10	5.97E-10	5.84E-10	5.90E-10	6.00E-10	5.90E-11	0.98
15	8.95E-10	8.76E-10	8.85E-10	9.00E-10	5.90E-11	0.98
20	1.19E-09	1.17E-09	1.18E-09	1.20E-09	5.90E-11	0.98
25	1.49E-09	1.46E-09	1.47E-09	1.50E-09	5.90E-11	0.98
27	1.61E-09	1.58E-09	1.59E-09	1.62E-09	5.90E-11	0.98
28	1.67E-09	1.64E-09	1.65E-09	1.68E-09	5.90E-11	0.98
30	1.79E-09	1.75E-09	1.77E-09	1.80E-09	5.90E-11	0.98
35	**2.08E-09**	**2.04E-09**	**2.06E-09**	**2.10E-09**	**5.89E-11**	**0.98**

1.2v:

Buffer stages	Rise delay	Fall delay	Average delay	Expected delay	delay per stage	Error
1	5.99E-11	5.33E-11	5.66E-11	5.66E-11	5.66E-11	1.00
5	2.79E-10	2.69E-10	2.74E-10	2.83E-10	5.48E-11	0.97
10	5.53E-10	5.39E-10	5.46E-10	5.66E-10	5.46E-11	0.96
15	8.27E-10	8.09E-10	8.18E-10	8.49E-10	5.45E-11	0.96
20	1.10E-09	1.08E-09	1.09E-09	1.13E-09	5.45E-11	0.96
25	1.37E-09	1.35E-09	1.36E-09	1.42E-09	5.44E-11	0.96
35	1.92E-09	1.89E-09	1.90E-09	1.98E-09	5.44E-11	0.96
37	**2.03E-09**	**1.99E-09**	**2.01E-09**	**2.10E-09**	**5.44E-11**	**0.96**
38	2.09E-09	2.05E-09	2.07E-09	2.15E-09	5.44E-11	0.96
40	2.20E-09	2.16E-09	2.18E-09	2.27E-09	5.44E-11	0.96

1.3v:

Buffer stages	Rise delay	Fall delay	Average delay	Expected delay	delay per stage	Error
1	5.89E-11	4.94E-11	5.41E-11	5.41E-11	5.41E-11	1.00
5	2.65E-10	2.52E-10	2.58E-10	2.71E-10	5.16E-11	0.95
10	5.22E-10	5.05E-10	5.13E-10	5.41E-10	5.13E-11	0.95
15	7.80E-10	7.58E-10	7.69E-10	8.12E-10	5.12E-11	0.95
20	1.04E-09	1.01E-09	1.02E-09	1.08E-09	5.12E-11	0.95
25	1.29E-09	1.26E-09	1.28E-09	1.35E-09	5.12E-11	0.95
35	1.81E-09	1.77E-09	1.79E-09	1.89E-09	5.11E-11	0.94
37	1.91E-09	1.87E-09	1.89E-09	2.00E-09	5.11E-11	0.94
38	1.96E-09	1.92E-09	1.94E-09	2.06E-09	5.11E-11	0.94
40	**2.06E-09**	**2.02E-09**	**2.04E-09**	2.17E-09	5.11E-11	0.94

Number of buffer stages for different voltages (0.8v → 1.3v)

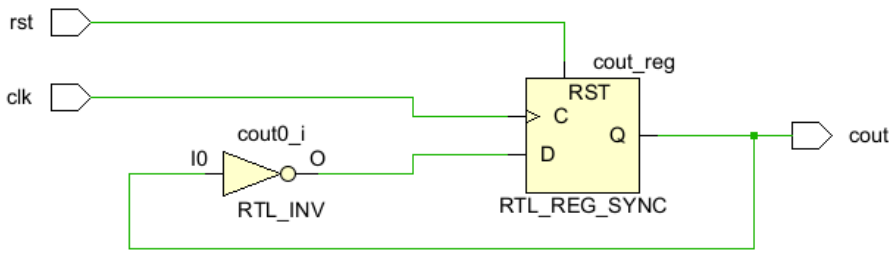
Voltage	Delay per stage	% change in delay	number of buffer stages	% bin change	Scale
1.3v	5.41E-11	17.53%	40	33.33%	10
1.2v	5.66E-11	13.72%	37	23.33%	7
1.1v	6.00E-11	8.54%	35	16.67%	5
1v	**6.56E-11**	0.00%	**30**	**0.00%**	**0**
0.9v	7.37E-11	-12.35%	26	-13.33%	-4
0.8v	8.74E-11	-33.23%	22	-26.67%	-8

Resolution of bin above 1v: 60ps

Resolution of bin below 1v: 50ps

Bin range	Scale	voltage difference (in mv)
40>	6	360
40 -41	5	300
38-39	4	240
36-37	3	180
34-35	2	120
32-33	1	60
30-31	0	0
28-29	-1	50
26-27	-2	100
24-25	-3	150
22-23	-4	200
<22	-5	250

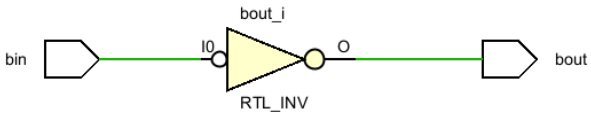
T-flip flop module:



In the Skitter module, a T (Toggle) Flip-Flop is used to ensure accurate detection of the clock signal's time period. Without the TFF, directly observing the output of D flip-flops connected to buffer stages and performing an XOR operation can result in two logic '1's per clock cycle, making it difficult to identify a complete time period.

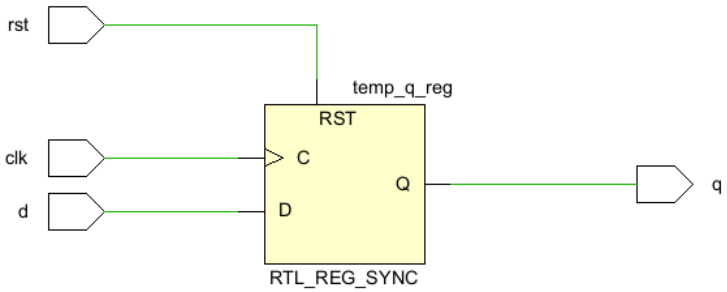
By introducing a TFF (which acts as a divide-by-2 circuit), the output clock period is effectively doubled. This simplifies the XOR output pattern, producing only one logic '1' per original clock cycle, making it easier to track and measure the full time period of the signal.

Buffer module:



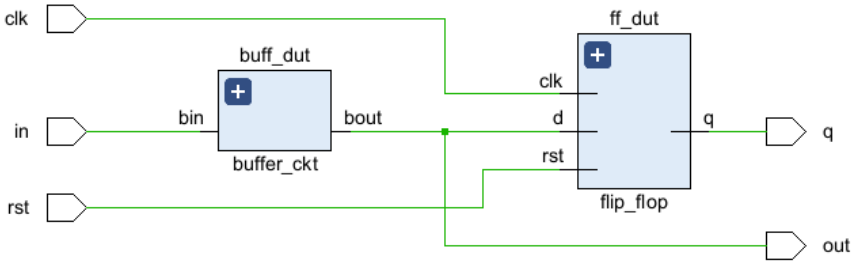
The buffer module is used to introduce controlled delay in the signal path, helping to observe timing variations caused by voltage fluctuations or process changes.

Flip flop module:



The D Flip-Flop is used to sample and store the delayed signal at each buffer stage, enabling the capture of timing changes across the signal path.

Flip flop with buffer module:



Dummy buffers:

Dummy buffers are a series of buffers connected without any flip-flops to avoid unnecessary clock power consumption. They are used solely to introduce a fixed delay in the signal path, which helps in observing how the clock signal's timing is affected by voltage variations.

These buffers simulate realistic propagation delay across different voltage conditions, for clock time period 2ns:

- For 1.3V:
    - Delay per buffer stage: **541 ps**
    - Required buffer stages: **37**
- For 0.8V:
    - Delay per buffer stage: **~90 ps**
    - Required buffer stages: **22**

In the design, **20 dummy buffer stages** are used without flip-flops to introduce delay while conserving clock power, and 4 buffers on either side is used as guard bits.

Encoder module:

The Encoder circuit is designed to identify the buffer stage at which one full clock period is observed. It takes inputs from all D Flip-Flop (DFF) outputs and uses XOR logic to detect the transition point that indicates a complete clock cycle.

For example, if the DFF output pattern is 11110000, the XOR logic detects a transition after the 4th flip-flop, indicating the clock period is completed at that stage.

The encoder then outputs the final stage index as:

Encoder Output = Transition Flip-Flop Index + Number of Dummy Buffers

Histogram :

The Histogram Logic is used to analyze voltage variations over time based on the output from the Encoder circuit.

The entire range of encoder outputs is divided into bins, where each bin represents a group of buffer stages (e.g., buffer stages 22 and 23 form a single bin).

Each bin is assigned to a dedicated counter. When the encoder output falls within a particular bin’s range, the corresponding counter starts incrementing with every clock cycle. This allows the histogram to track how long the system remains at a constant voltage (and thus the delay).

This enables the histogram to detect and reflect voltage changes:

- If only one counter is active throughout the simulation, it implies the system operated under constant voltage.
- If different counters activate over time, it indicates voltage variation during the simulation.

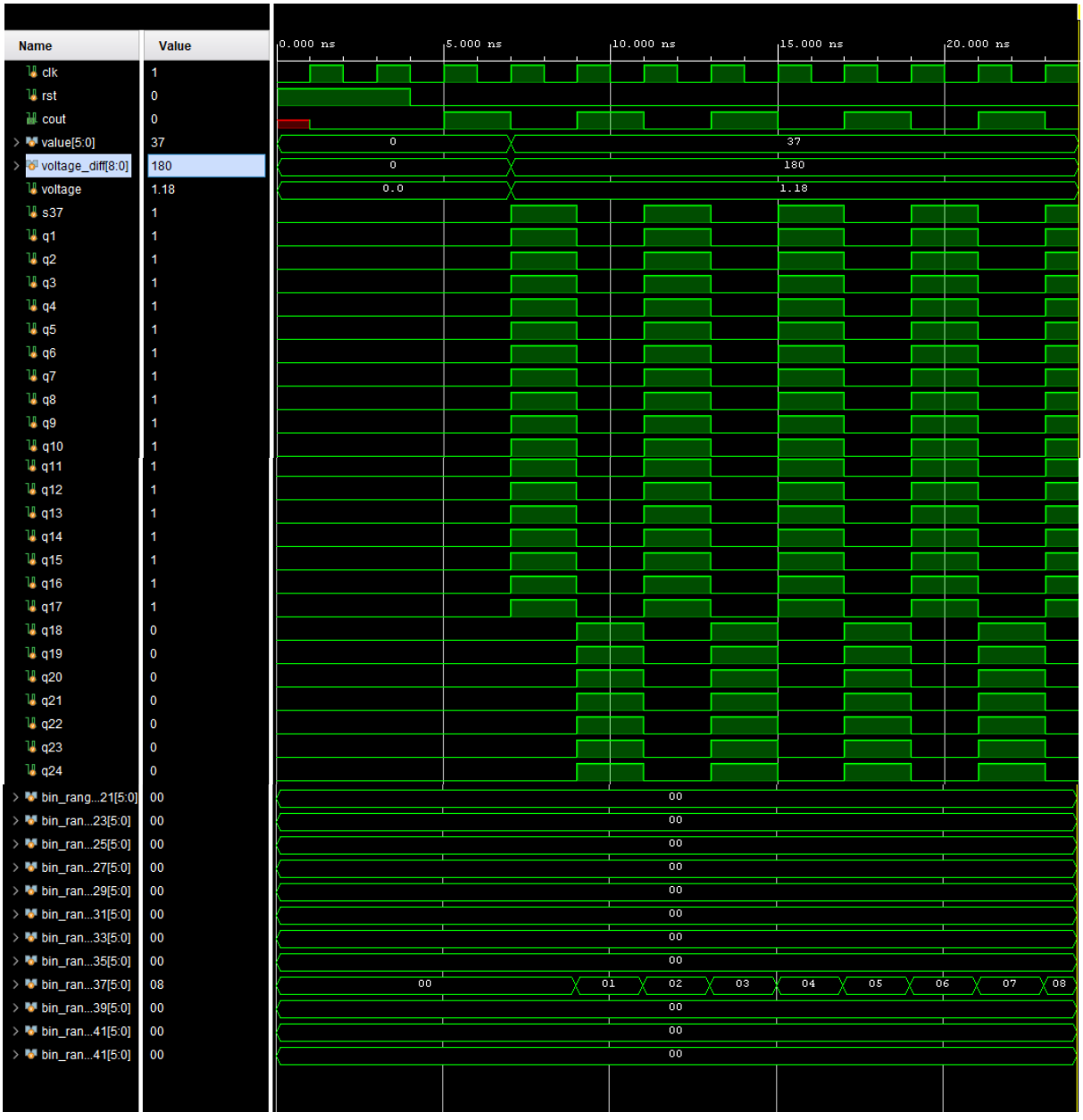
Voltage Difference output: Indicates how much the current voltage deviates from a reference value (e.g., 1V).

Estimated Voltage: Provides an estimate of the actual voltage level flowing through the circuit.

One stage buffer delay :

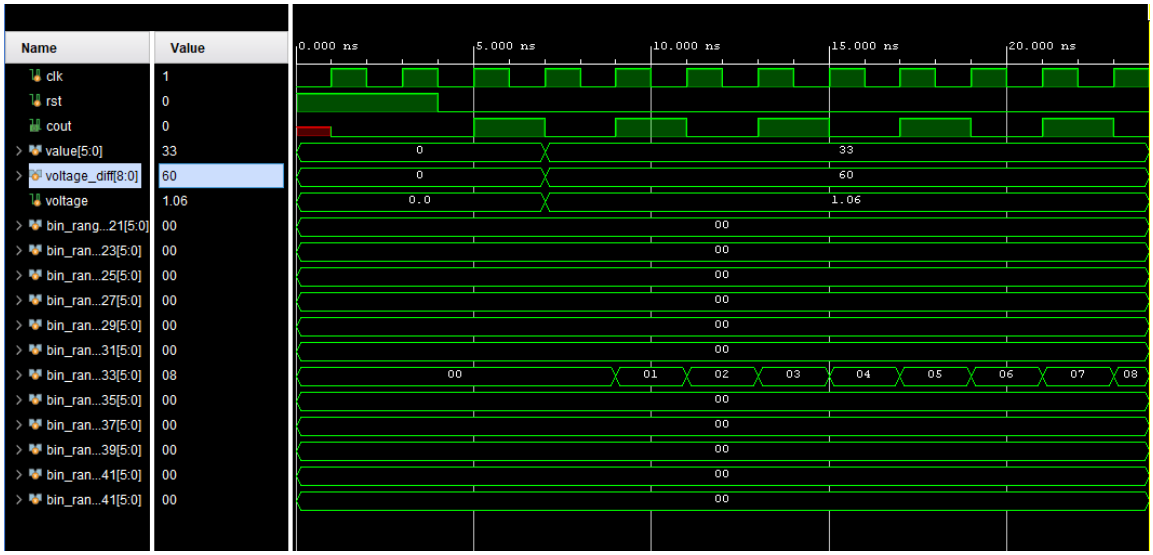
i) 54.1ps (2ns detected in bin stage : 37)

voltage difference : 180mv | Voltage is 1.18v



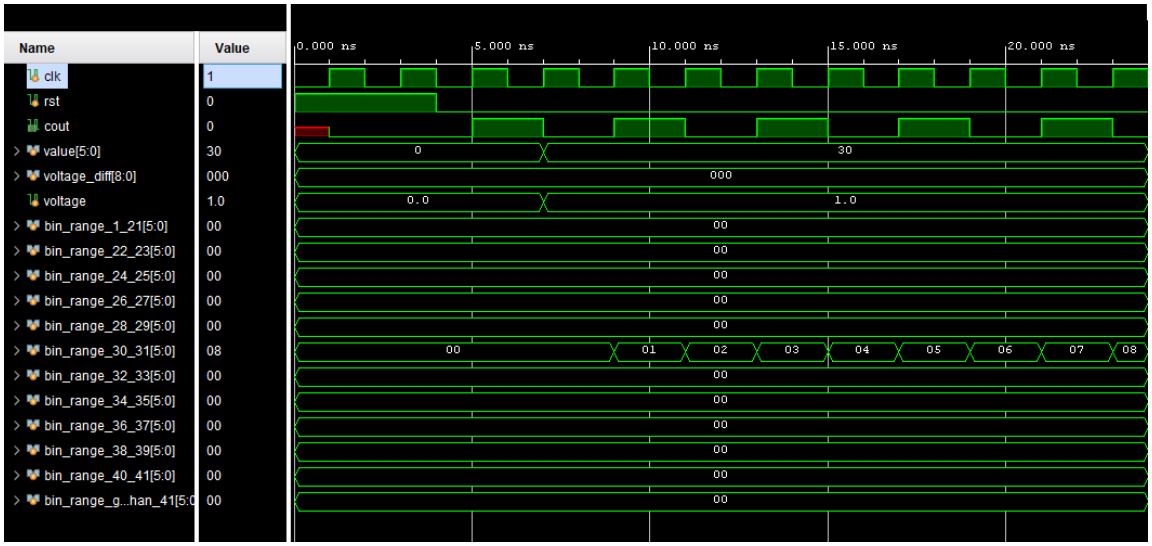
ii) 60ps (2ns detected in bin stage : 33)

voltage difference : 60mv | Voltage is : 1.06v



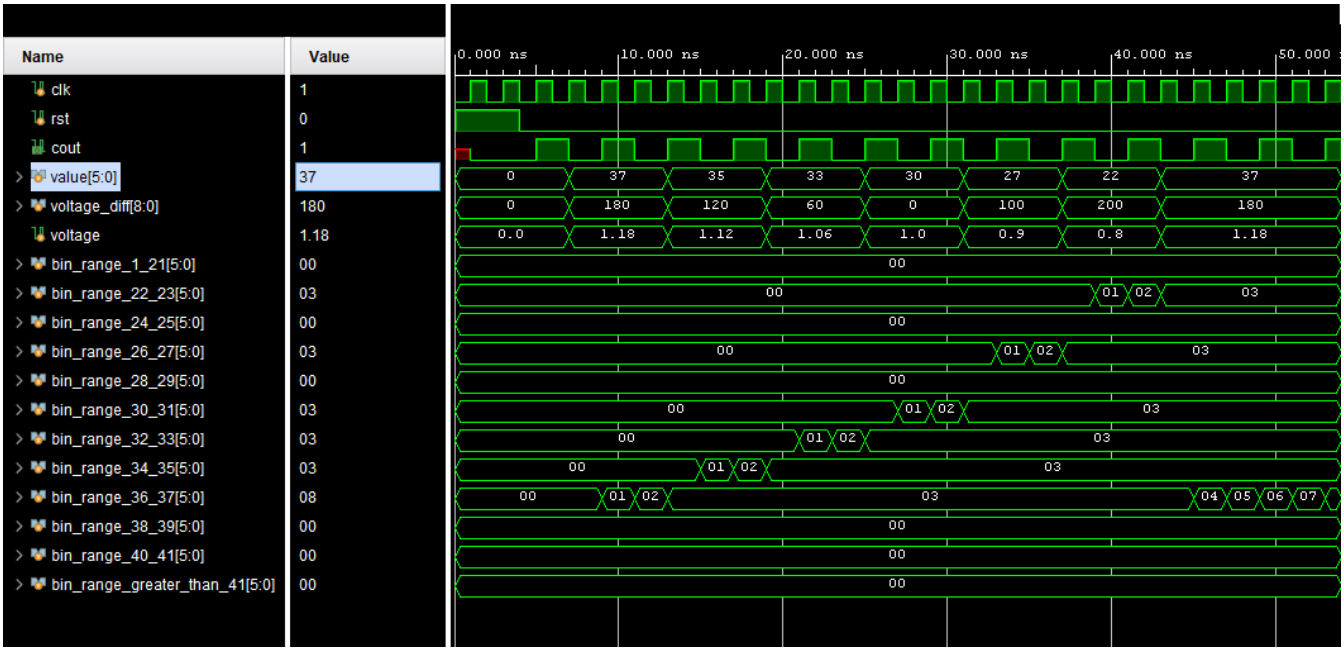
iii) 65.6ps (2ns detected in bin stage : 30)

voltage difference : 0mv | voltage : 1v



In the above waveforms, the delay remains constant over time, and also only one counter is active over the sim time, indicating that only a single voltage level is present throughout the circuit. Since there is no change in delay, it confirms that the voltage has remained stable during the entire simulation period.

Voltage variation at different simulation times:



In the above waveform, the delay changes after a certain simulation time, indicating that the voltage is varying during the operation. As a result, different histogram counters corresponding to specific bins become active and start counting, reflecting the transition between voltage levels over time.