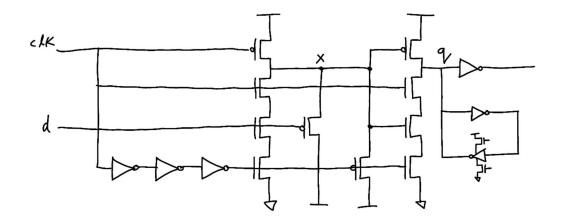
### **Hybrid Latched Flip Flop**

#### **Efficient HLFF:**



#### **Pulse Generation:**

- A clock pulse is generated internally by inverter delay chains that create the inverted clock (clkb).(3-stage inverter)
- The HLFF becomes transparent only during that pulse.

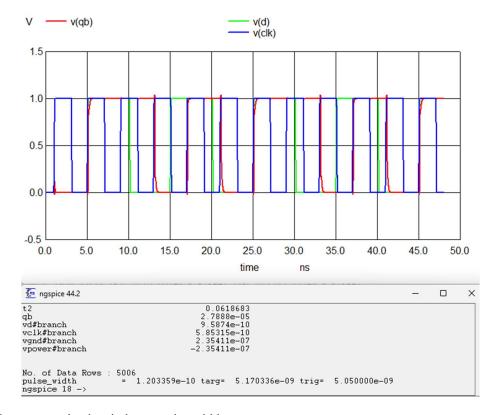
### **Data Sampling:**

- When the pulse is active (i.e. clk = 1, clkb = 0), the flip-flop allows the input D to pass through to an internal node.
- The latch closes immediately after the pulse ends, latching the sampled value.

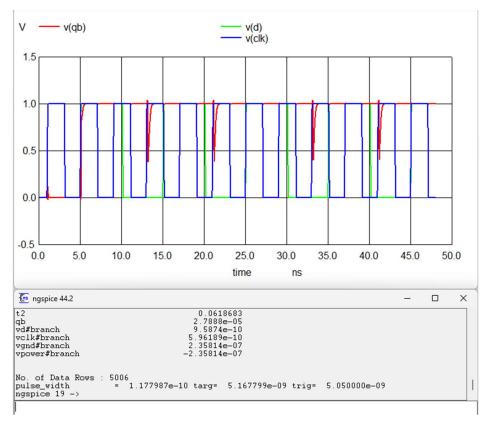
### **Data Storage:**

• A combination of tristate inverter and inverter holds the value even when the pulse is off.

### Minimum pulse width required to capture the data correctly: 120ps(1.20E-10)



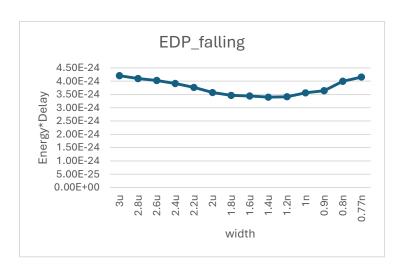
### Failed to capture the data in lesser pulse width:



Efficient HLFF: falling

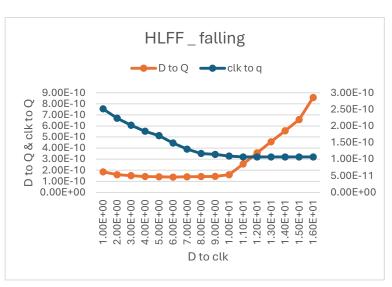
_	I	0					
Dvalue	d to clk	clk2q	delay	power	width	Energy	EDP(PDD)
1.914n	3.60E-11	9.51E-11	1.31E-10	2.45E-04	3u	3.21E-14	4.20E-24
1.9145n	3.55E-11	9.63E-11	1.32E-10	2.36E-04	2.8u	3.11E-14	4.10E-24
1.915n	3.50E-11	9.84E-11	1.33E-10	2.26E-04	2.6u	3.02E-14	4.03E-24
1.917n	3.30E-11	1.02E-10	1.34E-10	2.16E-04	2.4u	2.91E-14	3.91E-24
1.918n	3.20E-11	1.03E-10	1.35E-10	2.06E-04	2.2u	2.79E-14	3.77E-24
1.919u	3.00E-11	1.05E-10	1.35E-10	1.96E-04	2u	2.64E-14	3.57E-24
1.921n	2.90E-11	1.08E-10	1.37E-10	1.85E-04	1.8u	2.53E-14	3.47E-24
1.9228n	2.72E-11	1.13E-10	1.41E-10	1.74E-04	1.6u	2.45E-14	3.44E-24
1.923n	2.70E-11	1.17E-10	1.44E-10	1.64E-04	1.4u	2.36E-14	3.40E-24
1.925n	2.50E-11	1.24E-10	1.49E-10	1.53E-04	1.2n	2.28E-14	3.41E-24
1.926n	2.30E-11	1.34E-10	1.57E-10	1.44E-04	1n	2.27E-14	3.56E-24
1.927n	2.30E-11	1.41E-10	1.63E-10	1.37E-04	0.9n	2.23E-14	3.64E-24
1.927n	2.30E-11	1.51E-10	1.74E-10	1.32E-04	0.8n	2.30E-14	4.00E-24
1.924n	2.60E-11	1.52E-10	1.79E-10	1.29E-04	0.77n	2.32E-14	4.15E-24

### EDP falling:

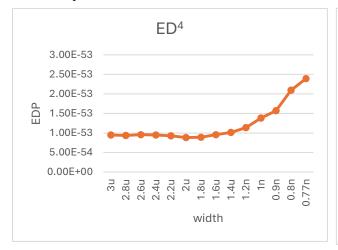


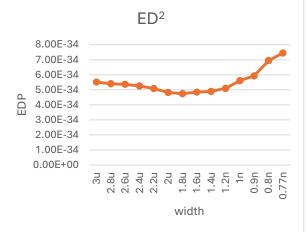
**Setup time characterization**: falling (setup time : 117ps (10% rise of clk to q))

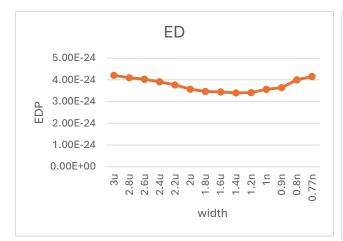
D value	D to clk	clk to Q	D to Q
2.006n	-5.60E-11	2.51E-10	1.85E-10
2.004n	-5.40E-11	2.23E-10	1.59E-10
2n	-5.00E-11	2.02E-10	1.52E-10
1.99n	-4.00E-11	1.84E-10	1.44E-10
1.98n	-3.00E-11	1.71E-10	1.41E-10
1.96n	-1.00E-11	1.49E-10	1.39E-10
1.94n	1.00E-11	1.30E-10	1.40E-10
1.924n	2.60E-11	1.17E-10	1.43E-10
1.92n	3.00E-11	1.15E-10	1.46E-10
1.9n	5.00E-11	1.09E-10	1.59E-10
1.8n	1.50E-10	1.07E-10	2.57E-10
1.7n	2.50E-10	1.07E-10	3.57E-10
1.6n	3.50E-10	1.07E-10	4.57E-10
1.5n	4.50E-10	1.07E-10	5.57E-10
1.4n	5.50E-10	1.07E-10	6.57E-10
1.2n	7.50E-10	1.07E-10	8.57E-10

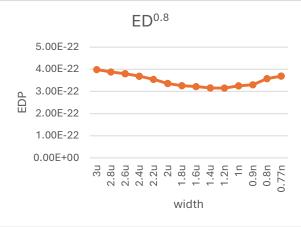


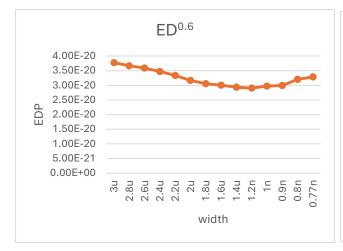
### **EDP** plots:

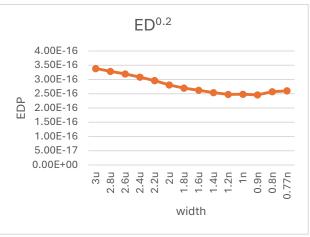






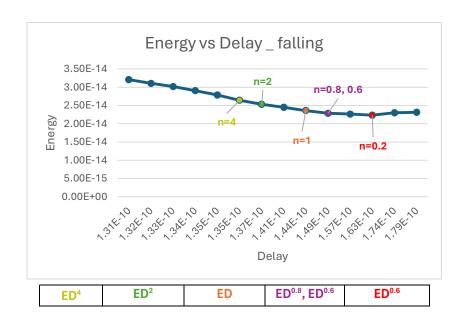






# Energy vs Delay: falling

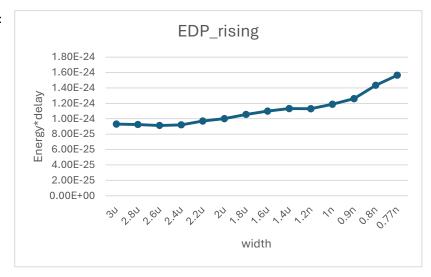
75.00 0.005.16
7E-20 3.39E-16
7E-20 3.28E-16
9E-20 3.20E-16
7E-20 3.09E-16
4E-20 2.96E-16
7E-20 2.81E-16
6E-20 2.70E-16
1E-20 2.62E-16
4E-20 2.54E-16
1E-20 2.48E-16
7E-20 2.48E-16
9E-20 <b>2.46E-16</b>
1E-20 2.57E-16
9E-20 2.60E-16
99



### Rising:

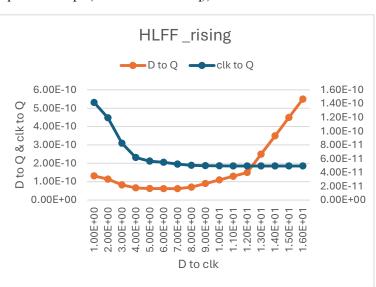
Dvalue	d to clk	clk2q	delay	power	width	Energy	EDP(PDD)
1.993n	7.00E-12	5.17E-11	5.87E-11	2.70E-04	3u	1.58E-14	9.30E-25
1.9925n	7.50E-12	5.25E-11	6.00E-11	2.57E-04	2.8u	1.54E-14	9.24E-25
1.9923n	7.70E-12	5.43E-11	6.12E-11	2.44E-04	2.6u	1.49E-14	9.13E-25
1.9927n	7.30E-12	5.71E-11	6.31E-11	2.31E-04	2.4u	1.46E-14	9.20E-25
1.9931n	6.90E-12	5.96E-11	6.65E-11	2.19E-04	2.2u	1.46E-14	9.69E-25
1.992n	8.00E-12	6.18E-11	6.98E-11	2.05E-04	2u	1.43E-14	1.00E-24
1.9915n	8.50E-12	6.55E-11	7.40E-11	1.93E-04	1.8u	1.43E-14	1.06E-24
1.993n	7.00E-12	7.08E-11	7.78E-11	1.81E-04	1.6u	1.41E-14	1.10E-24
1.9945n	5.50E-12	7.73E-11	8.28E-11	1.65E-04	1.4u	1.37E-14	1.13E-24
1.997n	4.00E-12	8.65E-11	9.05E-11	1.38E-04	1.2n	1.25E-14	1.13E-24
1.998n	2.00E-12	9.83E-11	1.00E-10	1.18E-04	1n	1.18E-14	1.19E-24
1.999n	1.00E-12	1.06E-10	1.13E-10	9.80E-05	0.9n	1.11E-14	1.26E-24
1.999n	1.00E-12	1.17E-10	1.25E-10	9.15E-05	0.8n	1.15E-14	1.43E-24
1.999n	1.00E-12	1.22E-10	1.33E-10	8.87E-05	0.77n	1.18E-14	1.57E-24

### **EDP** rising:

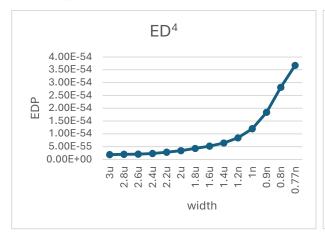


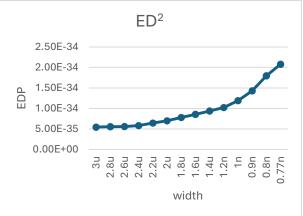
**Setup time characterization**: falling (setup time : 117ps (10% rise of clk to q))

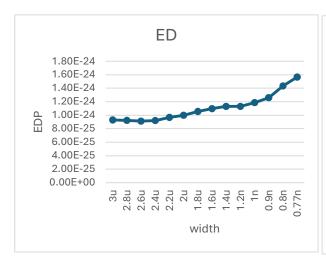
D value	D to clk	clk to Q	D to Q
2.01n	-1.00E-11	1.42E-10	1.32E-10
2.002n	-6.00E-12	1.19E-10	1.13E-10
2n	0.00E+00	8.25E-11	8.25E-11
1.996n	4.00E-12	6.18E-11	6.58E-11
1.994n	6.00E-12	5.64E-11	6.24E-11
1.9925n	7.50E-12	5.47E-11	6.22E-11
1.99n	1.00E-11	5.22E-11	6.22E-11
1.98n	2.00E-11	5.04E-11	7.04E-11
1.96n	4.00E-11	5.00E-11	9.00E-11
1.94n	6.00E-11	4.96E-11	1.10E-10
1.92n	8.00E-11	4.95E-11	1.30E-10
1.9n	1.00E-10	4.95E-11	1.49E-10
1.8n	2.00E-10	4.94E-11	2.49E-10
1.7n	3.00E-10	4.94E-11	3.49E-10
1.6n	4.00E-10	4.94E-11	4.49E-10
1.5n	5.00E-10	4.94E-11	5.49E-10

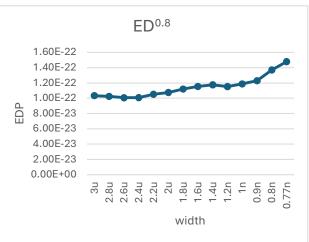


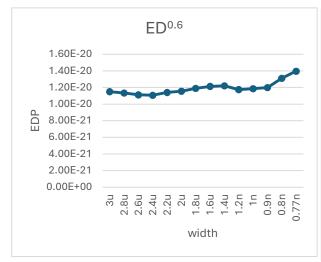
#### EDP plots: rising

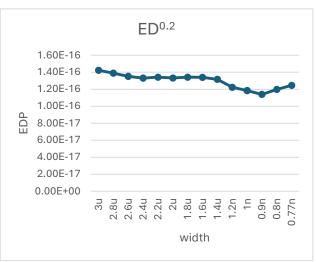






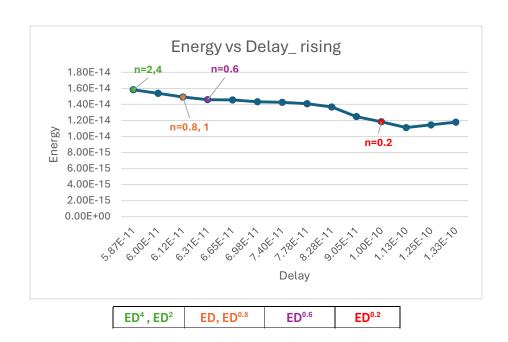






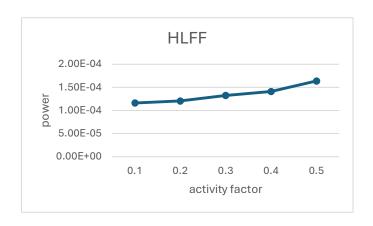
# Energy vs Delay: rising

delay	power	width	Energy	EDP(PDD)	ED4	ED2	ED0.8	ED0.6	ED0.2
5.87E-11	2.70E-04	3u	1.58E-14	9.30E-25	1.88E-55	5.45E-35	1.03E-22	1.15E-20	1.42E-16
6.00E-11	2.57E-04	2.8u	1.54E-14	9.24E-25	1.99E-55	5.54E-35	1.02E-22	1.13E-20	1.39E-16
6.12E-11	2.44E-04	2.6u	1.49E-14	9.13E-25	2.09E-55	5.59E-35	1.01E-22	1.11E-20	1.35E-16
6.31E-11	2.31E-04	2.4u	1.46E-14	9.20E-25	2.31E-55	5.80E-35	1.01E-22	1.11E-20	1.33E-16
6.65E-11	2.19E-04	2.2u	1.46E-14	9.69E-25	2.85E-55	6.44E-35	1.05E-22	1.14E-20	1.34E-16
6.98E-11	2.05E-04	2u	1.43E-14	1.00E-24	3.40E-55	6.98E-35	1.07E-22	1.16E-20	1.33E-16
7.40E-11	1.93E-04	1.8u	1.43E-14	1.06E-24	4.27E-55	7.81E-35	1.12E-22	1.19E-20	1.34E-16
7.78E-11	1.81E-04	1.6u	1.41E-14	1.10E-24	5.18E-55	8.54E-35	1.15E-22	1.21E-20	1.34E-16
8.28E-11	1.65E-04	1.4u	1.37E-14	1.13E-24	6.42E-55	9.37E-35	1.18E-22	1.22E-20	1.32E-16
9.05E-11	1.38E-04	1.2n	1.25E-14	1.13E-24	8.38E-55	1.02E-34	1.15E-22	1.18E-20	1.22E-16
1.00E-10	1.18E-04	<b>1</b> n	1.18E-14	1.19E-24	1.20E-54	1.19E-34	1.19E-22	1.19E-20	1.18E-16
1.13E-10	9.80E-05	0.9n	1.11E-14	1.26E-24	1.84E-54	1.43E-34	1.23E-22	1.20E-20	1.14E-16
1.25E-10	9.15E-05	0.8n	1.15E-14	1.43E-24	2.81E-54	1.79E-34	1.37E-22	1.31E-20	1.20E-16
1.33E-10	8.87E-05	0.77n	1.18E-14	1.57E-24	3.67E-54	2.08E-34	1.48E-22	1.40E-20	1.25E-16



# Power vs Activity factor:

activity factor	power
0.1	1.16E-04
0.2	1.20E-04
0.3	1.33E-04
0.4	1.41E-04
0.5	1.64E-04
slope	1.19E-04



# **HLFF** power:

clk, data	Static power
0,0	2.35E-07
0,1	2.44E-07
1,0	3.07E-08
1,1	4.08E-08
Avg =	1.38E-07
total power	1.64E-04

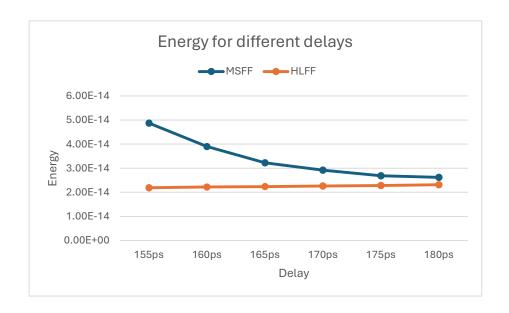
clk	data switching power		
0	1.95E-05		
1	1.18E-05		
Avg=	1.57E-05		
Rswitching	1.48E-04		

data	clk power
0	1.52E-04
1	5.57E-05
Avg=	1.04E-04

The efficient circuit of HLFF is in falling transition, because the worst case is in falling transition in terms of EDP.

# **Energy for different delays**: (MSFF and HLFF)

			MSFF						HLFF			
	Dvalue	setup	clk2q	delay	power	Energy	Dvalue	setup	clk2q	delay	power	Energy
155ps	1.873n	7.70E-11	7.86E-11	1.56E-10	3.13E-04	4.87E-14	1.926n	2.30E-11	1.34E-10	1.56E-10	1.40E-04	2.19E-14
160ps	1.8746n	7.54E-11	8.34E-11	1.59E-10	2.46E-04	3.90E-14	1.927n	2.33E-11	1.39E-10	1.62E-10	1.37E-04	2.22E-14
165ps	1.875n	7.50E-11	9.00E-11	1.65E-10	1.96E-04	3.23E-14	1.927n	2.39E-11	1.42E-10	1.66E-10	1.35E-04	2.24E-14
170ps	1.874n	7.60E-11	9.49E-11	1.71E-10	1.71E-04	2.92E-14	1.927n	2.43E-11	1.46E-10	1.70E-10	1.33E-04	2.26E-14
175ps	1.873n	7.70E-11	1.03E-10	1.76E-10	1.53E-04	2.69E-14	1.927n	2.50E-11	1.50E-10	1.74E-10	1.31E-04	2.28E-14
180ps	1.873n	7.70E-11	1.03E-10	1.80E-10	1.46E-04	2.62E-14	1.924n	2.60E-11	1.52E-10	1.79E-10	1.29E-04	2.32E-14



### Power vs Activity factor of MSFF and HLFF

	MSFF	HLFF
activity factor	power	power
0.1	7.30E-05	1.16E-04
0.2	8.79E-05	1.20E-04
0.3	9.94E-05	1.33E-04
0.4	1.14E-04	1.41E-04
0.5	1.34E-04	1.64E-04
slope	1.52E-04	1.19E-04

