Microprocessor and Computer Architecture Laboratory

UE22CS251B

4th Semester, Academic Year 2023-24

Date:03-04-2024

Name: ANKITH GOWDA B S	SRN:PES2UG22CS077	Section : B

Week#____6_____ Exercise: ____1__

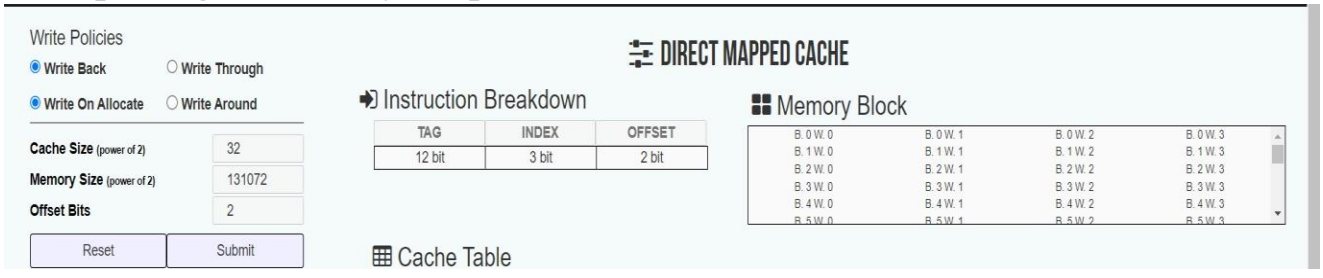
1. Use PARACACHE SIMULATOR for the exercise below given the following configuration .
   a. Cache Size: 32 words
   b. Memory Size: 131072 words[main memory].
   c. Block Size: 4 words.

      Use Write back policy

      Also, repeat the exercise for Write through policy.

Include One Screenshot(for Write Back Cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor



ii) Screenshot showing the Cache Table

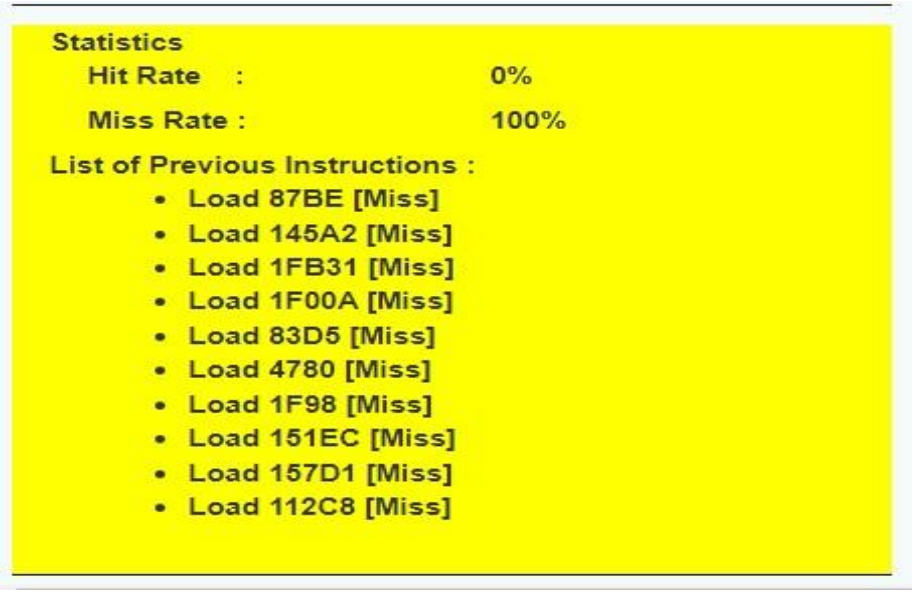
Generating random numbers

Cache Table

Cache Table

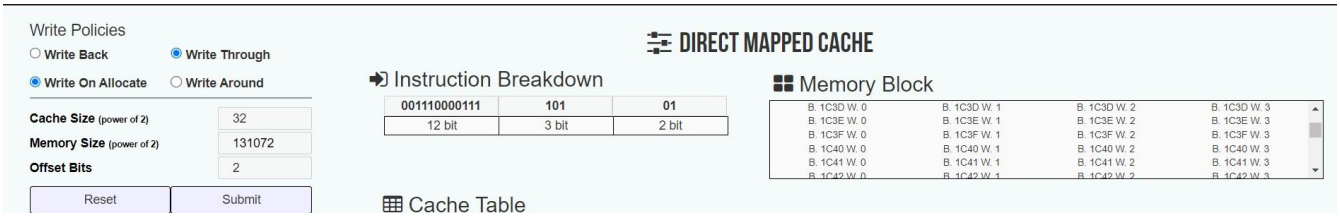
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	001000111100	BLOCK 11E0 WORD 0 - 3	0
1	0	-	0	0
2	1	100010010110	BLOCK 44B2 WORD 0 - 3	0
3	1	101010001111	BLOCK 547B WORD 0 - 3	0
4	1	101010111110	BLOCK 55F4 WORD 0 - 3	0
5	1	010000011110	BLOCK 20F5 WORD 0 - 3	0
6	1	000011111100	BLOCK 7E6 WORD 0 - 3	0
7	1	010000111101	BLOCK 21EF WORD 0 - 3	0

iii) Screenshot showing hit and miss rates



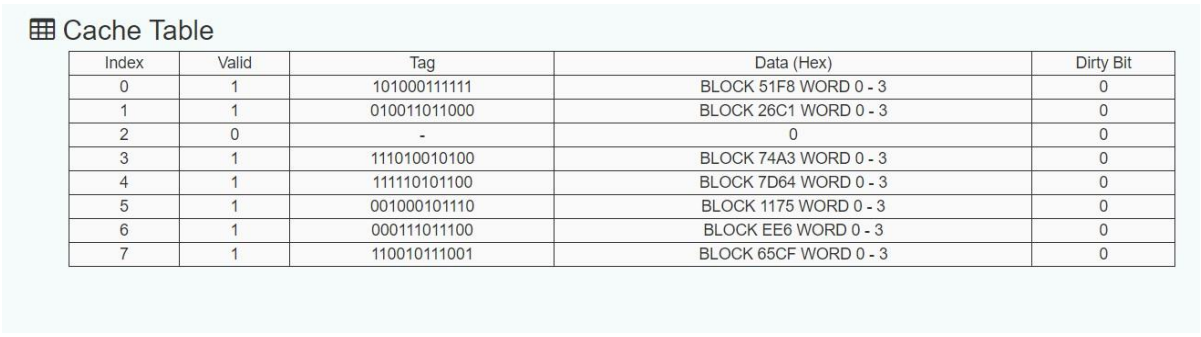
Include One Screenshot(for Write Through Cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor



ii) Screenshot showing the Cache Table Generating random numbers

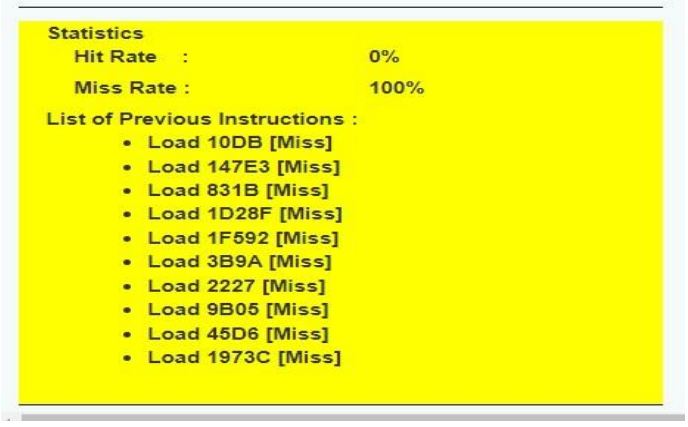
Cache Table



Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	101000111111	BLOCK 51F8 WORD 0 - 3	0
1	1	010011011000	BLOCK 26C1 WORD 0 - 3	0
2	0	-	0	0
3	1	111010010100	BLOCK 74A3 WORD 0 - 3	0
4	1	111110101100	BLOCK 7D64 WORD 0 - 3	0
5	1	001000101110	BLOCK 1175 WORD 0 - 3	0
6	1	000111011100	BLOCK EE6 WORD 0 - 3	0
7	1	110010111001	BLOCK 65CF WORD 0 - 3	0

iii) Screenshot showing hit and miss rates



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Week#____6_____ Exercise: ____3__

3. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Cache Size: 32 words

Memory Size: 16-bit memory address

Block Size: 16 words.

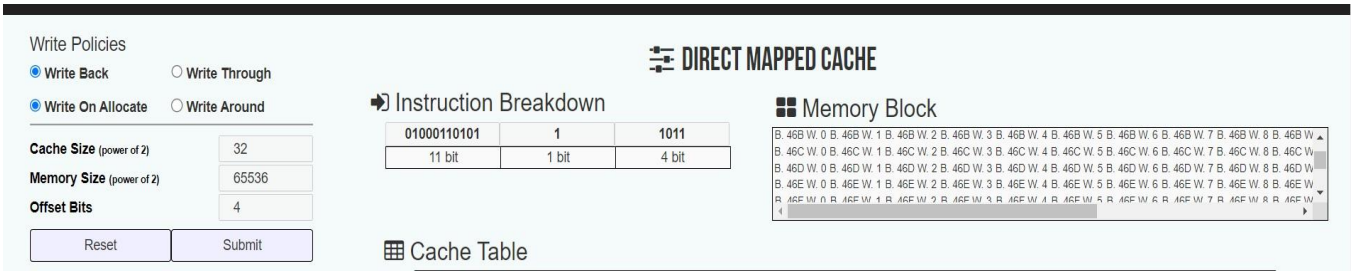
Use Write back policy

Also, repeat the exercise for Write through policy.

a.) Write Back

Include One Screenshot for each case with

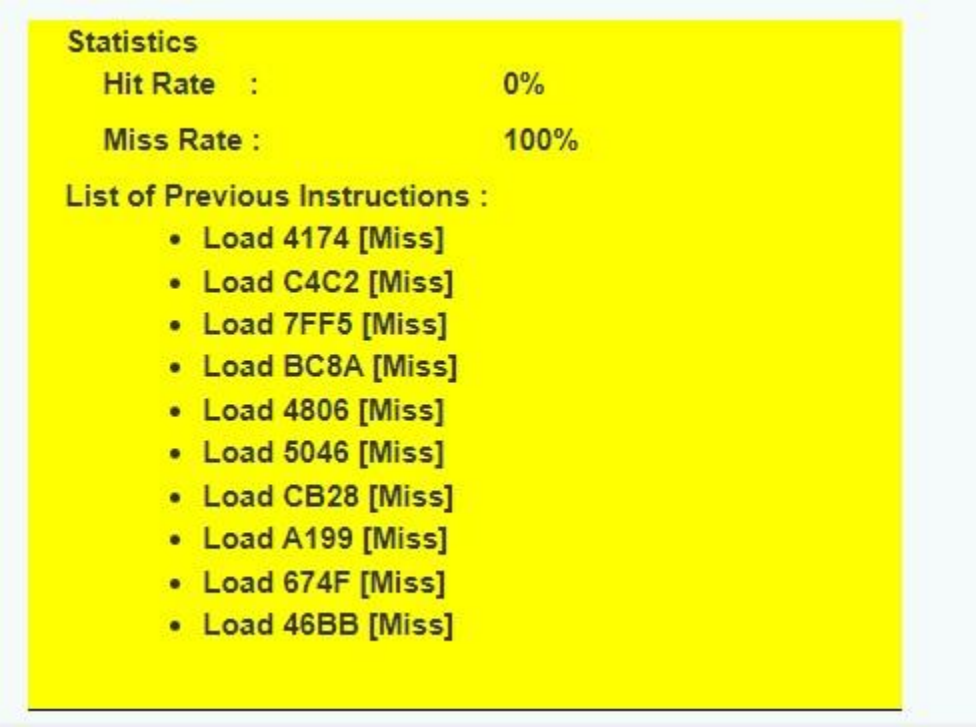
i) **Cache Address Table showing the splitup of the address fields for the requests generated by the processor**
ii) **Screenshot showing the Cache Table**



Cache Table

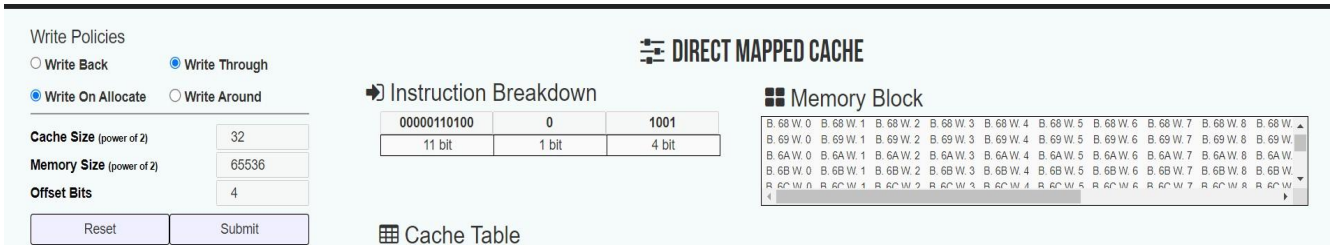
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	01100111010	BLOCK 674 WORD 0 - 15	0
1	1	01000110101	BLOCK 46B WORD 0 - 15	0

iii) Screenshot showing hit and miss rates



b.) Write Through

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

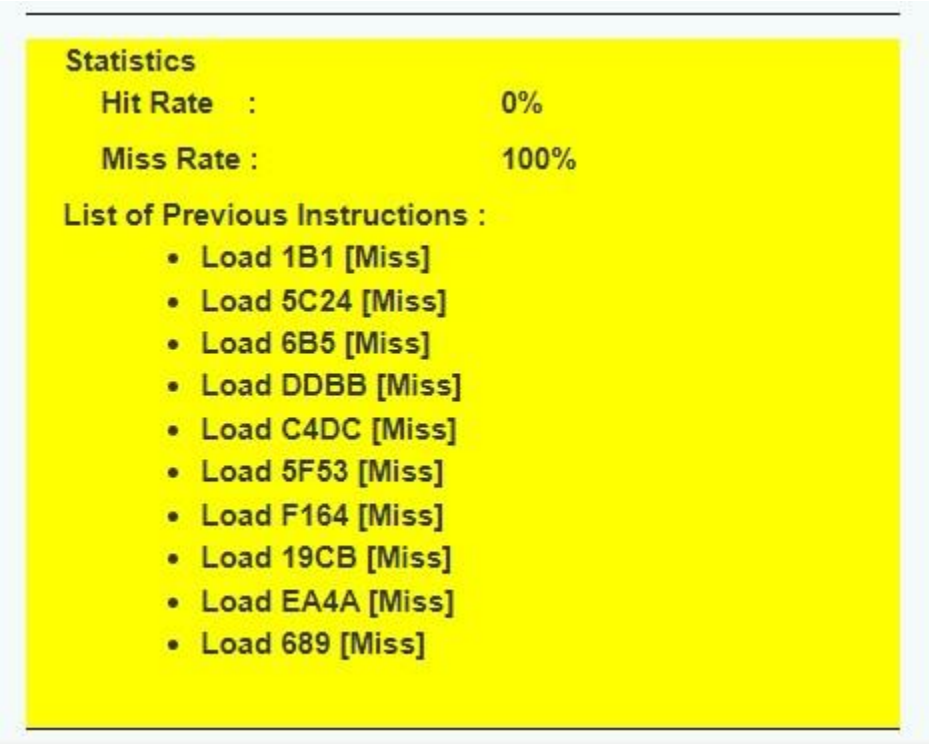


ii) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000110100	BLOCK 68 WORD 0 - 15	0
1	1	01011111010	BLOCK 5F5 WORD 0 - 15	0

iii) Screenshot showing hit and miss rates



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- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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