

Microprocessor and Computer Architecture Laboratory

UE22CS251B

4th Semester, Academic Year 2023-24

Date:03-04-2024

Name: ANKITH GOWDA B S	SRN:PES2UG22CS077	Section : B
------------------------	-------------------	-------------

Week# ____6____

Exercise: ____1____

1. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

- Cache Size: 32 words
- Memory Size: 131072 words[main memory].
- Block Size: 4 words.

Use Write back policy

Also, repeat the exercise for Write through policy.

Include One Screenshot(for Write Back Cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

The screenshot shows the PARACACHE SIMULATOR interface. On the left, under 'Write Policies', 'Write Back' is selected. Below it, 'Cache Size (power of 2)' is set to 32, 'Memory Size (power of 2)' is set to 131072, and 'Offset Bits' is set to 2. There are 'Reset' and 'Submit' buttons. In the center, 'Instruction Breakdown' shows a table with columns TAG (12 bit), INDEX (3 bit), and OFFSET (2 bit). On the right, 'DIRECT MAPPED CACHE' is selected, and 'Memory Block' shows a grid of 20 blocks labeled B.0W.0 to B.5W.3. At the bottom, there is a 'Cache Table' icon.

ii) Screenshot showing the Cache Table

Generating random numbers

Instruction

Load

(in hex)#

87be

145a2,1fb31,1f00a,83d5,4780,1f98,151ec,157

Gen. Random

Submit

Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	001000111100	BLOCK 11E0 WORD 0 - 3	0
1	0	-	0	0
2	1	100010010110	BLOCK 44B2 WORD 0 - 3	0
3	1	101010001111	BLOCK 547B WORD 0 - 3	0
4	1	101010111110	BLOCK 55F4 WORD 0 - 3	0
5	1	010000011110	BLOCK 20F5 WORD 0 - 3	0
6	1	000011111100	BLOCK 7E6 WORD 0 - 3	0
7	1	010000111101	BLOCK 21EF WORD 0 - 3	0

iii) Screenshot showing hit and miss rates

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load 87BE [Miss]
- Load 145A2 [Miss]
- Load 1FB31 [Miss]
- Load 1F00A [Miss]
- Load 83D5 [Miss]
- Load 4780 [Miss]
- Load 1F98 [Miss]
- Load 151EC [Miss]
- Load 157D1 [Miss]
- Load 112C8 [Miss]

Include One Screenshot(for Write Through Cache) with

- Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Write Policies
☐ Write Back ☒ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 32
Memory Size (power of 2): 131072
Offset Bits: 2

DIRECT MAPPED CACHE

Instruction Breakdown
001110000111 101 01
12 bit 3 bit 2 bit

Memory Block

B: 1C3D W: 0	B: 1C3D W: 1	B: 1C3D W: 2	B: 1C3D W: 3
B: 1C3E W: 0	B: 1C3E W: 1	B: 1C3E W: 2	B: 1C3E W: 3
B: 1C3F W: 0	B: 1C3F W: 1	B: 1C3F W: 2	B: 1C3F W: 3
B: 1C40 W: 0	B: 1C40 W: 1	B: 1C40 W: 2	B: 1C40 W: 3
B: 1C41 W: 0	B: 1C41 W: 1	B: 1C41 W: 2	B: 1C41 W: 3
B: 1C42 W: 0	B: 1C42 W: 1	B: 1C42 W: 2	B: 1C42 W: 3

ii) Screenshot showing the Cache Table

Generating random numbers

Instruction

Load (in hex)# 10db

147e3,831b,1d28f,1f592,3b9a,2227,9b05,45d6

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	101000111111	BLOCK 51F8 WORD 0 - 3	0
1	1	010011011000	BLOCK 26C1 WORD 0 - 3	0
2	0	-	0	0
3	1	111010010100	BLOCK 74A3 WORD 0 - 3	0
4	1	111110101100	BLOCK 7D64 WORD 0 - 3	0
5	1	001000101110	BLOCK 1175 WORD 0 - 3	0
6	1	000111011100	BLOCK EE6 WORD 0 - 3	0
7	1	110010111001	BLOCK 65CF WORD 0 - 3	0

iii) Screenshot showing hit and miss rates

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load 10DB [Miss]
- Load 147E3 [Miss]
- Load 831B [Miss]
- Load 1D28F [Miss]
- Load 1F592 [Miss]
- Load 3B9A [Miss]
- Load 2227 [Miss]
- Load 9B05 [Miss]
- Load 45D6 [Miss]
- Load 1973C [Miss]

Microprocessor and Computer Architecture Laboratory

UE22CS251B

4th Semester, Academic Year 2023-24

Date:03-04-2024

Name: ANKITH GOWDA B S	SRN:PES2UG22CS077	Section : B
------------------------	-------------------	-------------

Week# 6 Exercise: 3

3. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Cache Size: 32 words

Memory Size: 16-bit memory address

Block Size: 16 words.

Use Write back policy

Also, repeat the exercise for Write through policy.

a.) Write Back

Include One Screenshot for each case with

- Cache Address Table showing the splitup of the address fields for the requests generated by the processor**
- Screenshot showing the Cache Table**

The screenshot displays the PARACACHE SIMULATOR interface. On the left, under 'Write Policies', 'Write Back' is selected. Configuration parameters are set to: Cache Size (power of 2) = 32, Memory Size (power of 2) = 65536, and Offset Bits = 4. Buttons for 'Reset' and 'Submit' are at the bottom left. The main area is titled 'DIRECT MAPPED CACHE'. It features an 'Instruction Breakdown' table showing a 11-bit address split into three fields: 01000110101 (11 bit), 1 (1 bit), and 1011 (4 bit). Below this is a 'Cache Table' icon. On the right, a 'Memory Block' list shows addresses from 46B W 0 B to 46E W 4 B, with a scrollbar indicating a large list of memory blocks.

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	01100111010	BLOCK 674 WORD 0 - 15	0
1	1	01000110101	BLOCK 46B WORD 0 - 15	0

iii) Screenshot showing hit and miss rates

Statistics

Hit Rate :	0%
Miss Rate :	100%

List of Previous Instructions :

- Load 4174 [Miss]
- Load C4C2 [Miss]
- Load 7FF5 [Miss]
- Load BC8A [Miss]
- Load 4806 [Miss]
- Load 5046 [Miss]
- Load CB28 [Miss]
- Load A199 [Miss]
- Load 674F [Miss]
- Load 46BB [Miss]

b.) Write Through

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Write Policies

☐ Write Back
 ☒ Write Through

☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

65536

Offset Bits

4

Reset

Submit

DIRECT MAPPED CACHE

Instruction Breakdown

00000110100	0	1001
11 bit	1 bit	4 bit

Memory Block

B. 68 W. 0	B. 68 W. 1	B. 68 W. 2	B. 68 W. 3	B. 68 W. 4	B. 68 W. 5	B. 68 W. 6	B. 68 W. 7	B. 68 W. 8	B. 68 W. 9
B. 69 W. 0	B. 69 W. 1	B. 69 W. 2	B. 69 W. 3	B. 69 W. 4	B. 69 W. 5	B. 69 W. 6	B. 69 W. 7	B. 69 W. 8	B. 69 W. 9
B. 6A W. 0	B. 6A W. 1	B. 6A W. 2	B. 6A W. 3	B. 6A W. 4	B. 6A W. 5	B. 6A W. 6	B. 6A W. 7	B. 6A W. 8	B. 6A W. 9
B. 6B W. 0	B. 6B W. 1	B. 6B W. 2	B. 6B W. 3	B. 6B W. 4	B. 6B W. 5	B. 6B W. 6	B. 6B W. 7	B. 6B W. 8	B. 6B W. 9
B. 6C W. 0	B. 6C W. 1	B. 6C W. 2	B. 6C W. 3	B. 6C W. 4	B. 6C W. 5	B. 6C W. 6	B. 6C W. 7	B. 6C W. 8	B. 6C W. 9

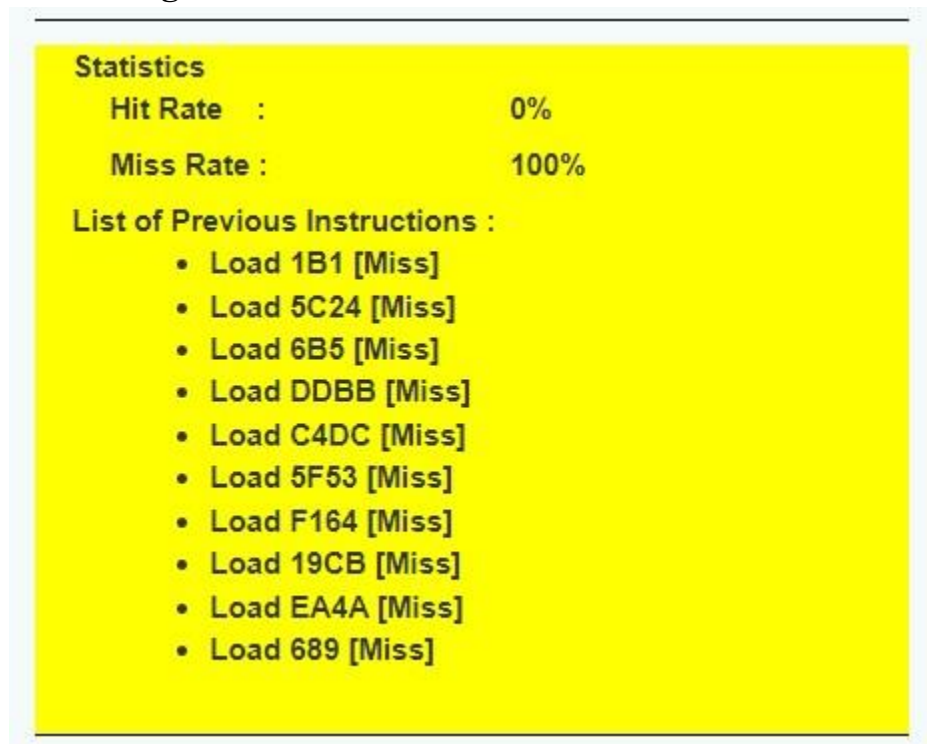
Cache Table

ii) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000110100	BLOCK 68 WORD 0 - 15	0
1	1	01011111010	BLOCK 5F5 WORD 0 - 15	0

iii) Screenshot showing hit and miss rates



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Name: ANKITH GOWDA B S

SRN: PES2UG22CS077

Section: B

Date: 03-04-2024