ASSESSMENT - 2

COMBINATIONAL LOGIC - SOLUTIONS

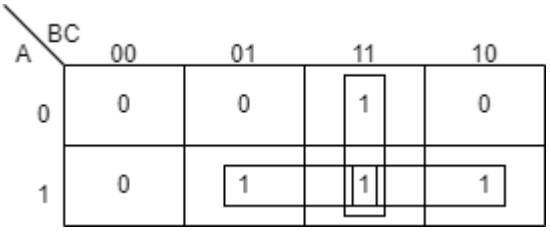
1. A majority function is generated in a combinational circuit, where the output is equal to 1 if the input variables have more 1's than 0's otherwise the output is 0. Design a three-input majority function. (2)

   Ans:

   TT - 1

   Eqn and kmap 1

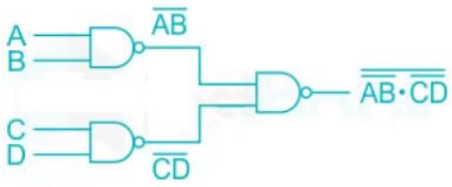
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



   Y = AB + AC + BC

2. Implement y = AB + CD using NAND gates (1)

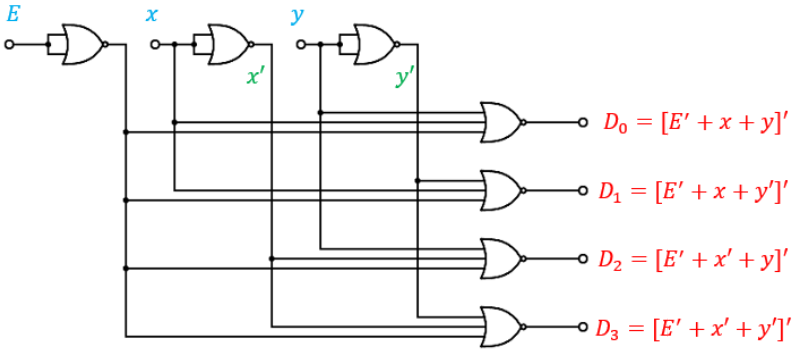
   Ans:



$$y = AB + CD$$
$$= \overline{\overline{AB + CD}}$$
$$= \overline{\overline{AB}.\overline{CD}}$$

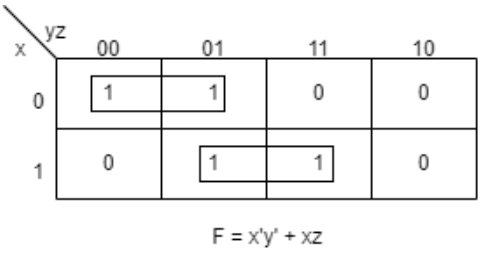
3. Draw the logic diagram of a 2-to-4-line decoder with only NOR gates. Include an enable input. (2)

Ans:

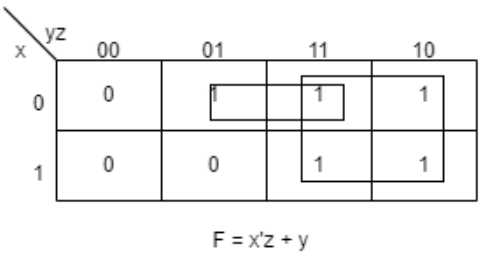


4. Simplify the following Boolean functions using three-variable maps. (2)
   a. F(x,y,z) = Σ(0, 1,5, 7)
   b. F(x,y,z) = Σ(1, 2, 3,6,7)
   c. F(x,y,z) = Σ(3,5,6,7)
   d. F(x,y,z) = Σ(0,2,3,4,6)

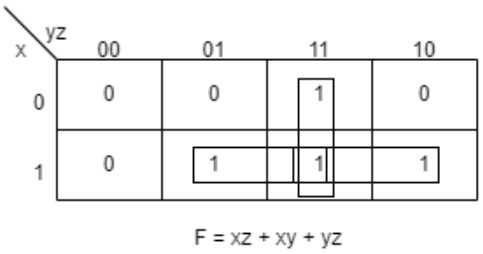
Ans:



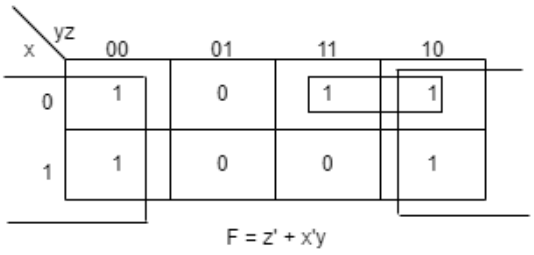
F = x'y' + xz



F = x'z + y



F = xz + xy + yz



F = z' + x'y

5. Prove De Morgan's theorem (2)

Ans:

a) 1st theorem

$\overline{(X+Y)} = X' . Y'$

Proof :

if X = 0 and Y = 0

LHS $\overline{(X+Y)} = \overline{(0+0)} = \overline{(0)} = 1$

RHS X' . Y'

$= \bar{0} . \bar{0} = 1 . 1 = 1$

if X = 1 and Y = 1

LHS $\overline{(X+Y)} = \overline{(1+1)} = \overline{(1)} = 0$

RHS $\bar{X} . \bar{Y}$

$= \bar{1} . \bar{1} = 0 . 0 = 0$

b) 2nd theorem

$\overline{(X.Y)} = \bar{X} + \bar{Y}$

Proof :

if X = 0 and Y = 0

LHS $\overline{(X.Y)}$

$= \overline{(1.1)} = \overline{(1)} = 1$

RHS $\bar{X} + \bar{Y}$

$= 0' + 0' = 1 + 1 = 1$

if X = 1 and Y = 1

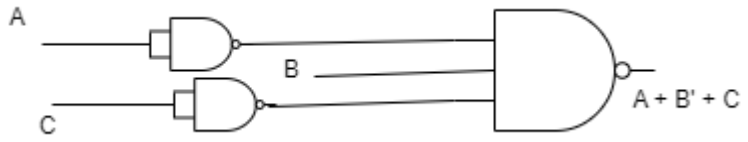
LHS $\overline{(X.Y)}$

$= \overline{(1.1)} = \overline{(1)} = 0$

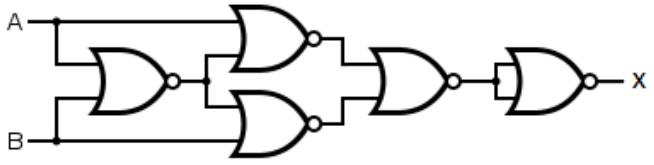
RHS $\bar{X} + \bar{Y}$

$= \bar{1} + \bar{1} = 0 + 0 = 0$

6. Design A + B' +C using 3 input and 2 input NAND gates (2)
Ans:



7. Design an XOR gate using a minimum number of NOR gates. (1)
Ans:



8. Simplify ABC + AB'C + ABC' using
    a. boolean laws
    b. using K-map.

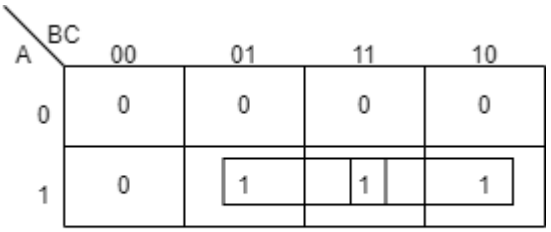
    Will the simplified expression be the same or different? (3)

    Ans:

    a.

    ABC + AB'C + ABC'
    = AC(B + B') + ABC'
    = AC + ABC'
    = A(C+ C'B)
    = A(C + B)
    = AB + AC

    b.

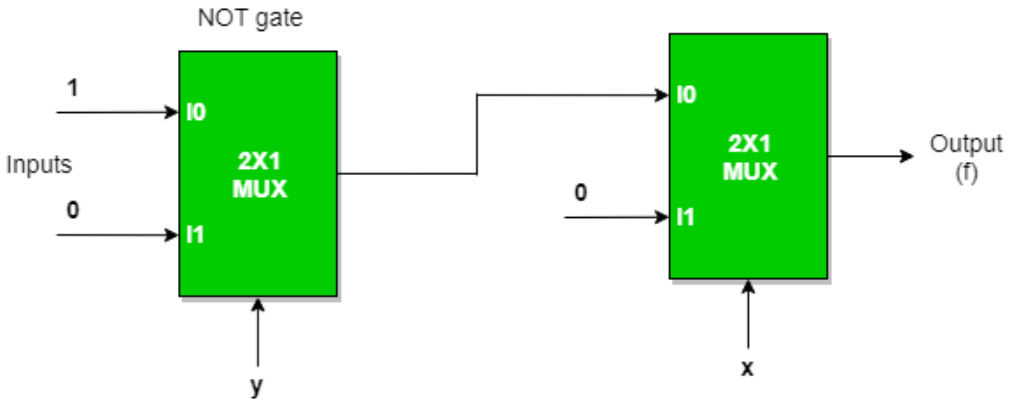


F = AB + AC

The simplified expressions will be same for both methods

9. Design a NOR gate using only MUX. (1)

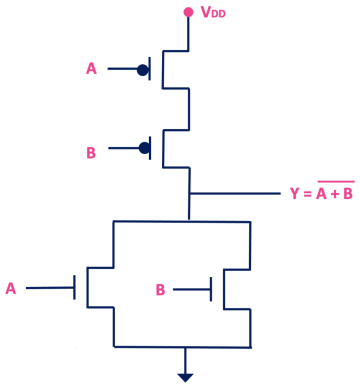
    Ans:



10. Provide CMOS representation of a NOR gate (2)

    Ans:

NOR Gate



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

11. How many select lines will there be for a 128x1 MUX? (1)

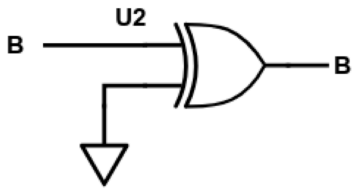
Ans:

7 select lines (2^n = number of inputs, where n is number of select lines)

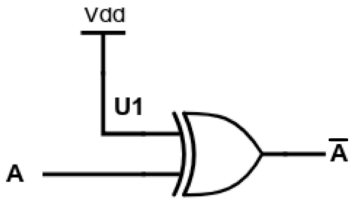
12. How can you make an XOR gate to (2)
    a. behave as a buffer?
    b. behave as an inverter?

Ans:

a.

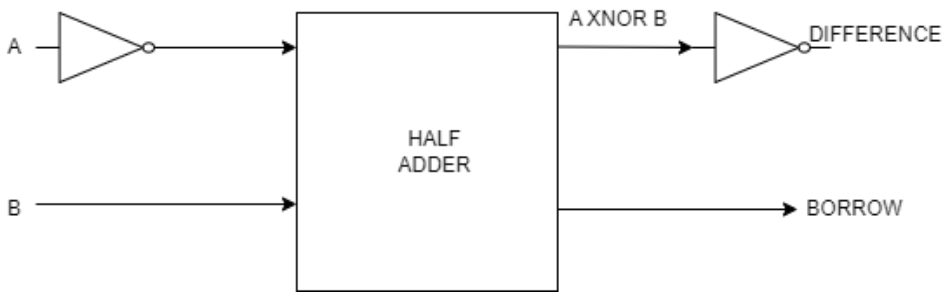


b.



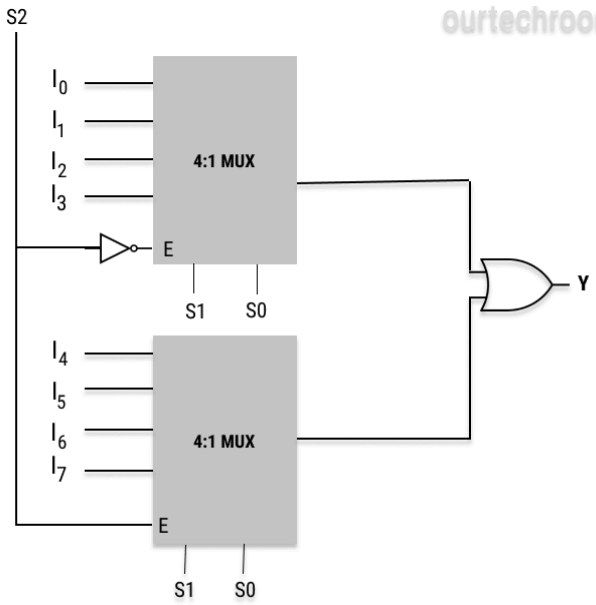
13. How will you obtain a Half subtractor using a Half adder block without modifying the internal circuit of the block? (2)

Ans:

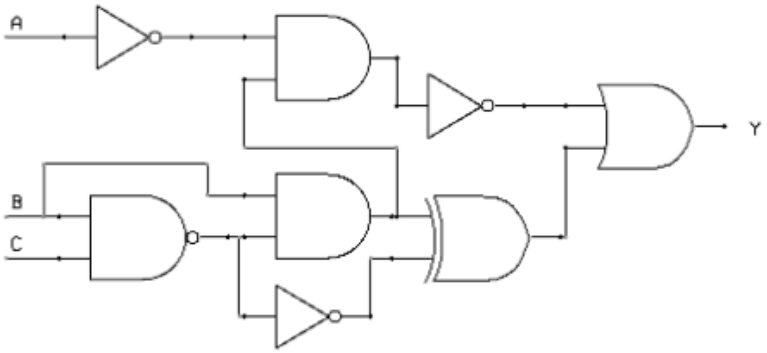


14. Design 8x1 MUX using only 4X1 MUX (3)

Ans:



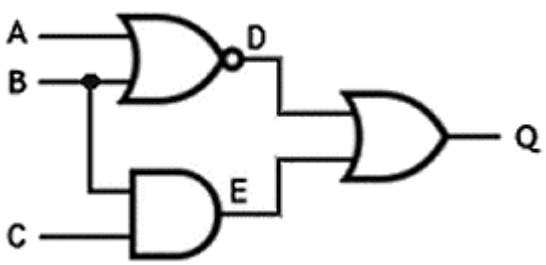
15. Obtain the simplified output expression for the below circuit. (3)



Ans:

(((BC)'B) XOR (BC)) + (A'(BC)'B)'
(((B'+C')B) XOR (BC)) + (A'(B'+C')B)'
(BC' XOR BC) + (A'BC')'
((BC')'BC + (BC)'(BC')) + A + B' + C
((B'+C)BC + (B'+C')(BC')) + A + B' + C
BC + BC' + A + B' + C
B + A + B' + C
=1

16. Find the output expression(Q), represent Q in canonical form and obtain the POS (2)

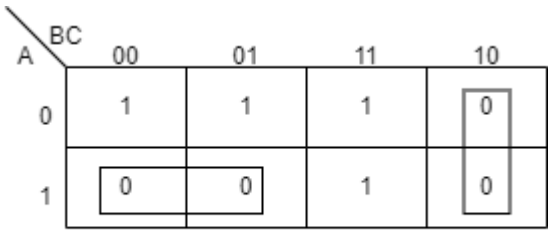


Ans:

(A+B)' + BC

A'B' + BC

A'B'C + A'B'C' + ABC + A'BC

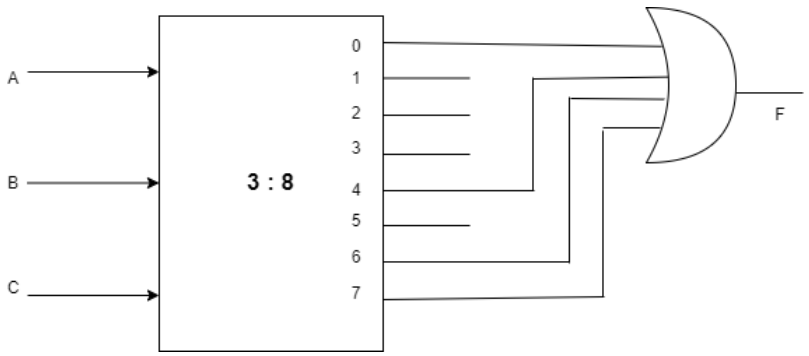


F=(A'+B) (B'+C)

17. Implement the following expression using a 3 to 8 Decoder

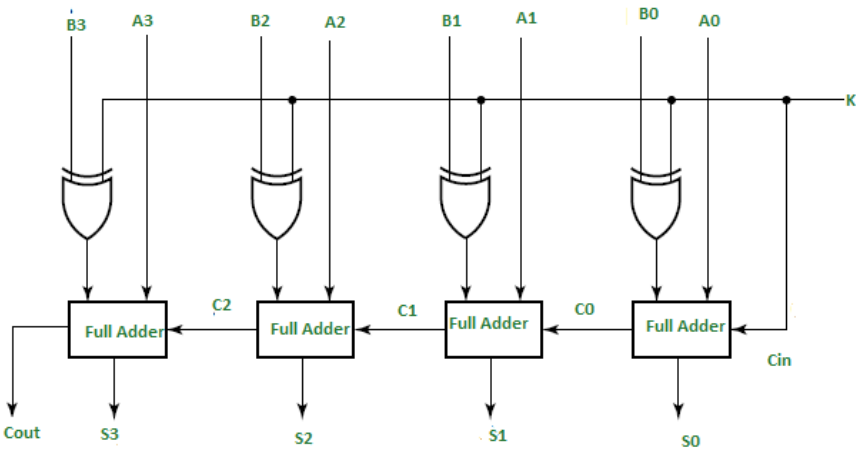
F = ∑m(0, 4, 6, 7) (2)

Ans:

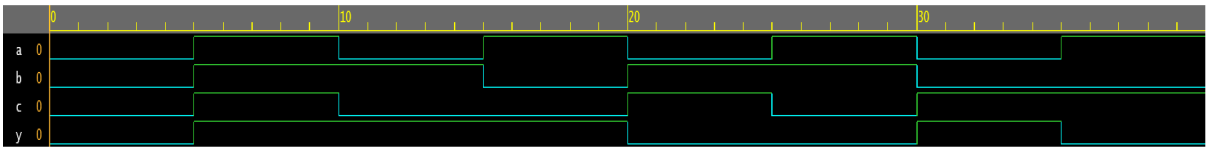


18. Design a 4 bit adder/subtractor(Block diagram). If Carry_in signal is 1, it should perform 4 bit subtraction and if it is 0, it should perform 4 bit addition (3)

Ans:

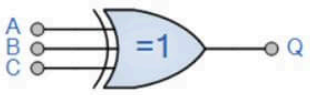


19. Write the truth table for below waveform(a, b, c are inputs and y is the output) and identify the circuit (2)



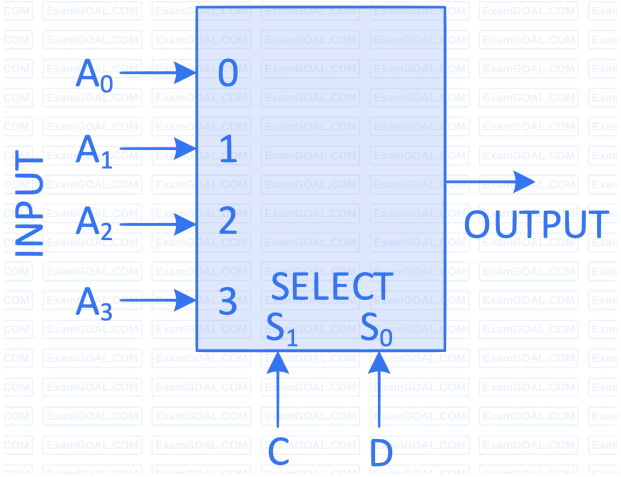
Ans:

Symbol	Truth Table			
	C	B	A	Q
	0	0	0	0
	0	0	1	1
	0	1	0	1
	0	1	1	0
	1	0	0	1
	1	0	1	0
	1	1	0	0
	1	1	1	1
Boolean Expression Q = A ⊕ B ⊕ C	"Any **ODD** Number of Inputs" gives Q			



3-input Ex-OR Gate

20. Consider the 2-bit multiplexer (MUX) shown in the figure. What should be the values for A0, A1, A2 and A3 for the OUTPUT to be the (2)
    a. XOR of C and D
    b. XNOR of C and D



Ans:

OUTPUT = C'D'A0 + C'DA1 + CD'A2 + CDA3

a. If A0 = 0, A1 = 1, A2 = 1, A3 = 0 then OUTPUT = C'D + CD' = C XOR D

b. If A0 = 1, A1 = 0, A2 = 0, A3 = 1 then OUTPUT = C'D' + CD = C XNOR D