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RTL Design & Integration – Skill training

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What is RTL?

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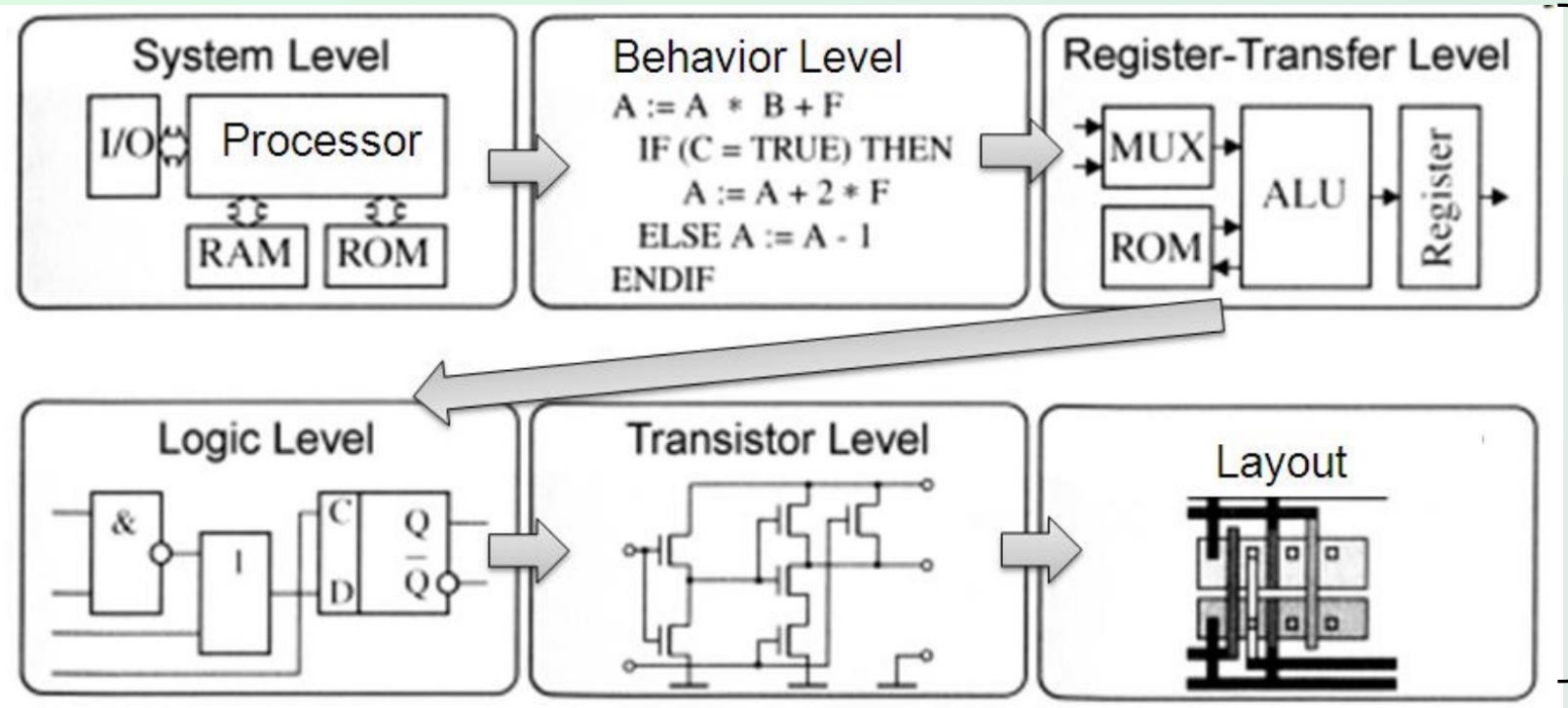
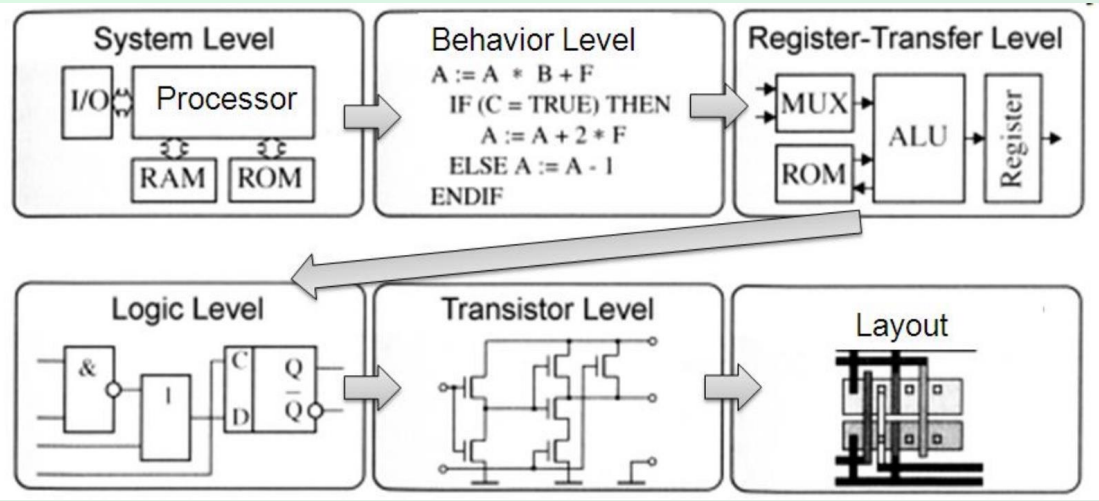


- The entire process is called **RTL design flow**.

- We want: Diagram of a system/circuit in paper => Layout in a chip

RTL design flow for FPGA/ASIC?



- FPGA – Field programable gate array
- ASIC – Application specific Integrated circuit

- **RTL design flow is of two types:**
  - **RTL flow for FPGA**
  - **RTL flow for ASIC**

Generalized RTL design flow for FPGA/ASIC

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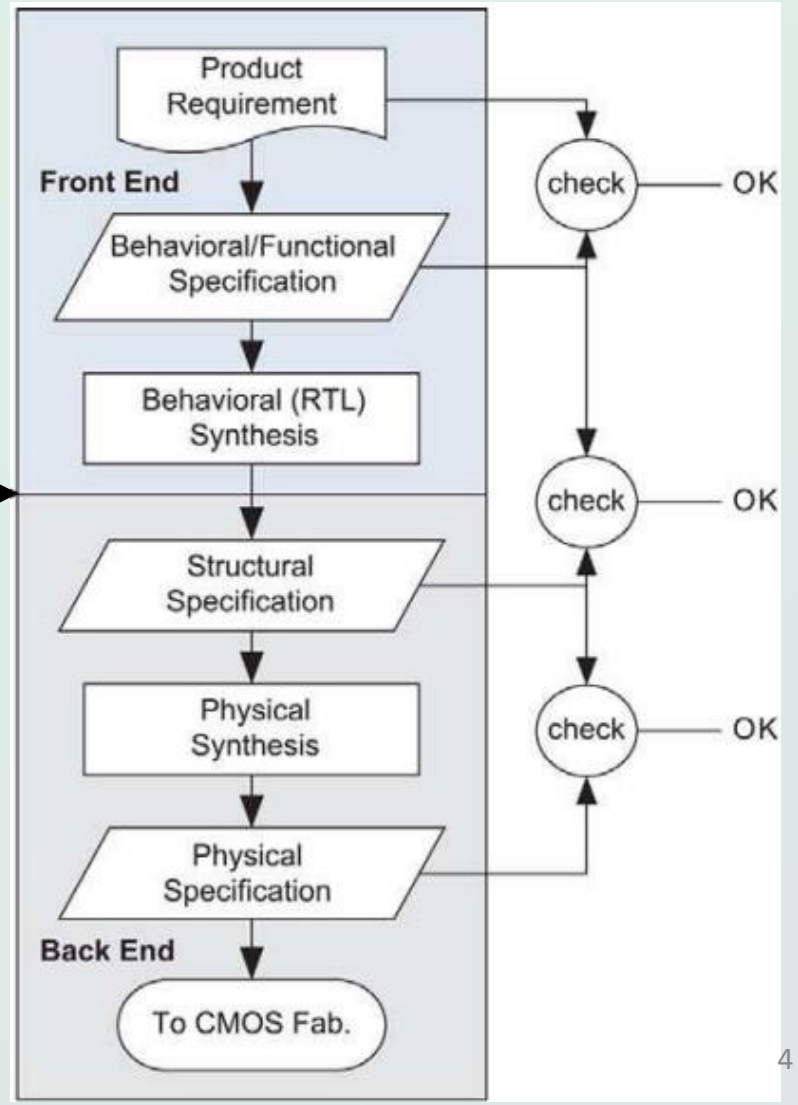
- High Level Design
  - Specification Capture
  - Design Capture in C, C++, SystemC or SystemVerilog
  - HW/SW partitioning and IP selection
- RTL Design
  - Verilog/VHDL
- System, Timing and Logic Verification
  - Is the logic working correctly?
- Physical Design
  - Floor planning, Place and Route, Clock insertion
- Performance and Manufacturability Verification
  - Extraction of Physical View
  - Verification of timing and signal integrity
  - Design Rule Checking/ LVS



RTL design flow for FPGA and ASIC

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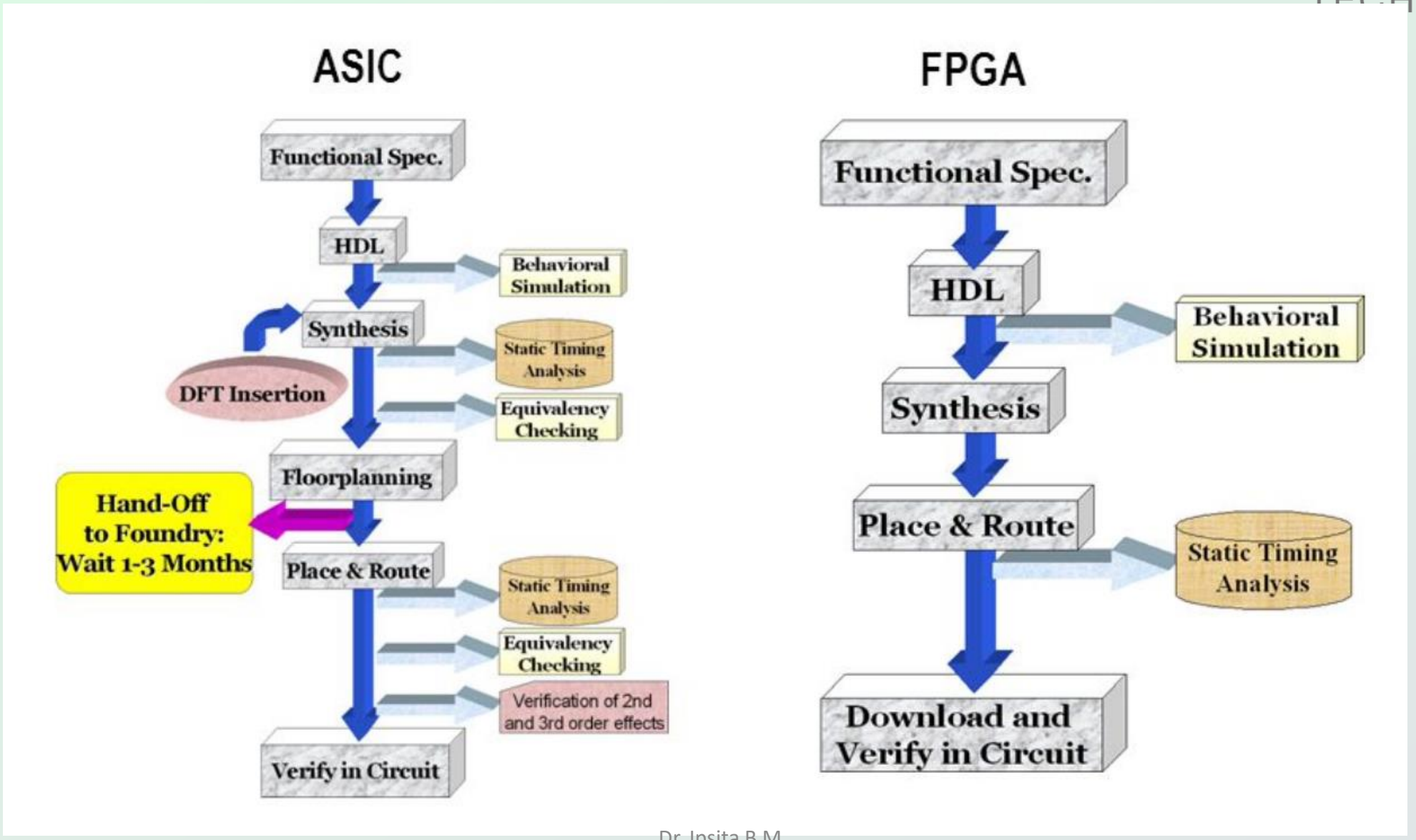

RTL design process

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- Functional Specification: Involves determining the desired functionality, performance targets like power consumption limits, and other constraints.
- HDL/Design entry: Designer creates a high-level description of the desired functionality using a HDL, such as VHDL or Verilog. This HDL code describes the behavior of the digital circuit to be implemented.
- Behavioral simulation: This stage involves simulating the RTL design using test vectors and checking for correct functionality.
- Synthesis: We convert the Verilog code to a gate-level netlist, which represents the circuit in terms of logic gates and flip-flops.
- Floor planning: This step controls how logic is placed in the die (FPGA/ASIC).
- Place & Route: This process assigns the synthesized logic elements to specific locations on the FPGA/ASIC and determines the routing of the interconnect wires connecting them.
- Static Timing Analysis: Static Timing Analysis (STA) of the design finds the potential timing issue that later causes the design’s metastability and negative slack.

RTL design process

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- DFT (Design for Test): Logic to test a design's functionality, after the chip is fabricated.
  - ✓ consists of logic and memory BIST (built-in-self-test), scan logic and Boundary Scan logic (JTAG) etc.
- Equivalence checking: LEC is an Equivalence Checker. LEC verifies that the design function has not changed over -

  RTL to RTL, RTL to Gate, Gate to Gate

RTL design process – Tools used

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- Modelling and Simulation
  - Questa ADMS = Questa+Modelsim+Eldo+ADiT (Mentor Graphics)
  - Verilog-XL, NC_Verilog, Spectre (Cadence)
- Design Synthesis (digital)
  - Leonardo Spectrum (Mentor Graphics)
  - Design Compiler (Synopsys), RTL Compiler (Cadence)
- Design for Test and Automatic Test Pattern Generation
  - Tessent DFT Advisor, Fastscan, SoCScan (Mentor Graphics)
- Schematic Capture & Design Integration
  - Pyxis Design Architect-IC (Mentor Graphics)
  - Design Framework II (DFII) - Composer (Cadence)
- Physical Layout
  - Pyxis IC Station (Mentor Graphics)
  - SOC Encounter, Virtuoso (Cadence)
- Design Verification
  - Calibre DRC, LVS, PEX (Mentor Graphics)
  - Diva, Assura (Cadence)

RTL Integration flow

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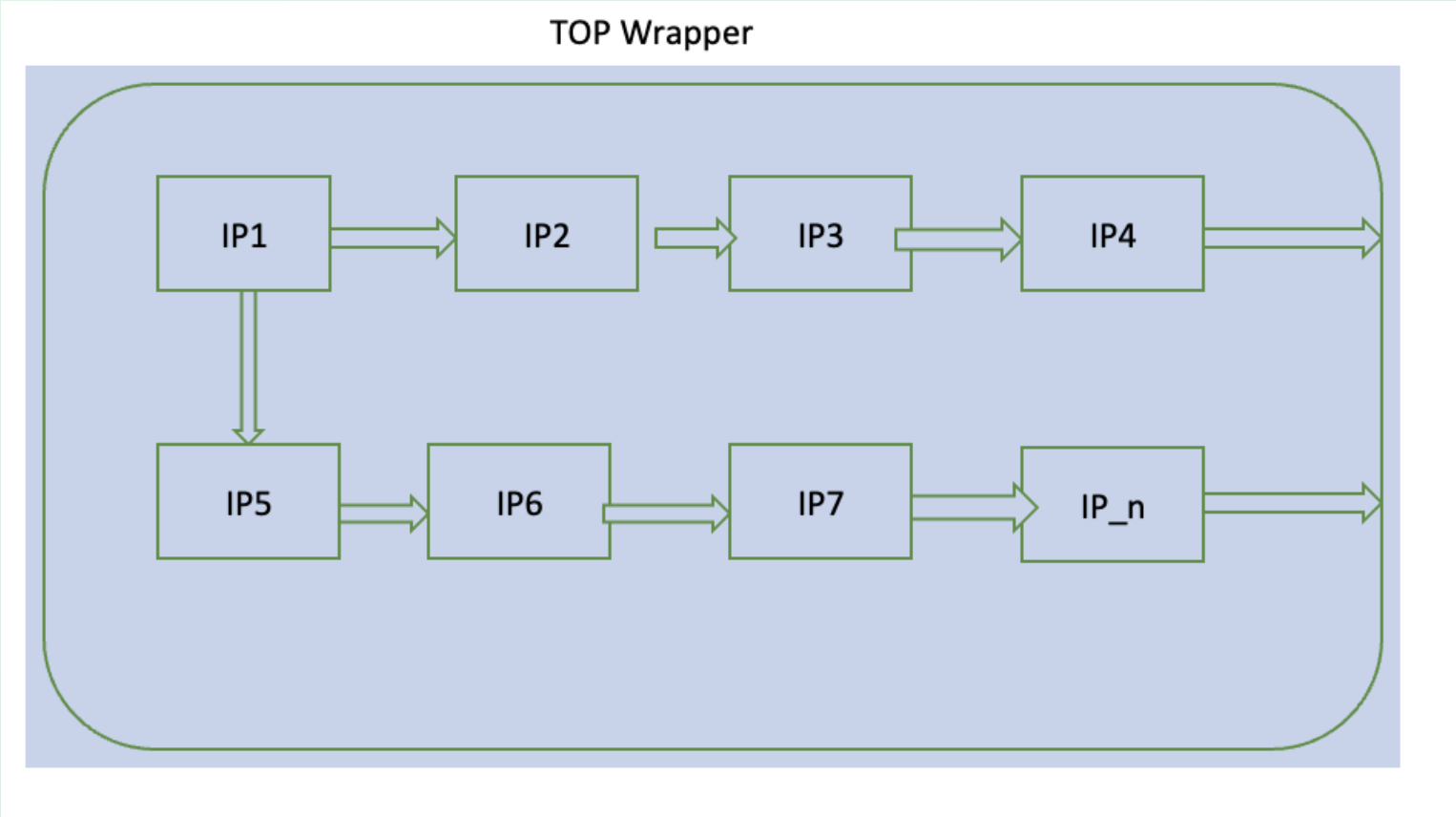
- The process of integrating the individual IPs into top-level hierarchy architecture is called RTL integration in SOC.

- We connect all the ports from one module to another module, and this port connection goes up to the top level, where it can be either an output or an input as per our design requirements.



RTL Integration flow – steps

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- 1st step – RTL integration; here we connect various blocks through port connections.
- 2nd step – Linting
- 3rd step – CDC
- 4th step – UPF
- 5th step – SDC
- 6th step – RTL synthesis
- 7th step – STA
- 8th step – LEC
- 9th step – FECO

RTL integration steps

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- Linting – Compiler does not check code correctness. Linting tools are used for static verification of code.
  - Here, we do not apply input to the design & check the output.
  - Rather, Linting tools checks whether the code conforms to the basic guidelines and the initial design requirements.
- CDC (Clock Domain Crossing) – Signal crosses from one domain to another creating CDC. This can create metastability. So, we need to check for clock domain synchronization – CDC is used for this.
- UPF (Unified Power Format) – Involves developing a syntax where we define the power intent of the design. UPF file tells how to define a level shifter at a specific point of the design; how to indicate there is an isolation cell at a specific point; how to define clock gating cells.
- SDC (Synopsys Design Constraint): This file contains the timing intent of the design. Tells us what timing constraints we need to meet to close a design at a specific frequency.
- RTL Synthesis – Process of getting optimized netlist from a given RTL. Is design code synthesizable? – this is checked during Linting.

RTL integration steps

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- LEC (Logic Equivalence Check) – Checks if RTL & Gate level netlist intent is matching.
  - Optimization technique used – input to LEC tool.
- STA (Static Timing Analysis) – Verify the timing sign off. There should not be any setup & hold violation in the netlist.
- FECO (Functional Engineering Change Order) – During the entire verification process, if any design bug is found in the gate level netlist, it is not preferred to start from RTL design level. Rather bugs are implemented as Functional ECOs at gate level netlist.
  - It ensures we meet the project timelines.
- ECO is of two types:
  - Functional ECO – as part of RTL integration process, we mostly deal with FECO
  - Timing ECO

EDA tools used in RTL integration

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- RTL integration

  Core tools – Core builder, Core assembler
- Linting – Spyglass Lint
- CDC – Spyglass CDC
- RTL synthesis – Design Compiler
- Low power UPF – VCLP/SGLP
- STA – Primetime
- LEC – Formality
- FECO

  Design compiler & Formality

  Do updates in both RTL & GLS; use LEC to validate
- Companies build wrappers on top of EDA tools for automating integration flow.

Thank you

Thank You