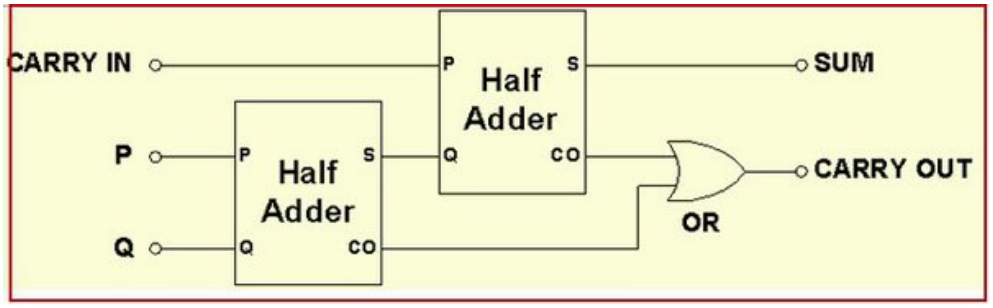
Combinational Assignment – III

1. What is a latch?
   Latch is an electronic device, which changes its output immediately based on the applied input. It is used to store either 1 or 0 at any specified time. It consists of two inputs namely “SET” and RESET and two outputs, which are complement to each other.

2. What is the input and output of a half adder?
   Half adder consists of 2 bits input and sum and carryout.

3. Draw the circuit for a full adder using two half adders.



4. What is the input and output of a full adder?
   2 signals of 1 bit and carry_in as inputs and,1 bit sum and 1 bit carry_out as outputs

5. In a full adder, the sum is obtained as the output of an XOR gate. Show how.

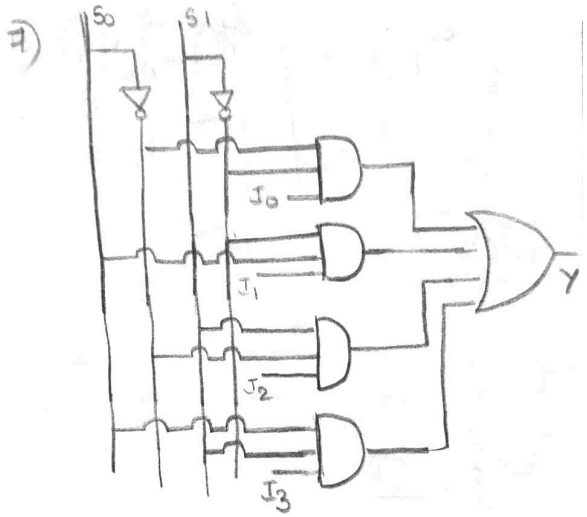
Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

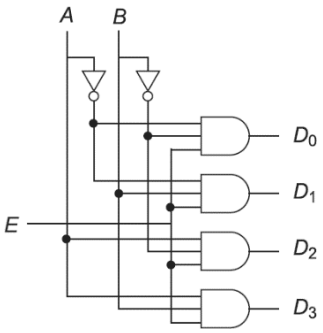
A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

SUM = $A \oplus B \oplus C$

6. Why are universal gates preferred for making flip-flops?
   Universal gates can be used to create all other types of logic gates. This allows for simpler circuit designs and reduces overall complexity of flip flop.

7. Implement the 4:1 multiplexer using basic gates.





8. For the de-multiplexer of above Fig., 'E' is held at 1. Prepare a truth table linking AB to output. Is it a decoder. If E = 0, what would be the outputs? Are these dependent on A, B?

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A	B	E	D_0	D_1	D_2	D_3
0	0	1	1	0	0	0
0	1	1	0	1	0	0
t	0	1	0	0	1	0
1	1	1	0	0	0	1

$D_0 = \bar{A}\bar{B}E$
$D_1 = \bar{A}BE$
$D_2 = A\bar{B}E$
$D_3 = ABE$

Yes, it is a decoder

A	B	E	D_0	D_1	D_2	D_3
0	0	0	0	0	0	0
0	1	0	0	0	0	0
1	0	0	0	0	0	0
1	1	0	0	0	0	0

They are not dependent on AB

i.e

A	B	E	D_0	D_1	D_2	D_3
x	x	0	0	0	0	0

9. For the multiplexer of Fig. 4, prepare the truth table for AB and F. Write the logic expression for F for input (0, 1).

Hint:

$F = A, BI_2 = \bar{A}BC$

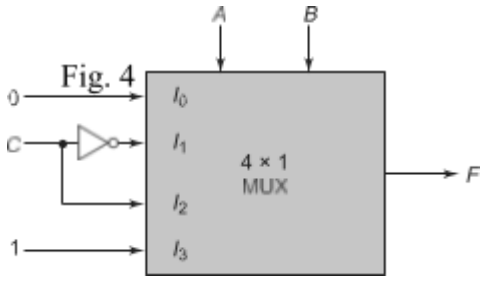


Fig. 4

9). Truth Table

A	B	F
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$F = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$

$F = \bar{A}B\bar{C} + A\bar{B}C + AB$

If input $C = 0$,

then $F = \bar{A}B + AB$

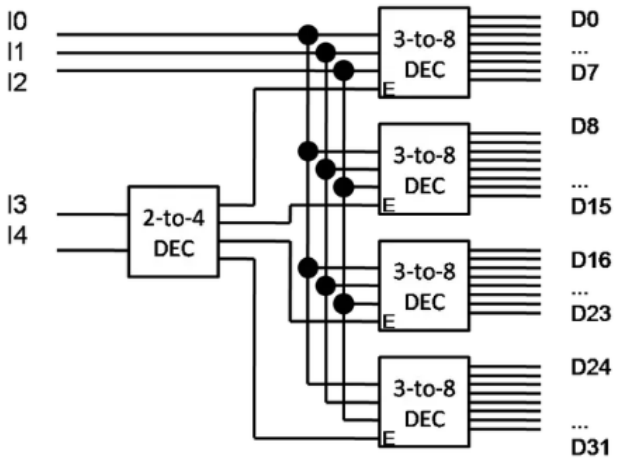
$F = \underline{B}$

If input $C = 1$,

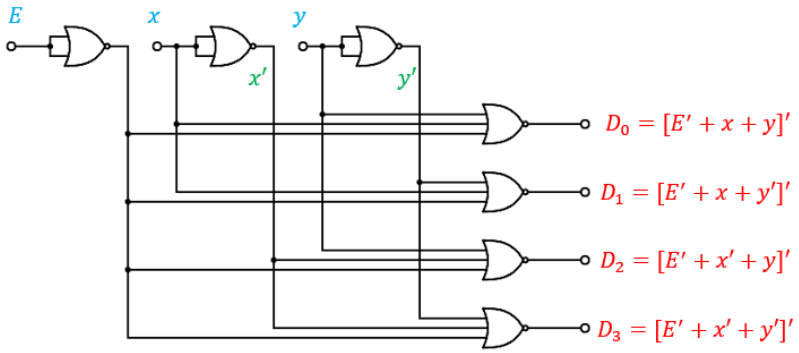
then $F = A\bar{B} + AB$

$= \underline{A}$

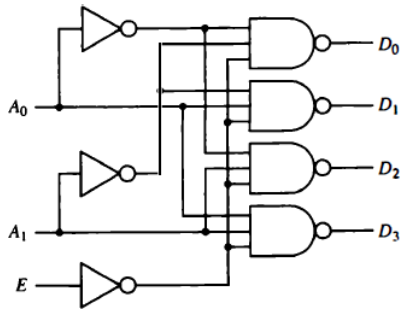
10. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and one 2-to+line decoder.

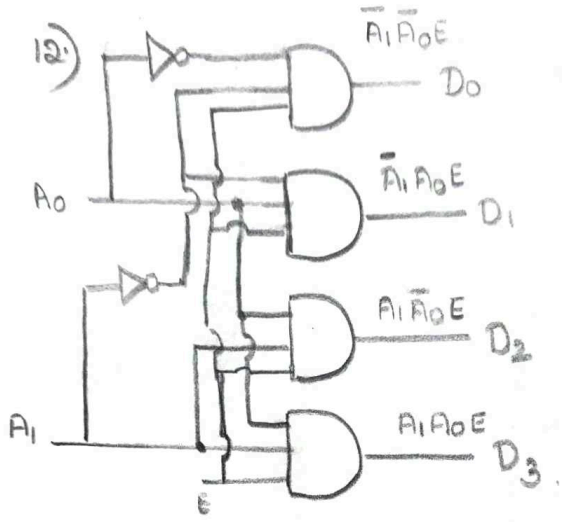


11. Draw the logic diagram of a 2-to-4-line decoder with only NOR gates. Include an enable input.



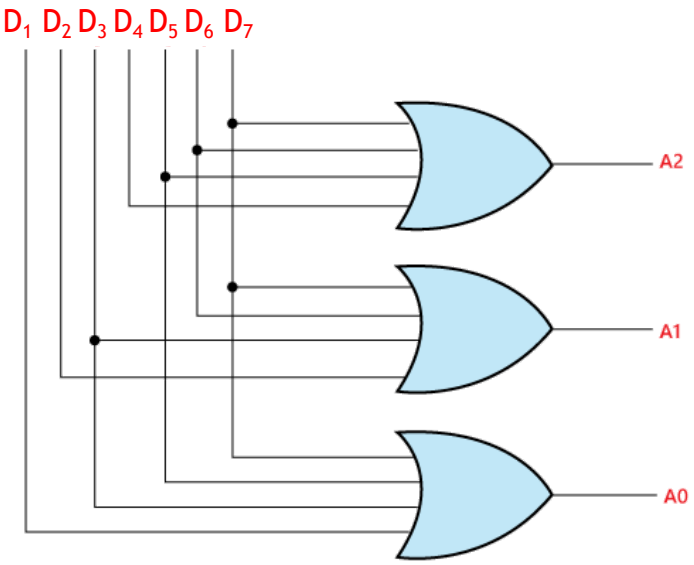
12. Modify the decoder of below Fig. so that the circuit is enabled when E = 1 and disabled when E = 0. List the modified truth table.





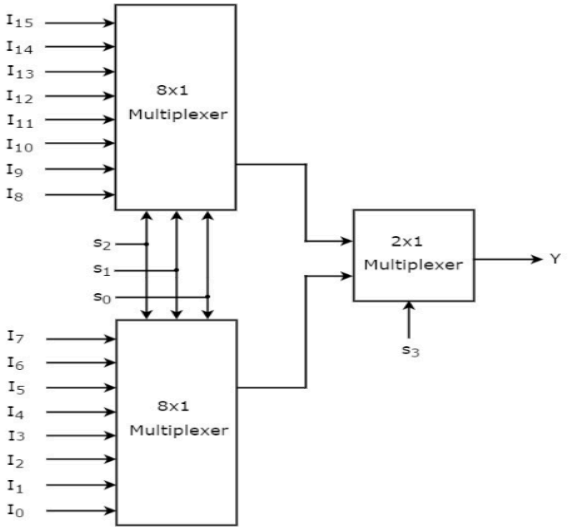
13. Draw the logic diagram of an eight-input, three-output encoder whose truth table is given below. What is the output when all the inputs are equal to 0? What is the output when only input Do is equal to 0? Establish a procedure that will distinguish between these two cases.

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1



When all the inputs are equal to A_O, A_1, A_2 will be 0
D_0 does not affect the outputs so the value of D_0 is invalid for output.

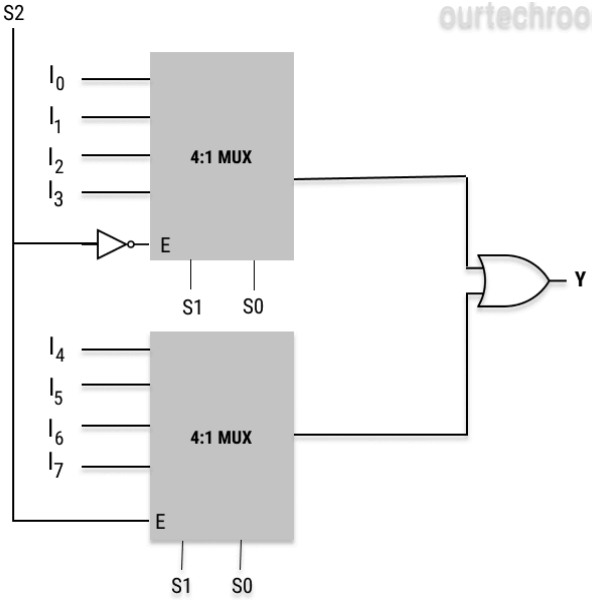
14. Construct a 16-to-1 line multiplexer with two 8-to-1 line multiplexers and one 2·to 1 line multiplexer. Use block diagrams for the three multiplexers.



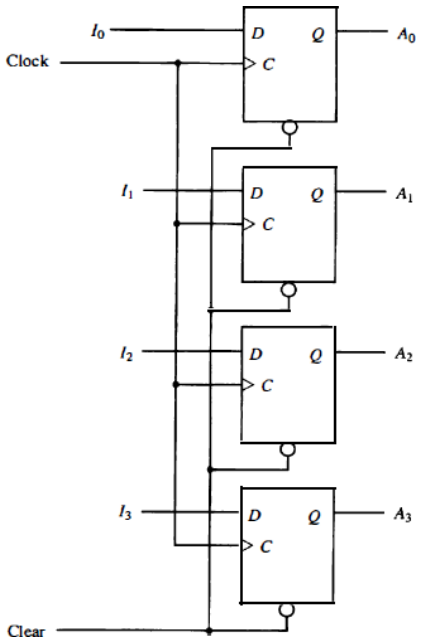
15. Draw the block diagram of a dual 4-to·1·line multiplexers and explain its operation by means of a function table.

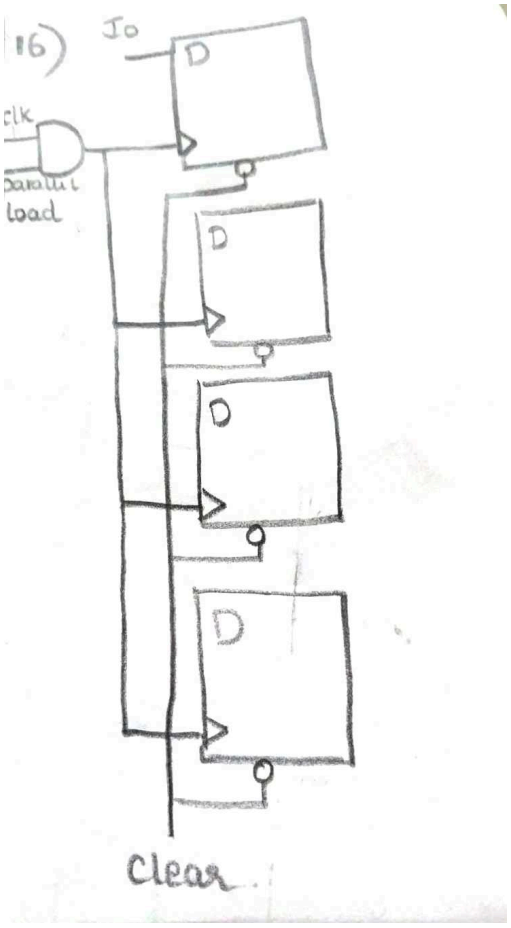
4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0, two selection lines s_1 & s_0 and one output Y. One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines

Dual 4x1 mux will behave as a 8x1 mux



16. Include a two-input AND gate with the register of Fig. 2·6 and connect the gate output to the clock inputs of all the flip-flops. One input of the AND gate receives the clock pulses from the clock pulse genera tor. The other input of the AND gate provides a parallel load control. Explain the operation of the modified register.





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During posedge clk and parallel load high, I0, I1, I2, I3 will be loaded to A0, A1, A2, A3 respectively and behaves like a PIPO. Clear is active low. Upon assertion of clear signal all the outputs will be reset.

17. The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?

1st shift —> O/P= 1, Content of register 1101

2nd shift —> O/P= 01, Content of register 1110

3rd shift —> O/P= 101, Content of register 0111

4th shift —> O/P= 1101, Content of register 1011

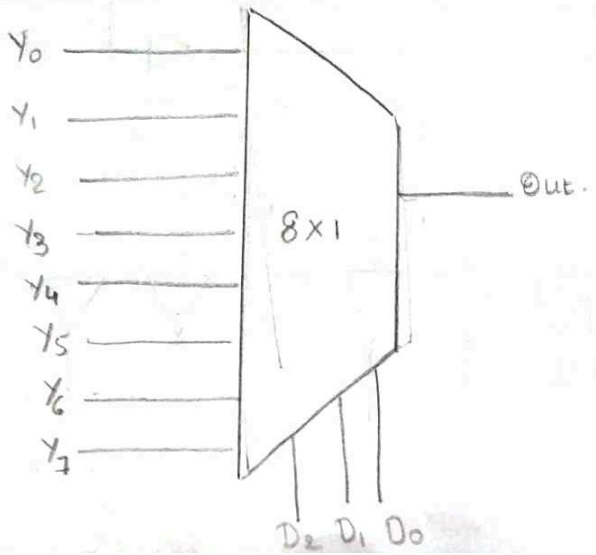
5th shift —> O/P= 11101, Content of register 1101

6th shift —> O/P= 011101, Content of register 0110

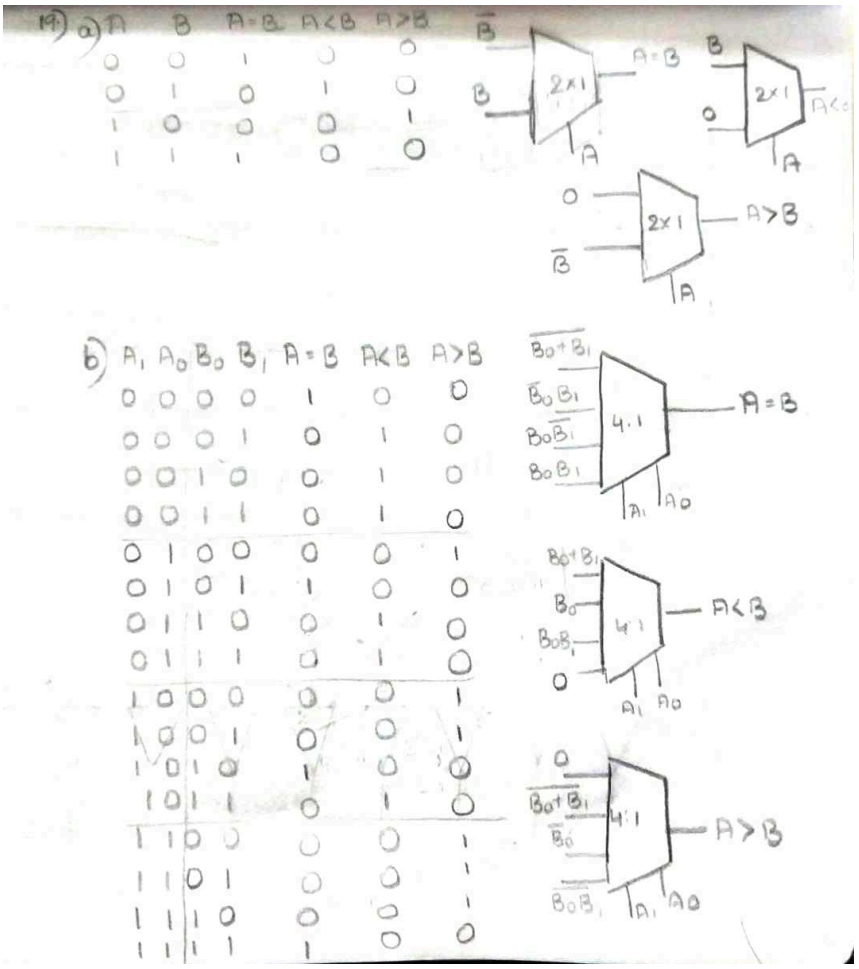
18. Realise a 3:8 Decoder using any Mux?

18.)

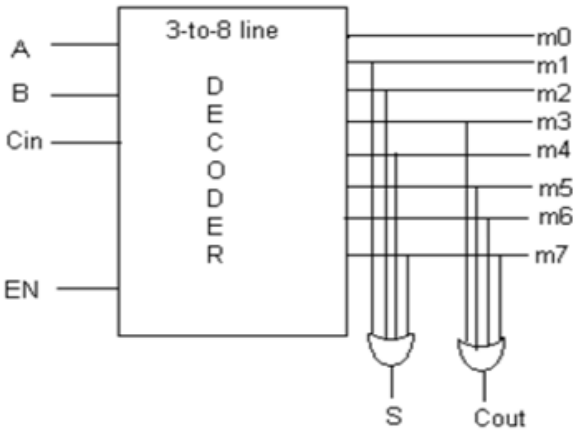
D_2	D_1	D_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

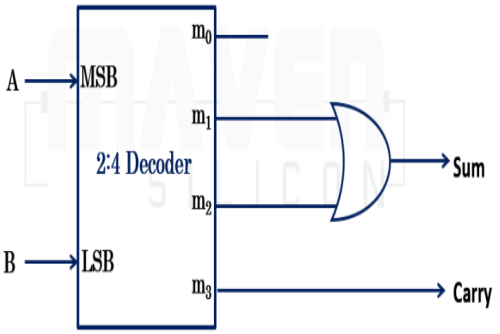


19. Realise an 1-bit and 2-bit comparator using any Mux?



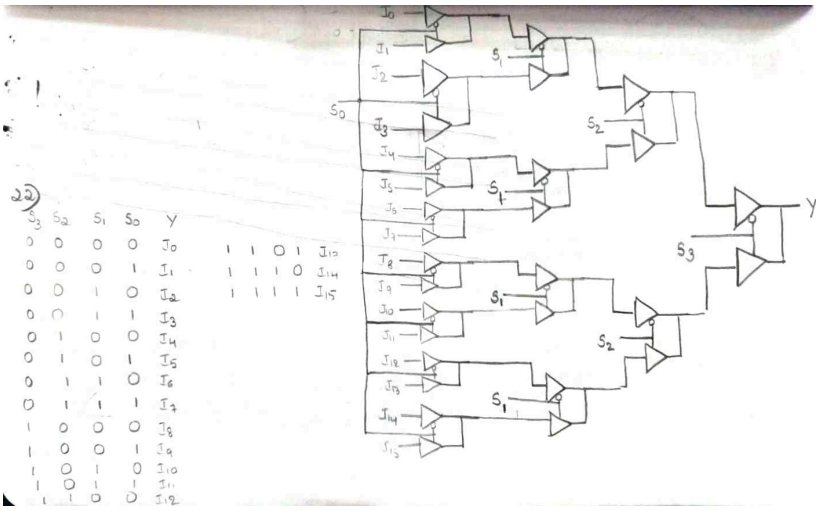
20. Realise a Full-adder and Half-adder using any decoder?



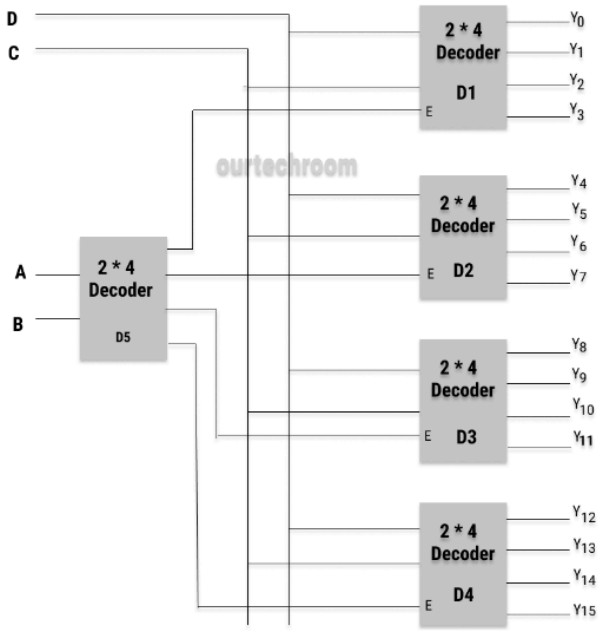


21. Implement a 16x4 encoder using 2-to-1 encoders?

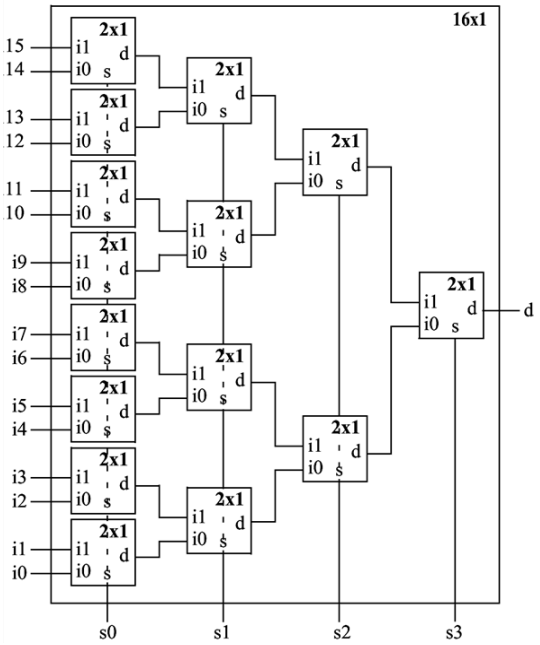
22. Implement a 16:1 Mux using tri-state buffers?



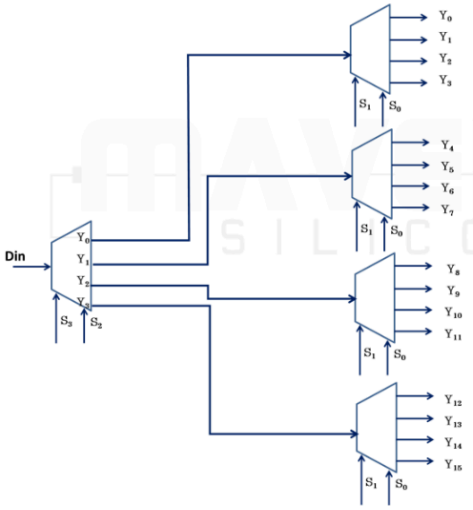
23. Implement a 4-to-16 decoder using 2-to-4 decoder?



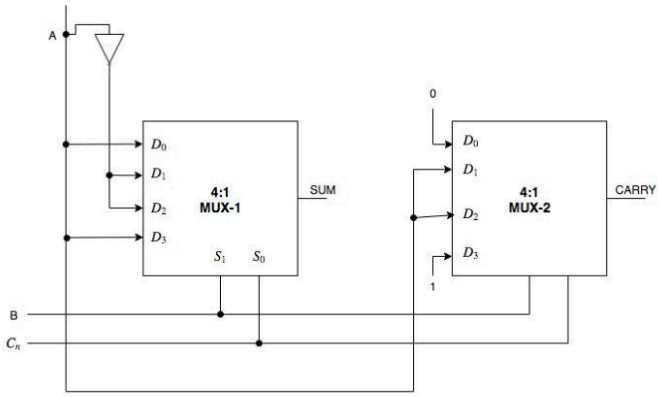
24. Implement a 16:1 Mux using 2:1 Mux?



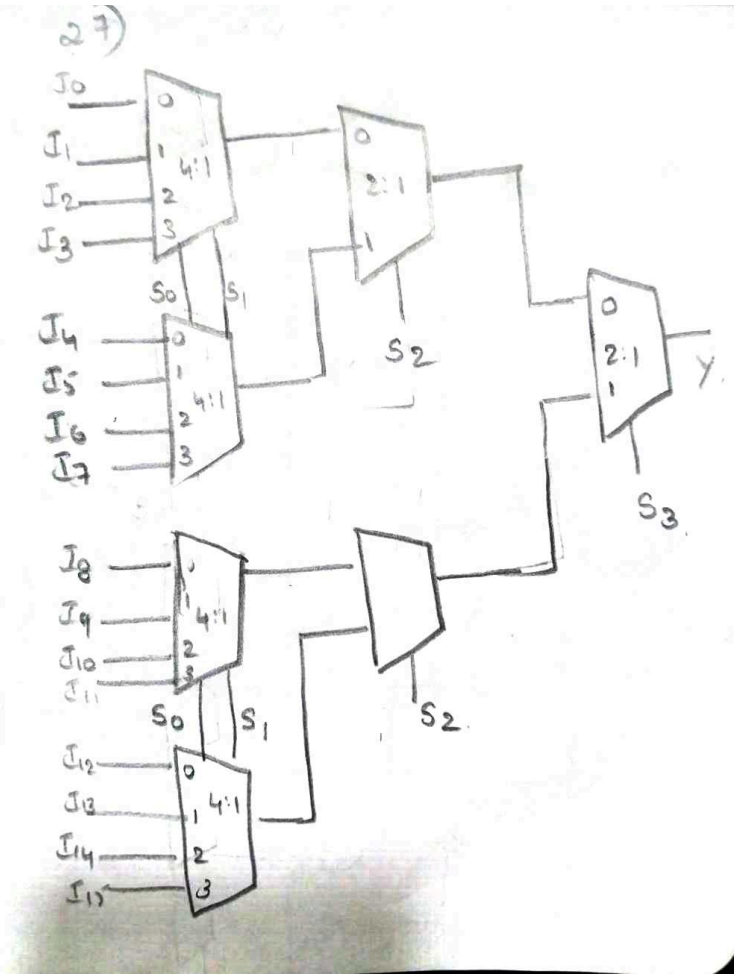
25. Implement a 1:16 demux using 1:2 de-mux?



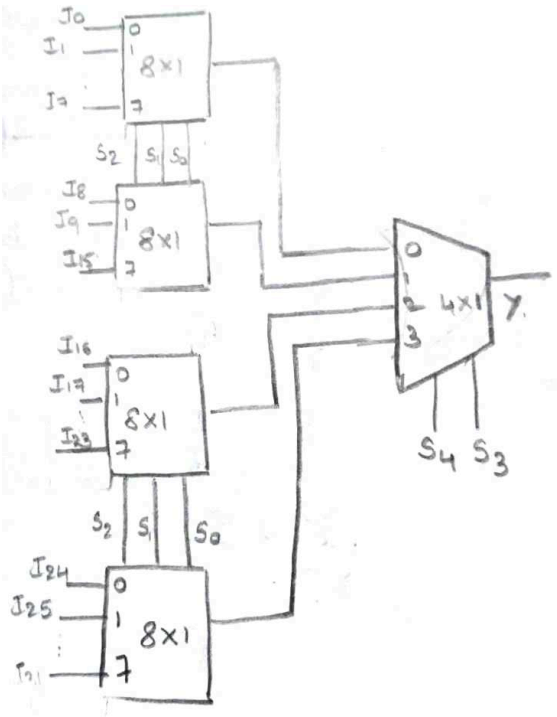
26. Implement a full-adder using 4x1 Mux?



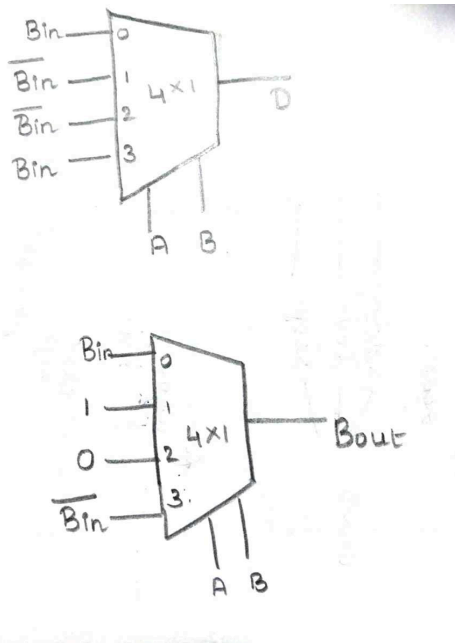
27. Implement 16x1 Mux using 4x1 and 2x1 Mux?



28. Implement 32x1 Mux using 8x1 and 4x1 Mux?



29. Implement full-subtractor using 4x1 Mux?



30. Implement full-adder using 2x1 Mux only?