Sequential circuits - Latches and Flip Flops
Assignment - 6

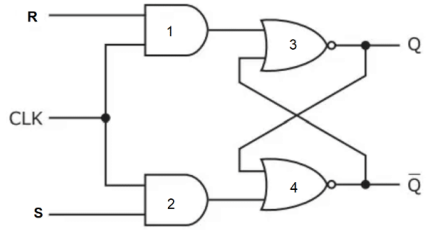
1. **How does a sequential circuit differ from a combinational circuit?**
   Combinational Circuit –
   Ans:
   Combinational circuit:
   In this output depends only upon present input.
   Speed is fast.
   It is designed easy.
   There is no feedback between input and output.
   This is time independent.
   Elementary building blocks: Logic gates
   Used for arithmetic as well as boolean operations.
   Combinational circuits don't have capability to store any state.
   As combinational circuits don't have clock, they don't require triggering.
   These circuits do not have any memory element.
   It is easy to use and handle.

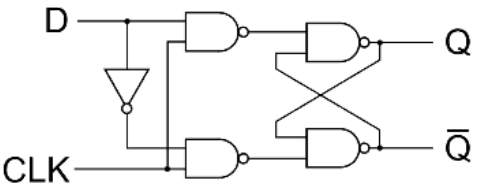
   Sequential Circuit –

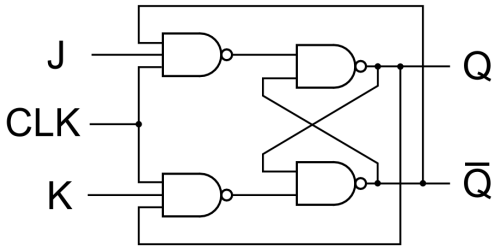
   In this output depends upon present as well as past input.
   Speed is slow.
   It is designed tough as compared to combinational circuits.
   There exists a feedback path between input and output.
   This is time dependent.
   Elementary building blocks: Flip-flops
   Mainly used for storing data.
   Sequential circuits have capability to store any state or to retain earlier state.
   As sequential circuits are clock dependent they need triggering.
   These circuits have memory element.
   It is not easy to use and handle.

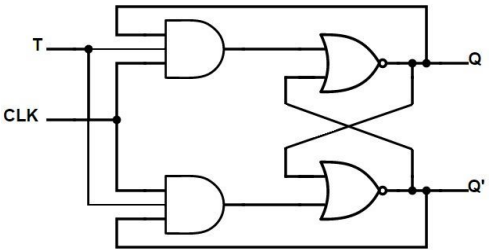
2. **Explain the term edge triggering.**
   Ans:
   Edge triggering is when the flip-flop state is changed as the rising or falling edge of a clock signal passes through a threshold voltage

3. **Draw and explain with excitation table of RS, JK, D and T flip-flop.**
   Ans:









SR Flip-flop			
Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop			
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

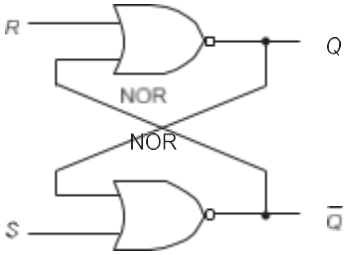
During clock edge, when S = 1 Output will be set, when R = 1 output will be reset. When both inputs are 1, the output will be unknown or invalid.

During clock edge, Output will get the value of D.

During clock edge, when J = 1 Output will be set, when K = 1 output will be reset. When both inputs are 1 the output will be toggled.

During clock edge, when input T is 1, output will toggle, else the output will hold previous value.

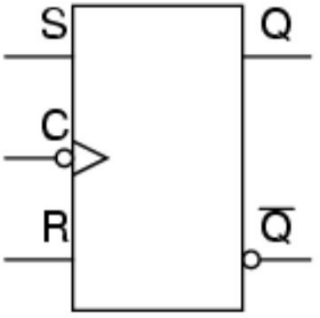
4. Identify the flip-flop of Fig.
   (a) If Q = 1, what are R and S?
   (b) if S = 1 and Q = 0, what is R?
   (c) S = 0, R = 1, what is Q?



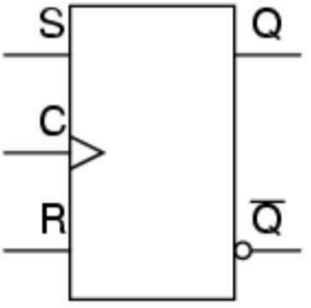
Ans:

a. R = 0, S = 1
b. R = 1
c. Q = 0

5. Draw the symbols of RS flip-flop for various types of triggering.
   Ans:
   Negative edge triggering

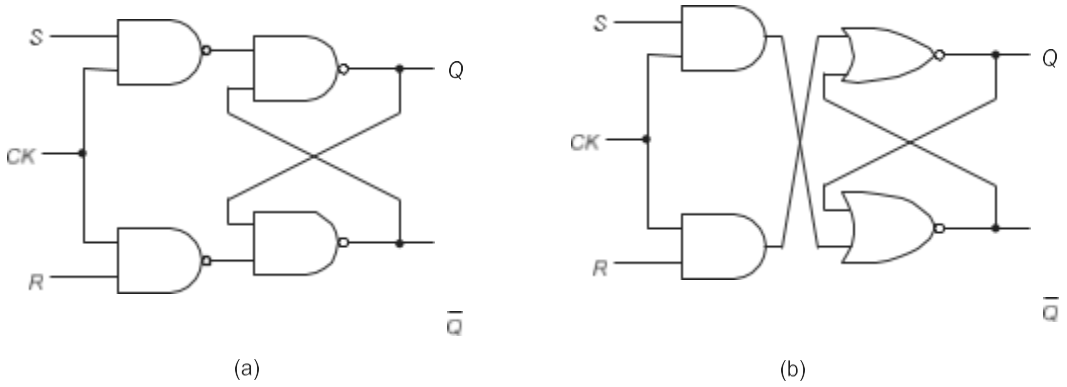


   Positive edge triggering



6. Why is an edge triggered flip-flop preferred over one with a clocked angle gate? (Skip)

7. Establish the equivalence of the given flip-flop. What happens when the clock is low?



Ans:

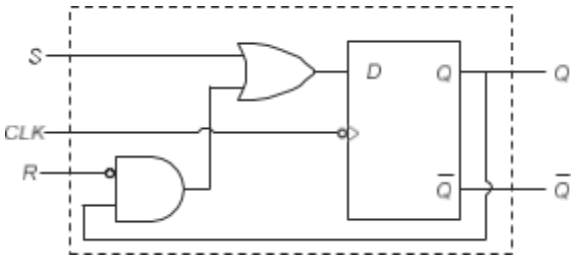
Case 1: a) Lets say, S = 0 and R = 0, then output of both NAND gates will be 1 and the value of Q and Q' will be same as their previous value, i.e, Hold state.
b)Let's say, S=0 and R=0, then output of both AND gates will be 0 and the value of Q and Q' will be same as their previous value, i.e, Hold state.

Case 2:a) Let's say, S=0 and R=1, then output of first NAND gates will be 1 and 0, correspondingly the value of Q' will be 1 as one of input is 0,hence Q' gets 1 value, similarly Q will be 0.
b)Let's say, S=0 and R=1, then output of both AND gates will be 1 and 0, correspondingly the value of Q will be 0 as one of input is 1 and it is a NOR gate so it will ultimately gives 0, hence Q gets 0 value, similarly Q' will be 1.

Case 3: a)Let's say, S=1 and R=0, then output of both NAND gates will be 0 and 1, correspondingly the value of Q will be 1 as one of input to NAND gate is 0, so output will be 1 hence Q' will become 0.
b) Let's say, S=1 and R=0, then output of both AND gates will be 0 and 1, correspondingly the value of Q' will be 0 as one of input to NOR gate is 1, so output will be 0 ultimately and this 0 value will go as input to upper NOR gate, and hence Q will become 1.

Case 4: a)Let's say, S=1 and R=1, then output of both NAND gates will be 0 and 0 which is invalid, as the outputs should be complement of each other.
b)Let's say, S=1 and R=1, then output of both AND gates will be 1 and 1 which is invalid, as the outputs should be complement of each other.

8. Show that the D flip-flop excitation table connected as in Fig. acts as an RS flip-flop.
   Hint: A bubble at the input of the AND gate is the symbol of the inverter.



Ans:

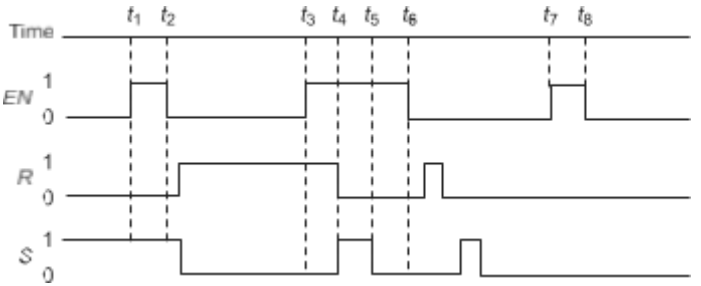
If S = 0 and R = 0, It'll hold the previous state. i.e., if Q = 0, then AND gate output will be 1 else 0.

If S = 0 and R = 1, Output Q will be 0 as OR gate output will be 0.

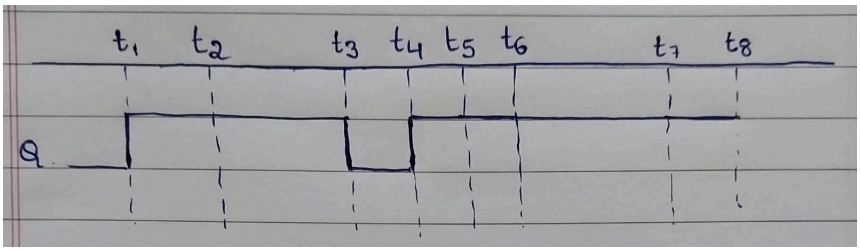
If S = 1, R = 0, Output of OR gate will be 1 and Q will be 1.

(1,1) is an exception

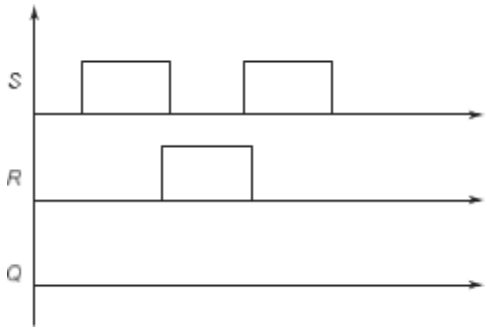
9. Figure shows the input waveform R, S, and EN applied to a clocked RS flip-flop. Below these waveforms, draw the timed output Q waveform.



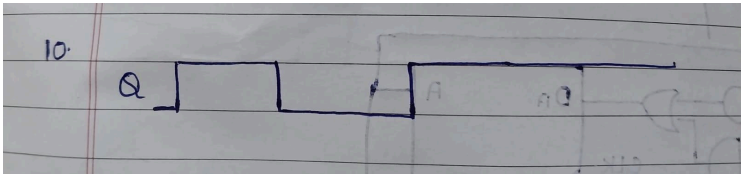
Ans:



10. Draw the output waveform for the following waveform input to the SR flip-flop.



Ans:



11. In an SR flip-flop, S is connected to R through a NOT gate input (1/0) given to S. Using the truth table, show that it acts as D flip-flop. Identify the output terminal.

Ans:

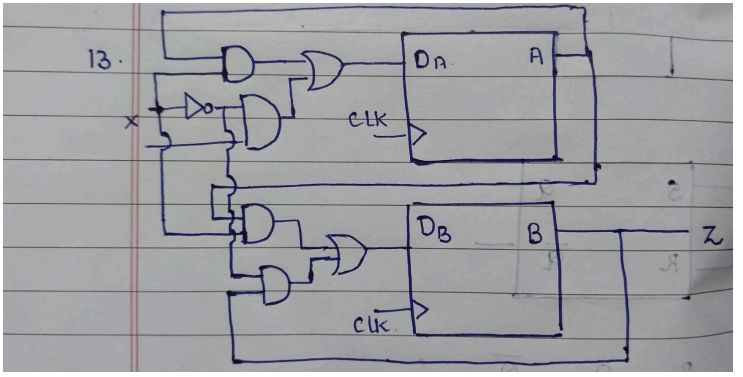
S	R	Q	Q’
0	1	0	1
1	0	1	0

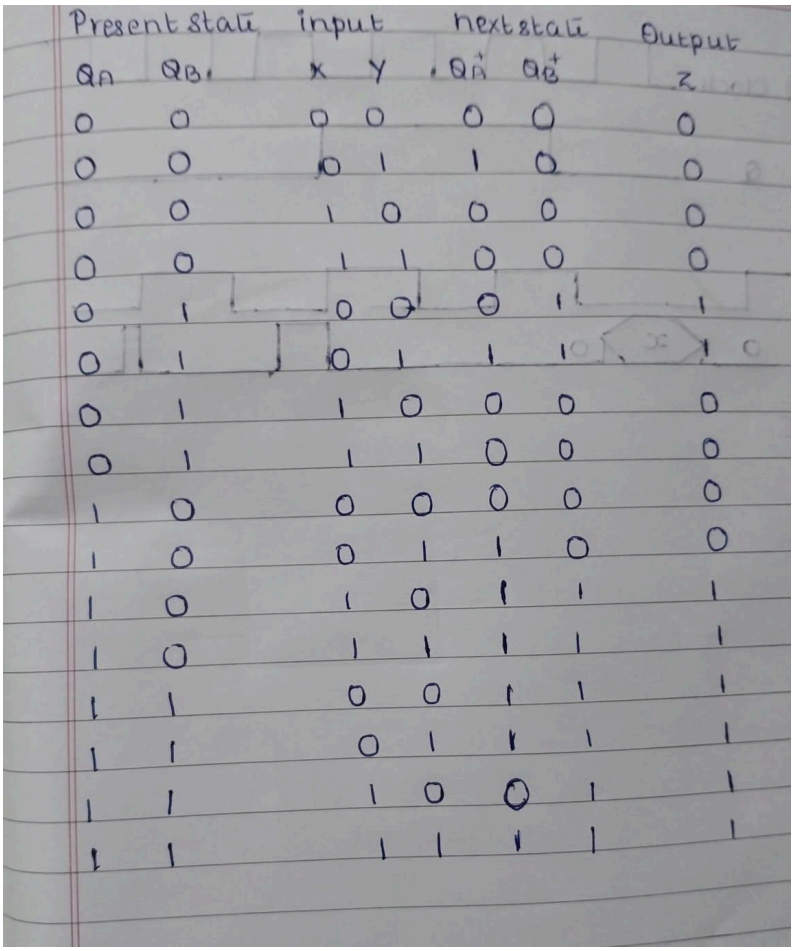
12. Show that a JK flip-flop can be converted to a D flip-flop with an inverter between the J and K inputs.
Ans:

J	K	Q	Q’
0	1	0	1
1	0	1	0

13. A sequential circuit has two D flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and the circuit output are as follows:
DA = x'y + xA
DB = x'B + xA
z = B
    - Draw the logic diagram of the circuit.
    - Tabulate the state table.

Ans:





Present state		input		next state		Output
Q_A	Q_B	x	y	Q_A^+	Q_B^+	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	0	1	1
1	1	1	1	1	1	1

14. For the logic circuit of Fig. 3, prepare the truth table for various combinations (except R = S = 1) linking to Qn and Qn + 1.

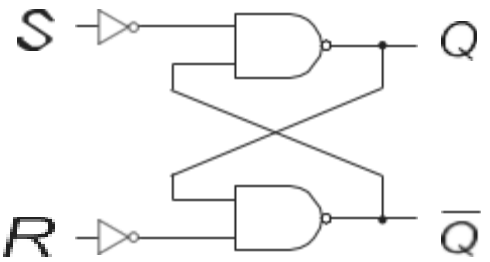


Fig 3

Ans:

S	R	Q+	Q'+
0	0	Q	Q'
0	1	0	1
1	0	1	0

16. Check the given excitation table of various flip-flops.

Qn	#	Qn-1	S	R	J	K	D	T
0		0	0	×	0	×	0	0
0		1	1	0	1	×	1	1
1		0	0	1	×	1	0	1
1		1	×	0	×	0	1	0

Hint: Look at the truth table of the flip-flops in the reverse way.

17. Convert
    (a) JK flip flop to SR flip flop
    (b) T flip flop to D flip flop

    Ans:

    a) Step 1: Write the truth table of the required flip-flop

Here the required flip-flop is SR flip flop

S	R	Qn	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Step 2: Write the excitation table of the given flip-flop

Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 3: The conversion table, which is a combination of truth table and excitation table

S	R	Q_N	Q_{N+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	1	X	X	X

Step 4: Find the Boolean expressions for the inputs of the given flip-flop

K-Map for J:

	$\bar{R}\bar{Q}_N$	$\bar{R}Q_N$	RQ_N	$R\bar{Q}_N$
$\bar{S}$	0	X	X	0
S	1	X	X	X

Expression for J would be

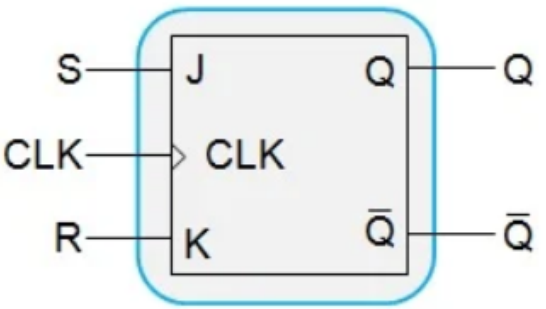
J=S

Now, K-Map for K:

	$\bar{R}\bar{Q}_N$	$\bar{R}Q_N$	RQ_N	$R\bar{Q}_N$
$\bar{S}$	X	0	1	X
S	X	0	X	X

Therefore, the expression for K would be

K=R



b) Step 1: Write the truth table of the required flip-flop

D	Q_N	Q_{N+1}
0	0	0
0	1	0
1	0	1
1	1	1

Step 2: Write the excitation table of the given flip-flop

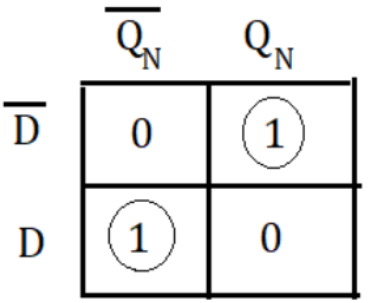
Q_N	Q_{N+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 3: The conversion table, which is a combination of truth table and excitation table

D	Q_N	Q_{N+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Step 4: Find the Boolean expressions for the inputs of the given flip-flop

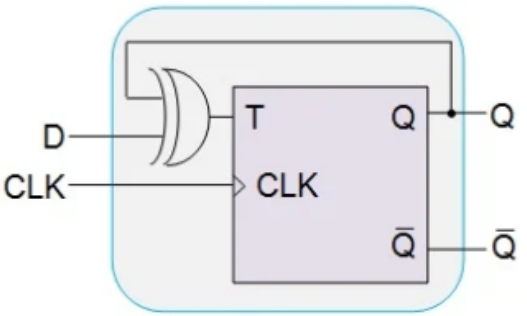
K-Map for T:



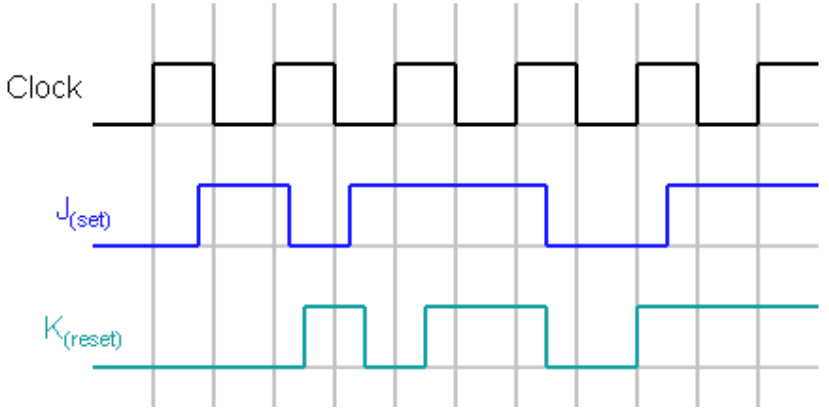
Expression for T would be

$$T = D'Q_N + DQ_N'$$

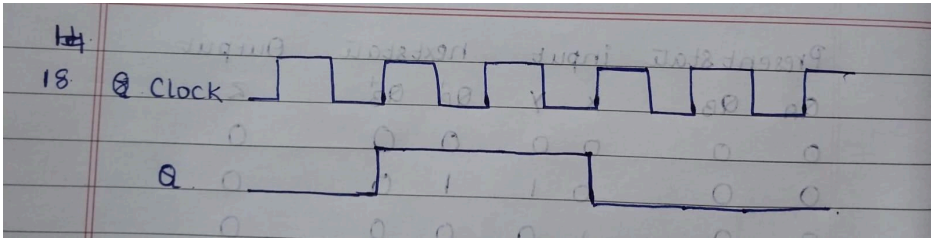
Step 5: Draw the circuit for implementing D flip-flop from T flip-flop



18. Draw the output waveform for the following waveform input to the JK flip-flop.

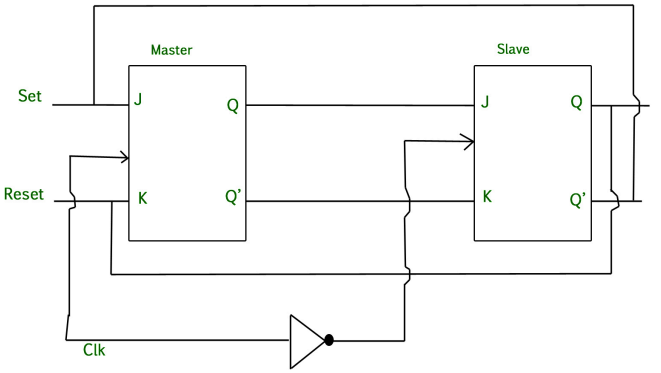


Ans: Considering positive edge triggered



19. How to overcome the race around condition in Jk flip flop? Explain the detailed procedure for the same.

Ans:
The most practical way to solve the problem of race-around condition in JK flip-flops is to use the JK flip-flops in the Master and Slave Mode.



Master-slave JK Flip-Flop

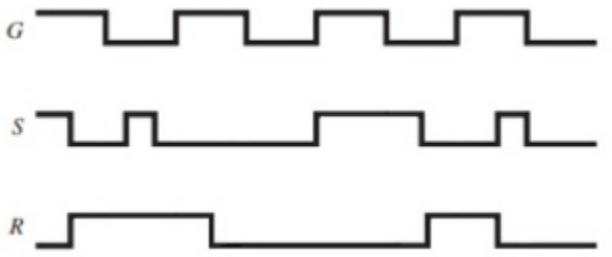
Working of a master slave flip flop –

When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.
Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.
If J=0 and K=1, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.
If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.
If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.
If J=0 and K=0, the flip flop is disabled and Q remains unchanged.

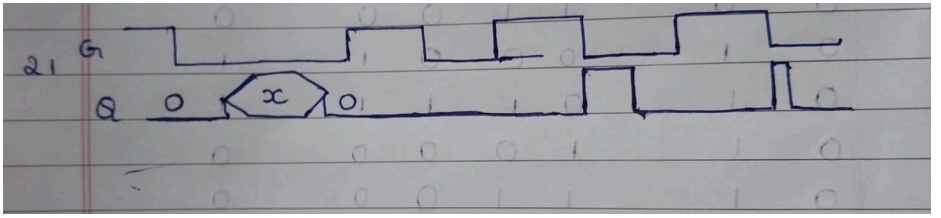
20. How does a Latch differ from a Flip Flop ?
Ans:

Latches	Flip Flops
Latches are building block of sequential circuits and they are built using logic gates	Flip flops are also building blocks of sequential circuits but they are made using latches
Latches continuously changes input and output changes correspondingly	Flip flop output changes only when clock is applied
Latches are level sensitive	Flip flops are edge sensitive

21. Given the following timing diagram for a SR Latch, sketch the output waveform Q. G is the enable input and is active LOW



Ans:



22. With a neat diagram explain the working of D flip flop

Ans:

D flip flop consist of a single input D and two outputs (Q and Q'). The basic working of D Flip Flop is as follows:

- When the clock signal is low, the flip flop holds its current state and ignores the D input.
- When the clock signal is high, the flip flop samples and stores D input.
- The value that was previously fed into the D input is reflected at the flip flop's Q output.
- If D = 0 then Q will be 0.
- If D = 1 then Q will be 1.

The Q' output of the flip flop is complemented by the Q output.

- If Q = 0 then Q' will be 1.
- If Q = 1 then Q' will be 0.