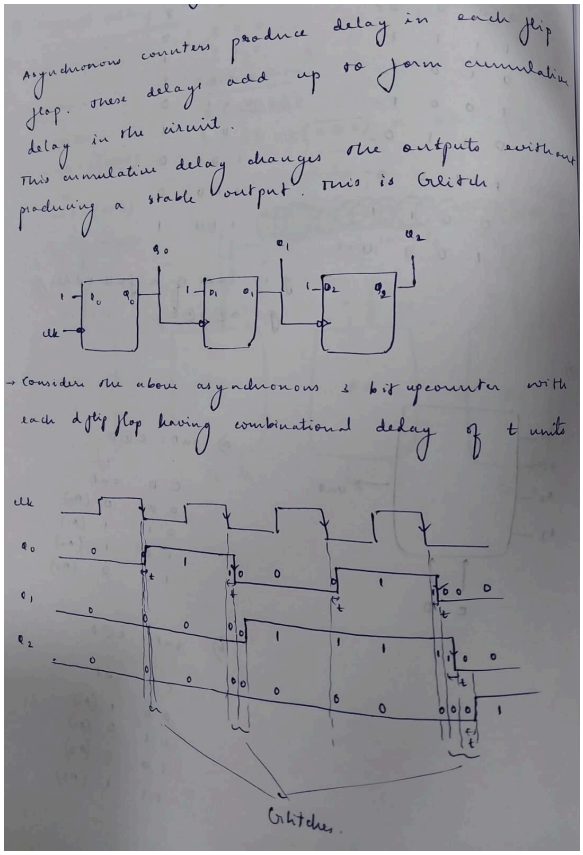
Digital Assessment-3

1. Explain the concept of glitch occurring in a counter with a relevant diagram? (1)
   Ans:



2. Derive the characteristic equation of a JK flip-flop using the K-map method?(1)
   Ans :

INPUTS			OUTPUTS
J	K	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$Q_{n+1} = Q'_nJ + Q_nK'$

3. Convert SR flip flop to D & T flip flop (3)

SR to D

Step 1: Write the truth table of the required flip-flop
Here the required flip-flop is D flip-flop

D	Q_N	Q_{N+1}
0	0	0
0	1	0
1	0	1
1	1	1

Step 2: Write the excitation table of the given flip-flop

In this case the given flip-flop is SR flip-flop

Q_N	Q_{N+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Step 3: The conversion table, which is a combination of the truth table and excitation table

To implement a D flip-flop from SR flip-flop is as follows

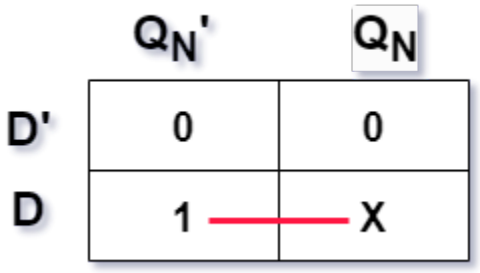
0	Q_N	Q_{N+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Step 4: Find the Boolean expressions for the inputs of the given flip-flop

In this case, the given flip-flop is SR.

Therefore, write the Boolean expressions for S AND R from the conversion table using K-Map.

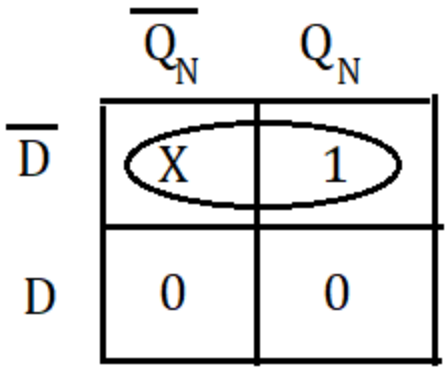
K-Map for S:



Expression for S would be

S=D

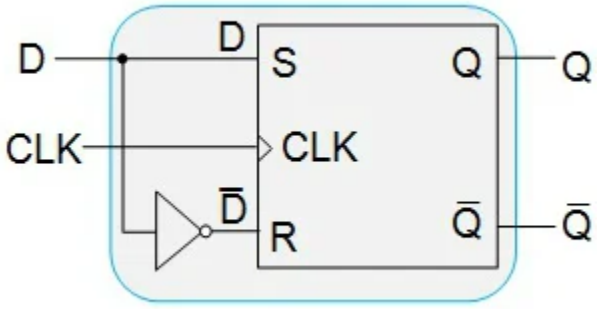
K-Map for R:



Expression for R would be

R=D'

Step 5: Draw the circuit for implementing D flip-flop from SR flip-flop



SR to T

Step 1: Write the truth table of the required flip-flop

Here the required flip-flop is T flip-flop

T	Q_N	Q_{N+1}
0	0	0
0	1	1
1	0	1
1	1	0

Step 2: Write the excitation table of the given flip-flop

In this case the given ff is SR ff

Q_N	Q_{N+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Step 3: The conversion table, which is a combination of the truth table and excitation table

To implement a T flip-flop from SR flip-flop is as follows

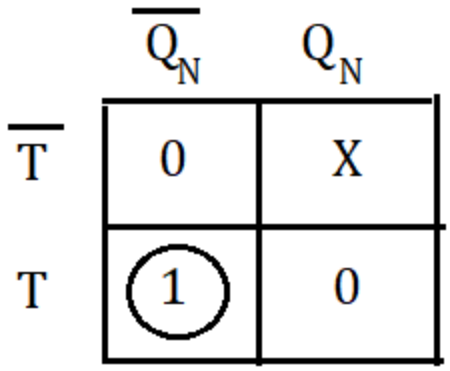
T	Q_N	Q_{N+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	1	0	1

Step 4: Find the Boolean expressions for the inputs of the given flip-flop

In this case, the given flip-flop is SR.

Therefore, write the Boolean expressions for S AND R from the conversion table using K-Map.

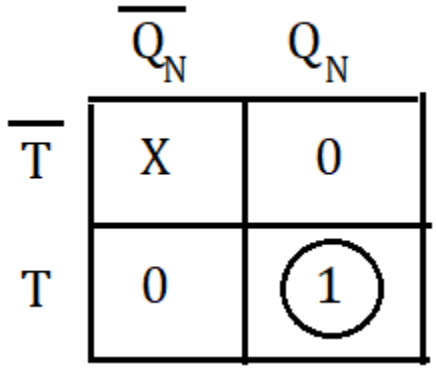
K-Map for S:



Expression for S would be

$$S = TQ_N'$$

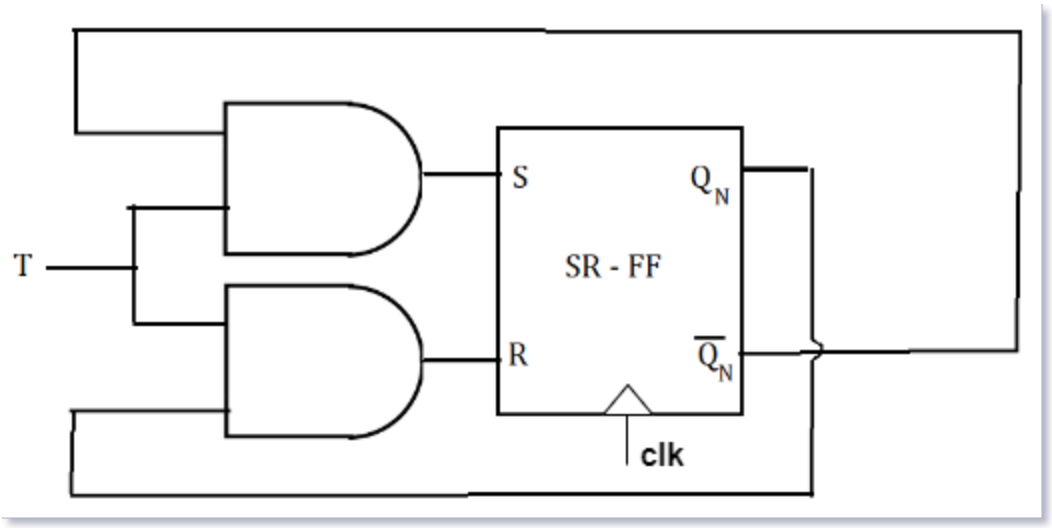
K-Map for R:



Expression for R would be

$$R = TQ_N$$

Step 5: Draw the circuit for implementing T flip-flop from SR flip-flop



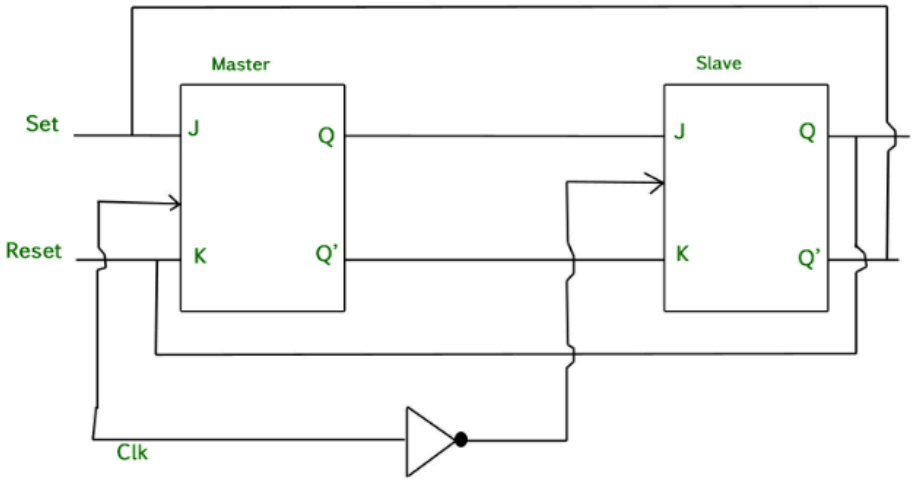
4. How to overcome the race around condition in Jk flip flop? Explain the detailed procedure for the same (4)

Ans:

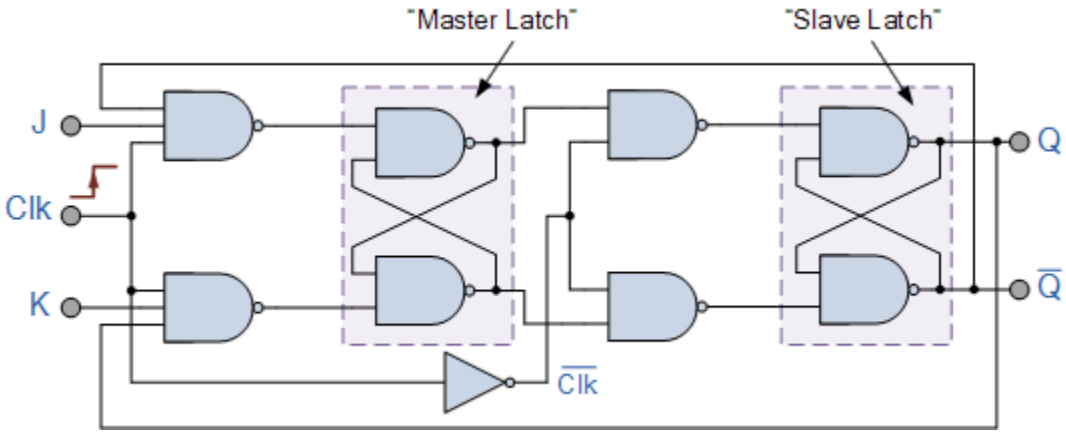
Master-Slave flip flops are mainly used to avoid the timing problems associated with JK flip-flops, such as the possibility of race conditions that can occur when both inputs change simultaneously.

When the clock signal transitions from low to high, the master latch that latches the input data and sets its output, while the slave latch remains in its previous state. Then, when the clock signal transitions from high to low, the slave latch captures the output of the master latch, and its output updates to the same state as the master latch.

By using this master-slave arrangement, the flip-flop avoids race conditions and provides a more reliable and predictable behavior than simple latches or flip-flops.



Working



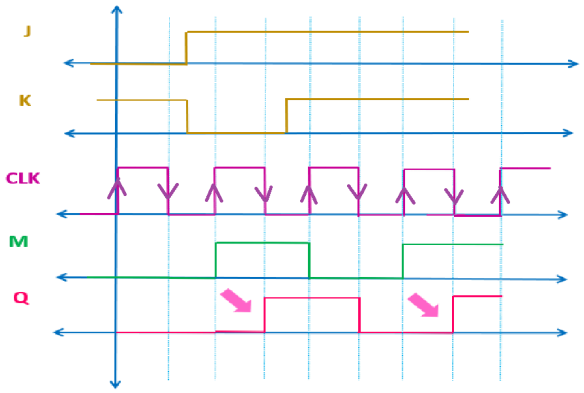
- When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave latch is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master latch to the slave and output is obtained.

Truth Table for Master-Slave J-K Flip Flop

J	K	CLK	Q	Q'	
0	0	⎍	Q_0	Q_0'	Hold
0	1	⎍	0	1	Reset
1	0	⎍	1	0	Set
1	1	⎍	Q_0'	Q_0	Toggle (opposite state)

- When J = 0, K = 0 and clk is 1 master will be active and slave wont be active due to a inverter. Lets assume a value 0 to Q ad Q' will be 1 to both master and slave output hence there will be no change in the output and occurs in positive edge for master and when clock is 0 it occurs in negative edge for slave and it remains in the hold state.
- When J = 0, K = 1 and clk is 1 master will be active and slave wont be active due to a inverter. Lets assume a value 0 to Q ad Q' will be 1 to both master and slave output hence output remains same as input and occurs in positive edge for master and when clock is 0 it occurs in negative edge for slave and it remains in the reset state.

- When J = 1, K = 0 and clk is 1 master will be active and slave wont be active due to a inverter. Lets assume a value 0 to Q ad Q' will be 1 to both master and slave output hence output remains same as input and occurs in positive edge for master and when clock is 0 it occurs in negative edge for slave and it remains in the set state.
- When J = K = 1, and clk is 1 master will be active and slave wont be active due to a inverter. Lets assume a value 0 to Q ad Q' will be 1 to both master and slave output hence output Q will be 1 and Q' is 0 and then at the positive edge of the clock pulse, the master flip flop toggles (means the change of the previous state into its opposite state), and at the negative edge of the clock pulse, the slave flip flop toggles.



5. Define set-up time, hold time and propagation delay (3)

   Set-up time : The amount of time the data at the input must be stable before the active edge of the clock. Any violation may cause incorrect data to be captured, which is known as setup violation.

   Hold time : The amount of time the data at the input must be stable after the active edge of the clock. Any violation may cause incorrect data to be captured, which is known as Hold violation.

   Propagation delay : The delay for the input to propagate to the output

6. Explain the concept behind an edge-triggering flip-flop? Explain why we need them? (2)

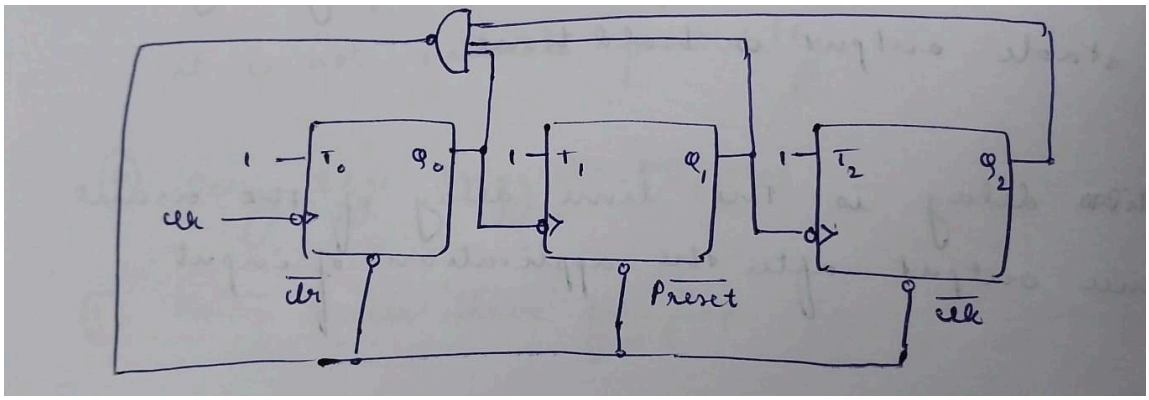
   Ans:

   Edge Triggered Flip-Flops

   • Uses just one of the edges of the control to affect the reading of information on input lines.
   • Designed to use either the positive or negative edge of the clock.
   • Once the triggering edge occurs the flip-flop remains unresponsive to information input changes until the next triggering edge.

To avoid race around condition.
To make the circuit less prone to glitches.

7. Design an asynchronous counter which counts the sequence 2-3-4-5-6-2? (2)
   Ans:



8. Write the excitation table for JK and D (2)
   Ans:

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

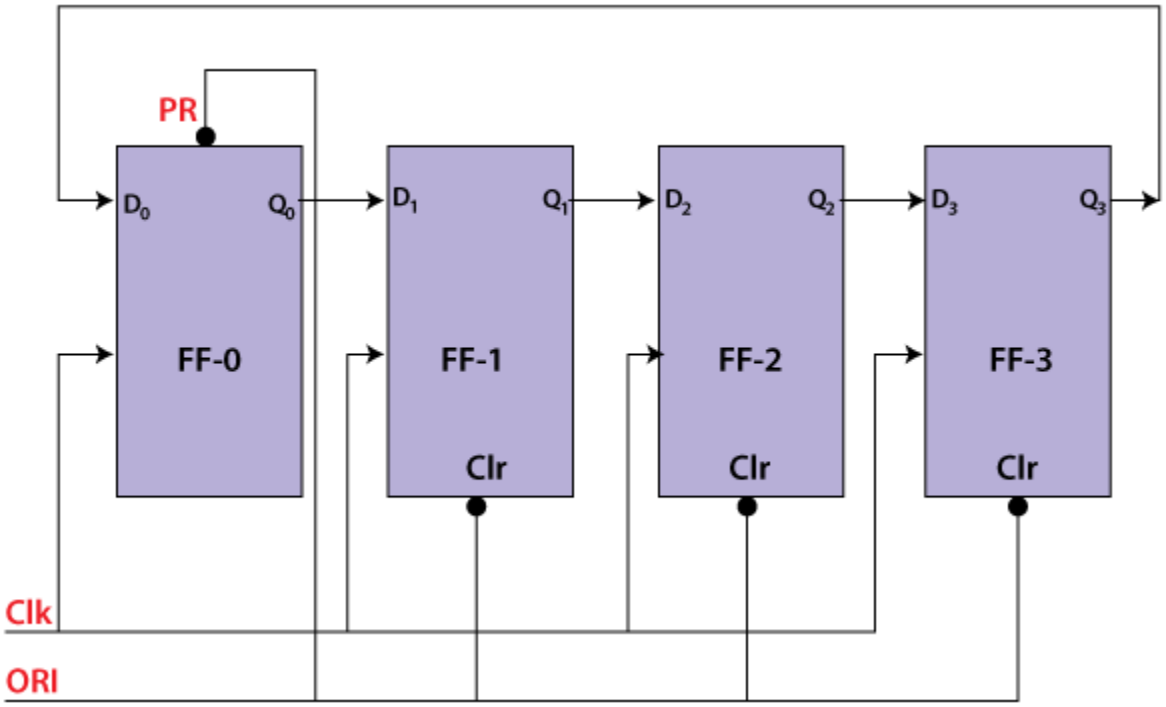
JK Flip-flop

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

D Flip-flop

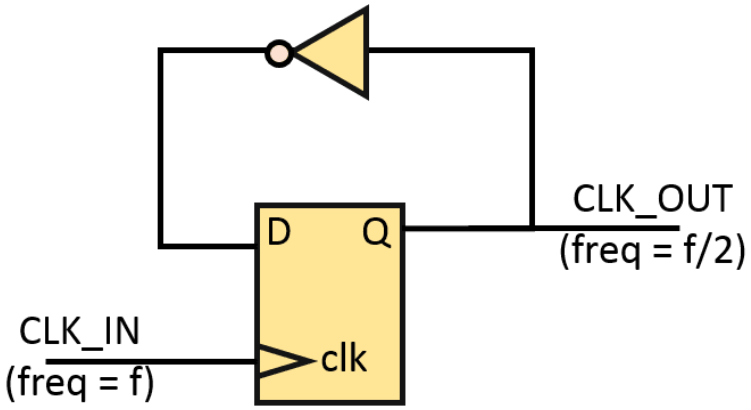
9. What is the number of flip flops required to design Mod 273 asynchronous counter (1)
   Ans:
   9 flip flops

10. Design a 4-bit ring counter? (2)

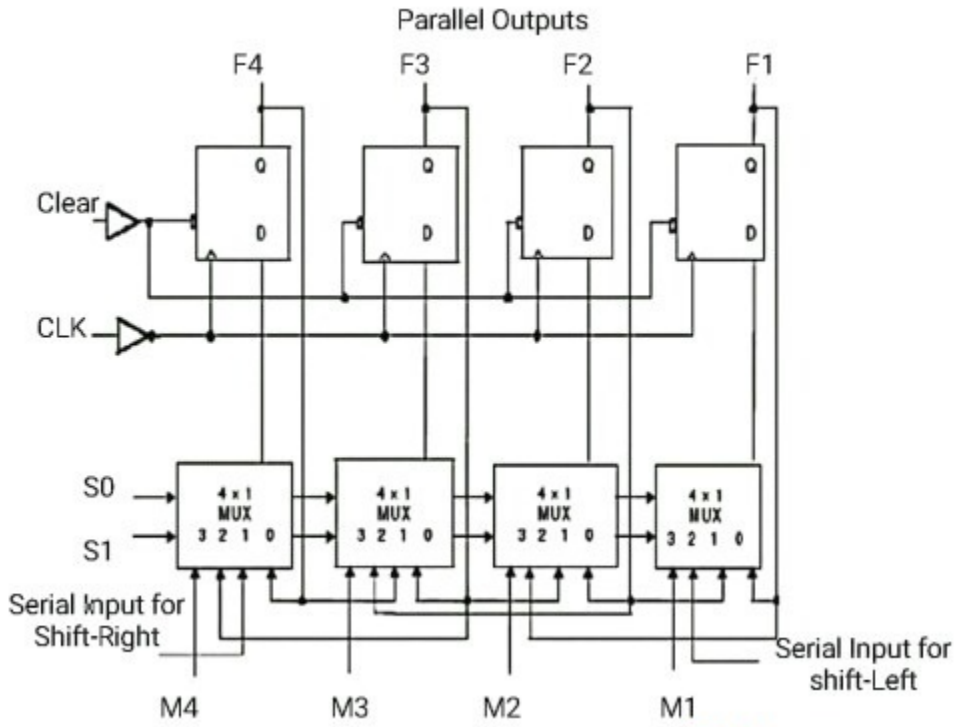


11. Design a frequency divider circuit to implement frequency/2? (2)

Ans:



12. With a neat diagram and waveform, explain the working of an Universal shift register (4)

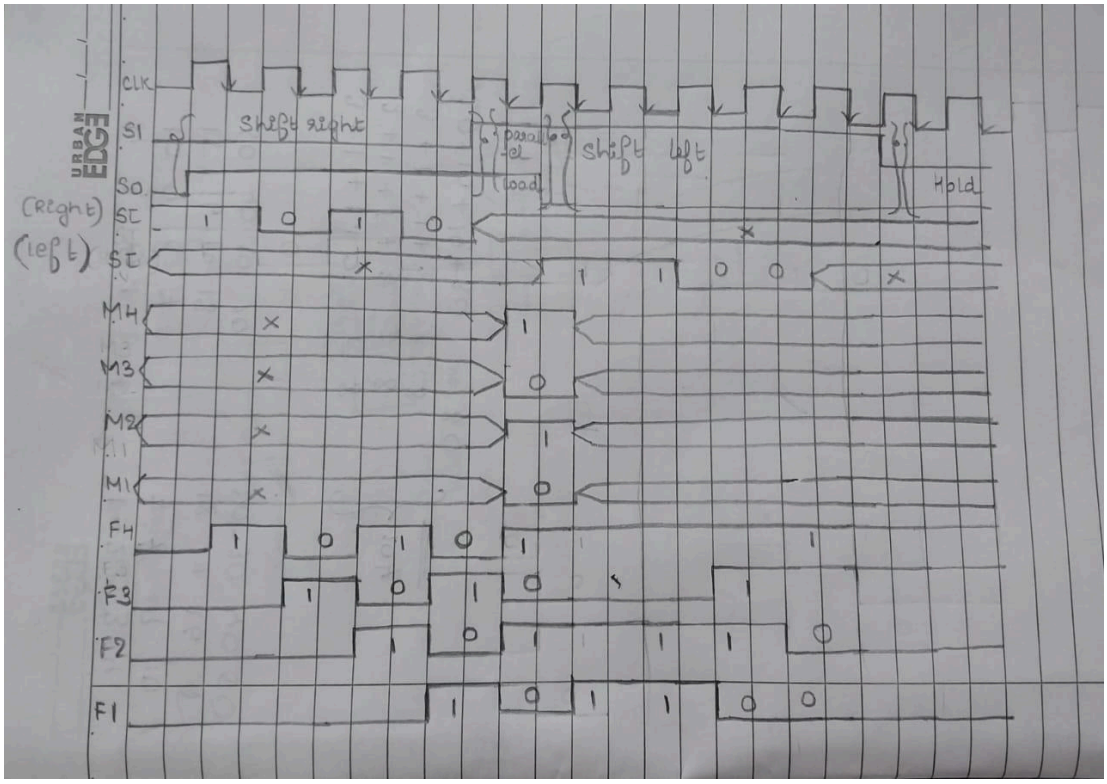


- From the above figure, selected pins the mode of operation of the universal shift register. Serial input shifts the data towards the right and left and stores the data within the register.
- Clear pin and CLK pin are connected to the flip-flop.
- M0, M1, M2, M3 are the parallel inputs while F0, F1, F2, F3 are the parallel outputs of flip-flops
- When the input pin is active HIGH, then the universal shift register loads / retrieve the data in parallel. In this case, the input pin is directly connected to 4×1 MUX
- When the input pin (mode) is active LOW, then the universal shift register shifts the data. In this case, the input pin is connected to 4×1 MUX via NOT gate.
- When the input pin (mode) is connected to GND (Ground), then the universal shift register acts as a Bi-directional shift register.
- To perform the shift-right operation, the input pin is fed to the 1st AND gate of the 1st flip-flop via serial input for shit-right.
- To perform the shift-left operation, the input pin is fed to the 8th AND gate of the last flip-flop via input M.
- If the selected pins S0= 0 and S1 = 0, then this register doesn’t operate in any mode.

That means it will be in a Locked state or no change state even though the clock pulses are applied.

- If the selected pins S0 = 0 and S1 = 1, then this register transfers or shifts the data to left and stores the data.
- If the selected pins S0 = 1 and S1 = 0, then this register shifts the data to right and hence performs the shift-right operation.
- If the selected pins S0 = 1 and S1 = 1, then this register loads the data in parallel. Hence it performs the parallel loading operation and stores the data.

Waveform:



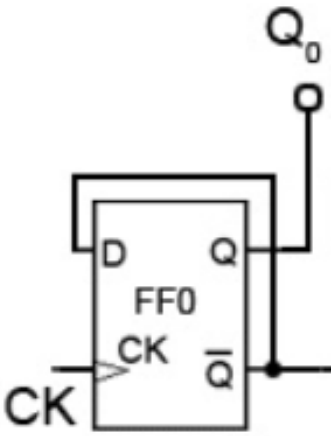
13. a. The initial state of the ring counter is 0010. What will be the output after 17 clock pulses?
    b. The initial state of the ring counter is 0000 (No Preset). What will be the output after 10 clock pulses (2)

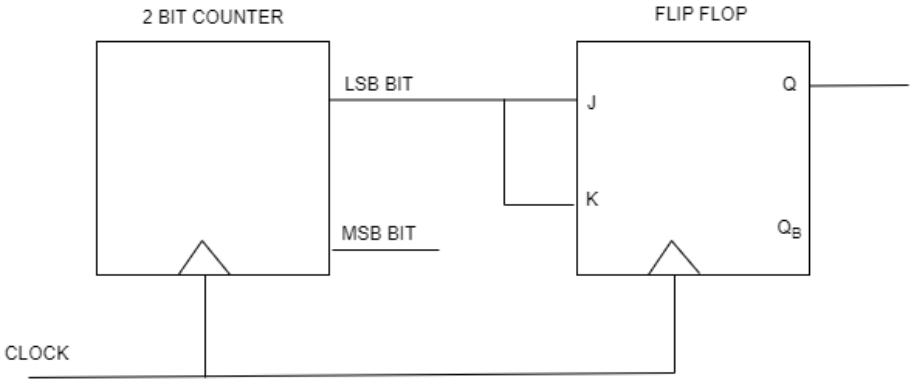
    Ans:

    a. 0001
    b. 0000

14. Construct a T flip flop using D flip flop which performs operation of input HIGH only (without externally supplying the input) (2)

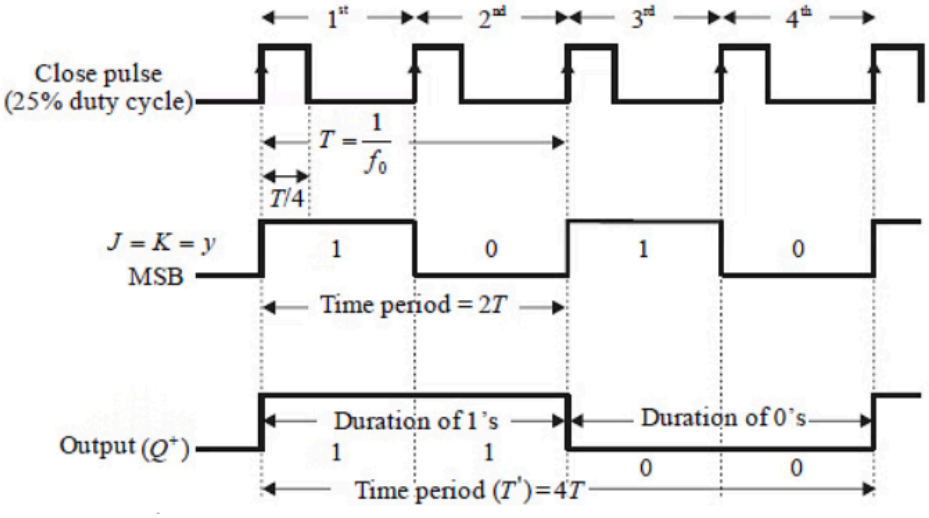
Ans:





15. For the circuit shown, the clock frequency is f0 and the duty cycle is 25%. Draw the CLOCK and output Q waveform. What will be the output frequency in comparison with f0 and what will be its duty cycle (3)

Ans:



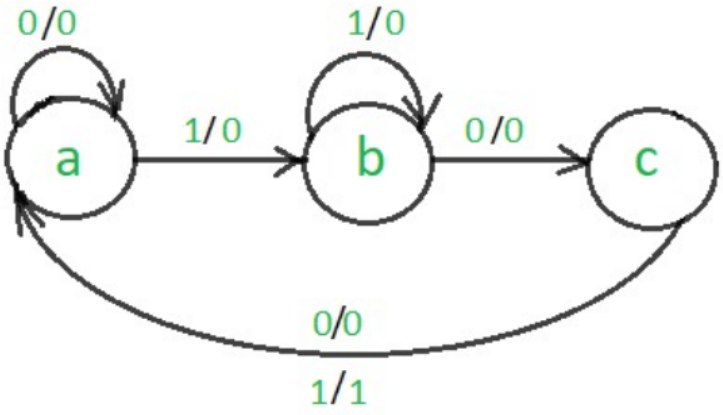
Period of Q is 4T, Thus frequency is f0/4 and the duty cycle is 50%.

16. Design a non-overlapping 101 Mealy sequence detector circuit (5)

Ans:

Step 1: Develop the state diagram –

The state diagram of a Mealy machine for a 101 sequence detector is:



a = 00, b = 10, c = 01

Step 2: Code Assignment –

Rule 1 : States having the same next states for a given input condition should have adjacent assignments.

Rule 2: States that are the next states to a single state must be given adjacent assignments.

Rule 1 given preference over Rule 2.

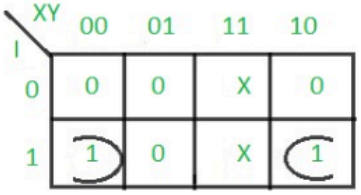
States	Next States
a	a,b
b	b,c
c	a

Step 3: Make Present State/Next State table –

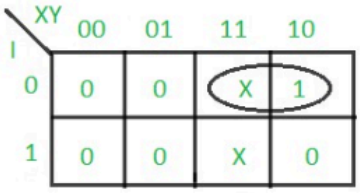
We'll use D-Flip Flops for design purposes.

Present States		i/p	Next States		Flip Flop Excitations		O/P
X	Y		X'	Y'	Dx	Dy	
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	1	1	0	1	0	0
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

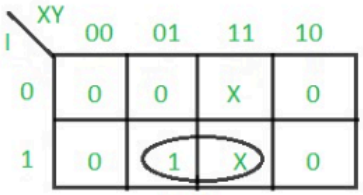
Step 4: Draw K-maps for Dx, Dy and output (Z) –



Dx=$\overline{Y}$.I

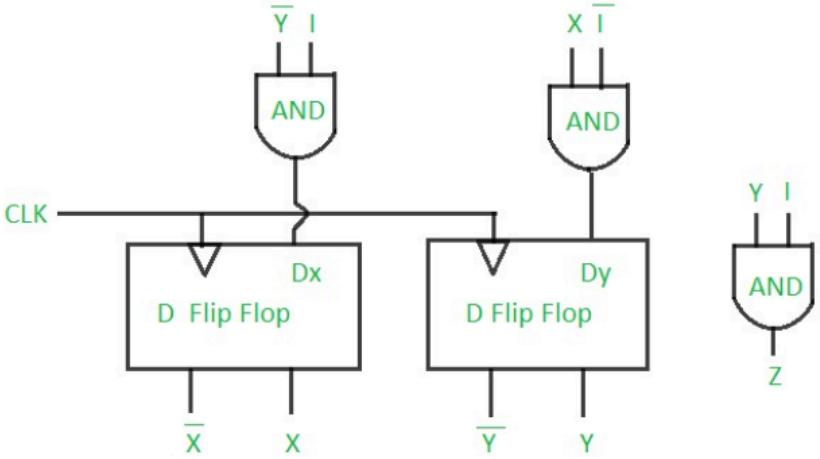


Dy= X.$\overline{I}$



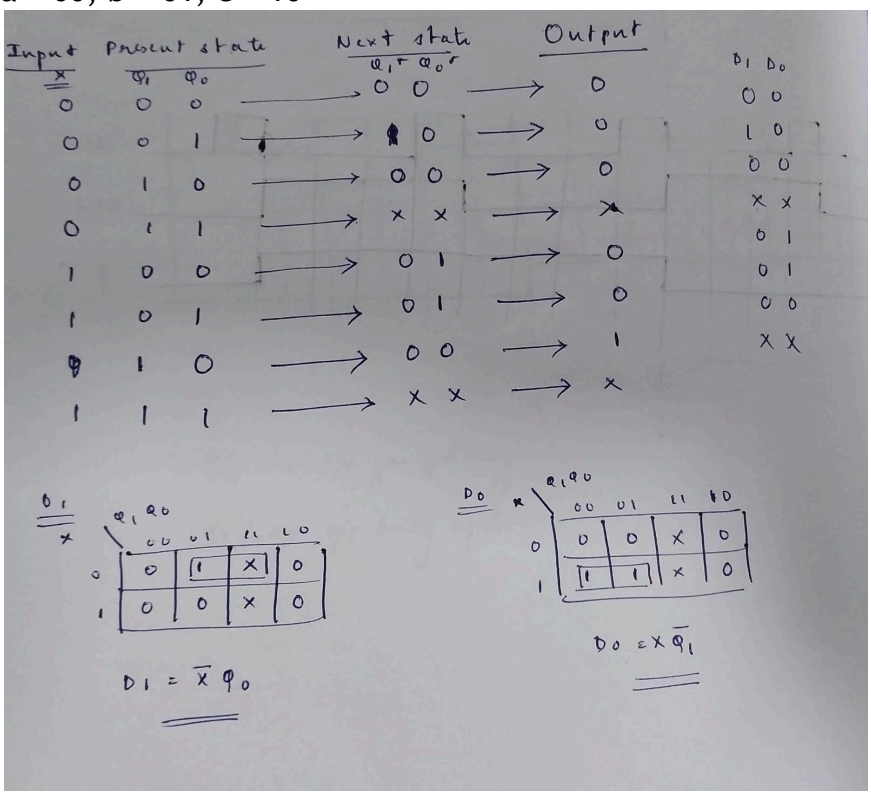
Z=Y.I

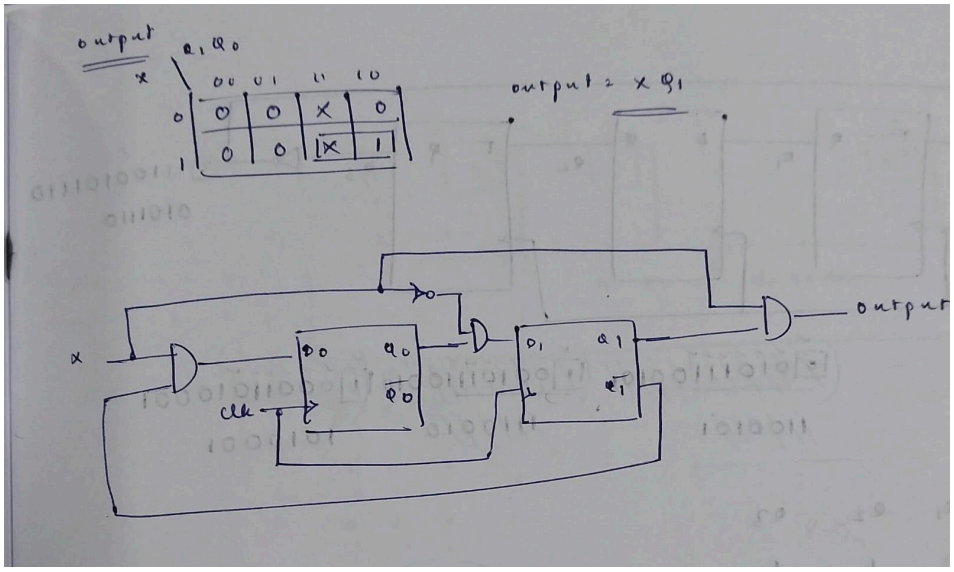
Step 5: Finally implement the circuit –



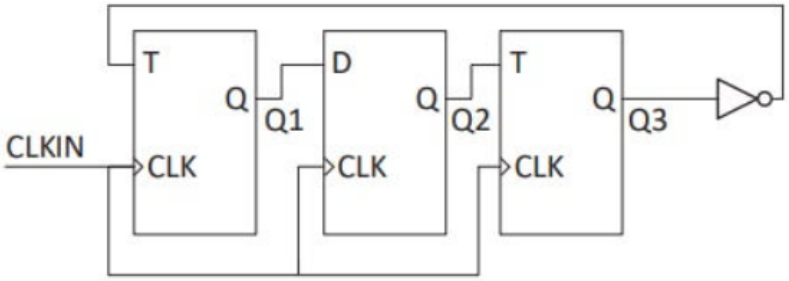
OR

a = 00, b = 01, c = 10





17. Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. At the beginning Q1, Q2, Q3 have values 0, 1 and 1 respectively. Draw the state diagram describing the pattern of outputs (2)



Ans:

From the given 3 state counter made from T flipflops and D flipflops, the next input sequence are as follows:

- $T_0 = \overline{Q}_2$
- $D_1 = Q_0$
- $T_2 = Q_1$

Initial State			Current input			Next State		
Q_0	Q_1	Q_2	T_0	D_1	T_1	Q_0^+	Q_1^+	Q_2^+
0	1	1	0	0	1	0	0	0
0	0	0	1	0	0	1	0	0
1	0	0	1	1	0	0	1	0
0	1	0	1	0	1	1	0	1
1	0	1	0	1	0	1	1	1
1	1	1	0	1	1	1	1	0
1	1	0	1	1	1	0	1	1

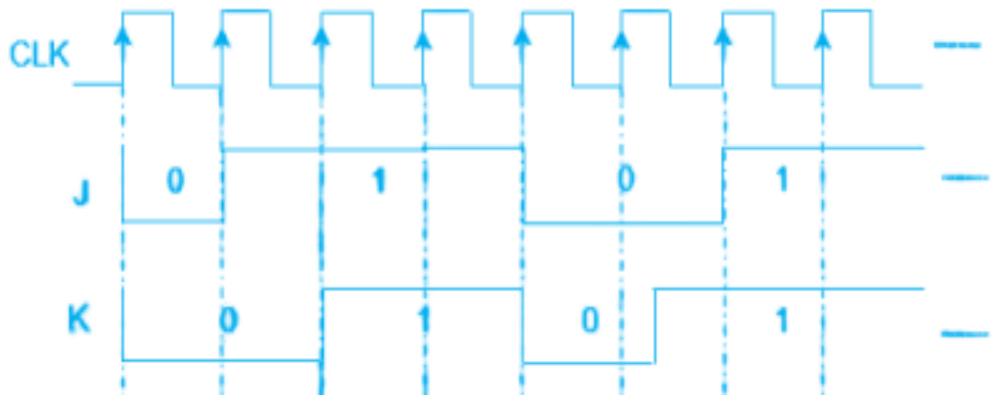
we can see from the above table given counter count sequence like $011 \rightarrow 000 \rightarrow 100 \rightarrow 010 \rightarrow 101 \rightarrow 111 \rightarrow 110$. The state 001 is missing.

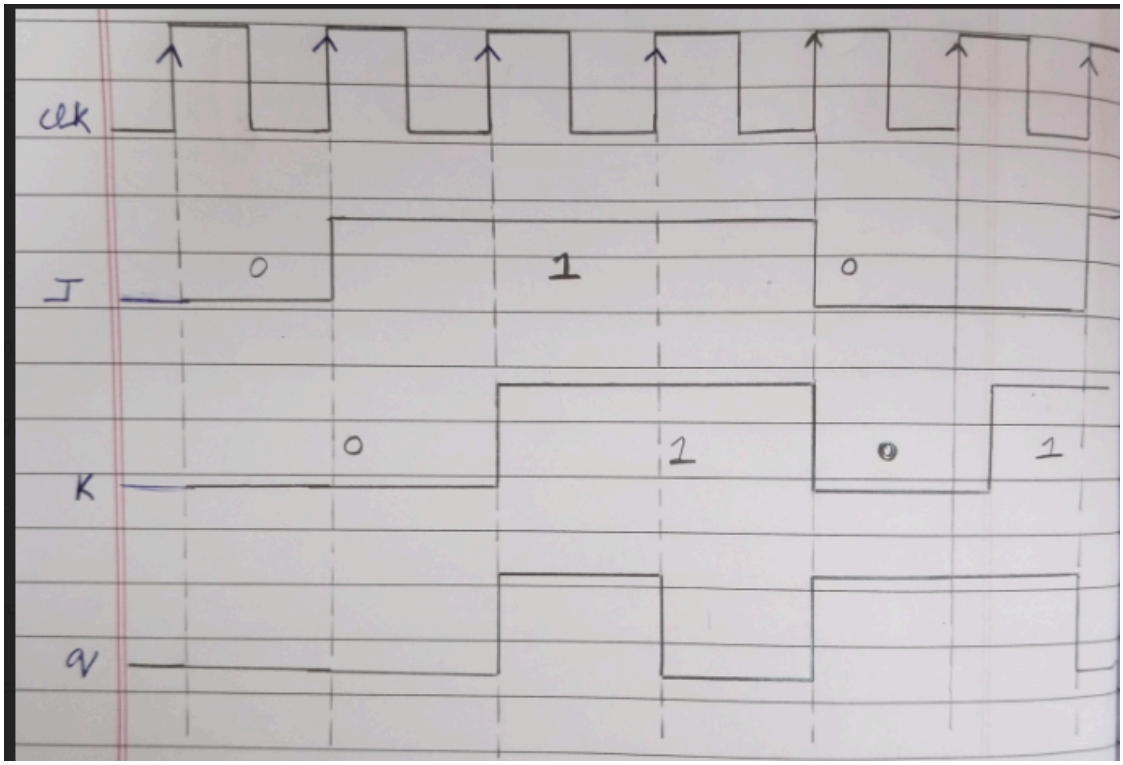
18. Let k = 2^n. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2^n bit decoder. This circuit is equivalent to which counter of how many bits? (2)

    Ans:

    k bit Ring counter

19. Draw the output waveform of the JK master-slave configuration (Consider the timing constraints): (2)


CLK
J
0
1
0
1
K
0
1
0
1


clk
J
0
1
0
K
0
1
0
1
Q