

as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff

- System Design and Analysis
- IC Package Design and Analysis
- Mixed Signal Modeling and Verification
 Tensilica® Processor IP
- Computational Fluid Dynamics
- Safety and Reliability Platform

Onboarding

cadence

PCB Design and Analysis Learning Map

Logic Design

Allegro® X Design Entry HDL Front-to-Back Flow (2) [3]

Beginner

OrCAD® X Capture



Allegro X Design **Entry HDL Basics**



Allegro X System **Capture Basics ⊘** 0.5 **▲**

Allegro X System Capture



Allegro Design Reuse



Analog Simulation with PSpice® using Design Entry HDL **4** OrCAD CIS



OrCAD X Capture **Constraint Manager PCB 5** Flow

Allegro EDM Design Entry HDL Front-to-**Back Flow** 3

Analog Simulation with PSpice® 23 1

Analog Simulation with PSpice® using System Capture **⊘ 3 4**

PCB Design

OrCAD X Presto Basic **Techniques**



Allegro X PCB Editor Basic **Techniques**



Allegro X PCB Editor Intermediate Techniques **2.5**

Allegro X PCB Router Basics



Allegro X PCB Editor **Advanced Methodologies**



Allegro X High-Speed Constraint **⊘** 2 **△** Management

Allegro DesignTrue DFM



Allegro X Update Training



Advanced Design Verification with the RAVEL Programming **⊘** 2 **△** Language

SI/PI Analysis

Essential High-Speed PCB Design for Signal Integrity



PCB Design at RF - Multi-Gigabit Transmission, EMI Control, and PCB Materials



Sigrity Aurora



Sigrity PowerDC[™] and OptimizePI[™]





Model Generation and Analysis using PowerSI and Broadband SPICE

Clarity 3D Solver NEW





DE-HDL Library Development using DE-HDL **2 2**







Allegro X EDM PCB Librarian







⊘ 3 **▲**





Allegro Design Entry HDL SKILL® **Programming Language**

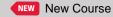


Allegro X PCB Editor SKILL **Programming Language**



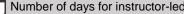




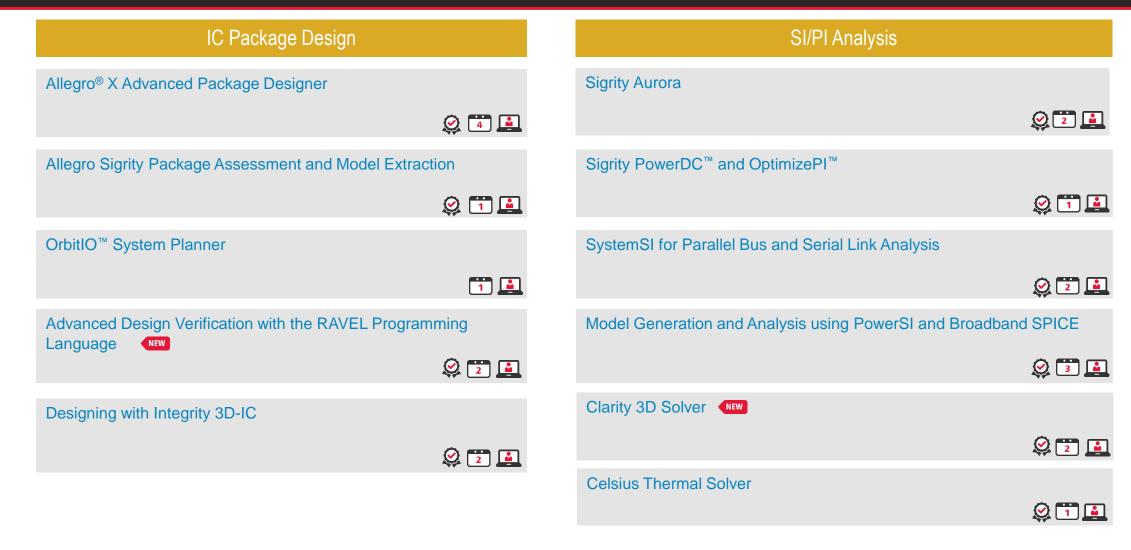


Advanced





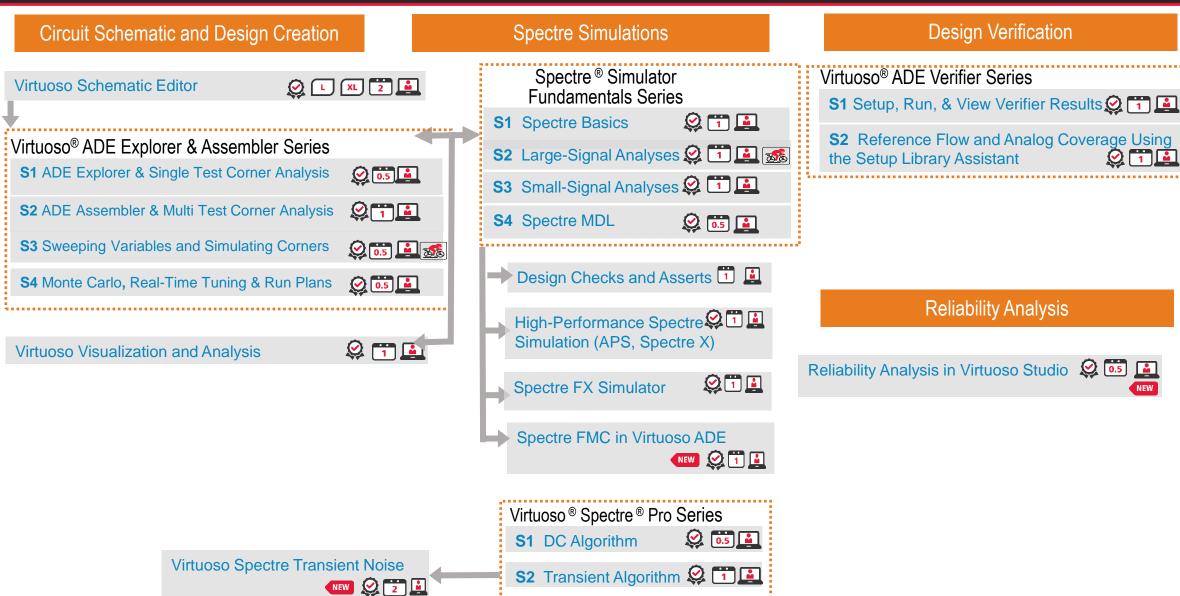
IC Package Design and Analysis Learning Map

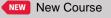




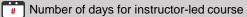
Advanced













Accelerated Learning Path Course

Advanced

AWR Microwave Design Microwave & RF Design (AWR®) Microwave Office for RF Designers Planar EM Analysis in AWR Microwave Office NEW Q 2

System Design

5G mmWave Handset System Design -\$1 Simulation and Verification of the RFIC (Transceiver)

RF Design and Simulations

Virtuoso Schematic Editor Q L XL 2 Virtuoso® ADE Explorer & Assembler Series **S1** ADE Explorer & Single Test Corner Analysis **⊘** 0.5 **≜** S2 ADE Assembler & Multi Test Corner Analysis

Spectre [®] Simulator Fundamentals Series

S1 Spectre Basics

Q 1 **L S2** Large-Signal Analyses

2 1 \$3 Small-Signal Analyses

Spectre ® RF Series

RF Analysis Using Shooting Newton

RF Analysis Using Harmonic Balance

Custom IC/Analog Physical Design and Verification Learning Map IC CAD Physical Design and Advanced Nodes **Physical Verification** Virtuoso® Layout Design Basics Virtuoso® Layout Pro Series SKILL® Language Quantus™ Pegasus **Programming** T1: Env. and Basic Commands Q L 1 Verification Introduction (2) [2] System NEW T2: Create and Edit Commands Q L 1 **2 2** SKILL Language Virtuoso Connectivity-Driven **Programming Layout Transition** T3: Basic Commands **⊗ XL** 1 **≜ Physical ⊘ 5 4** L XL GXL EXL 2

T4: Advanced Commands

T6: Constraint-Driven Flow

T7: Module Generator

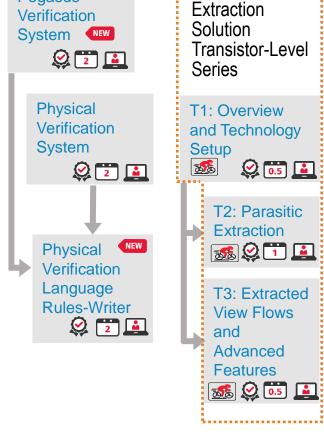
and Floorplanner

and Power Routing 😂 XL GXL 1

T8: Concurrent Layout Editing (EXL)

T9: Virtuoso Design Planner (EXL 2)

T5: Interactive Routing



Accelerated Learning Path Course



Advanced



SKILL Development

2 2

3

of Parameterized

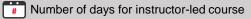
Advanced SKILL

Programming NEW

Language

Cells





Platform

Nodes



€ EXL 0.5

Virtuoso Abstract Generator

Virtuoso Floorplanner

Virtuoso® Advanced-Node – ICADVM

T1: Place and Route (2) 1

T2: Electromigration (2) 0.5 (2)

Virtuoso Layout for Advanced **Nodes and Methodology**

Virtuoso Layout for Advanced

GXL 1

GXL 1

2

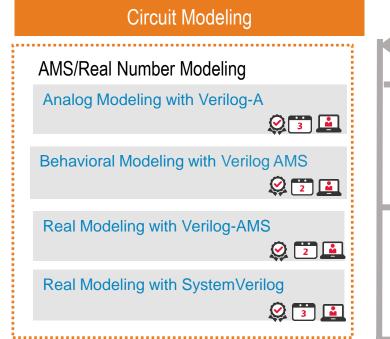


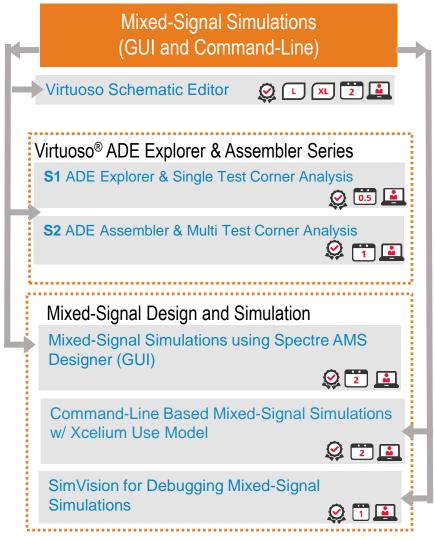
⊗ XL 1 **≜**

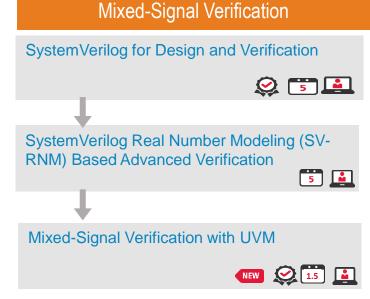
⊗ XL 1 **≜**

XL GXL 1

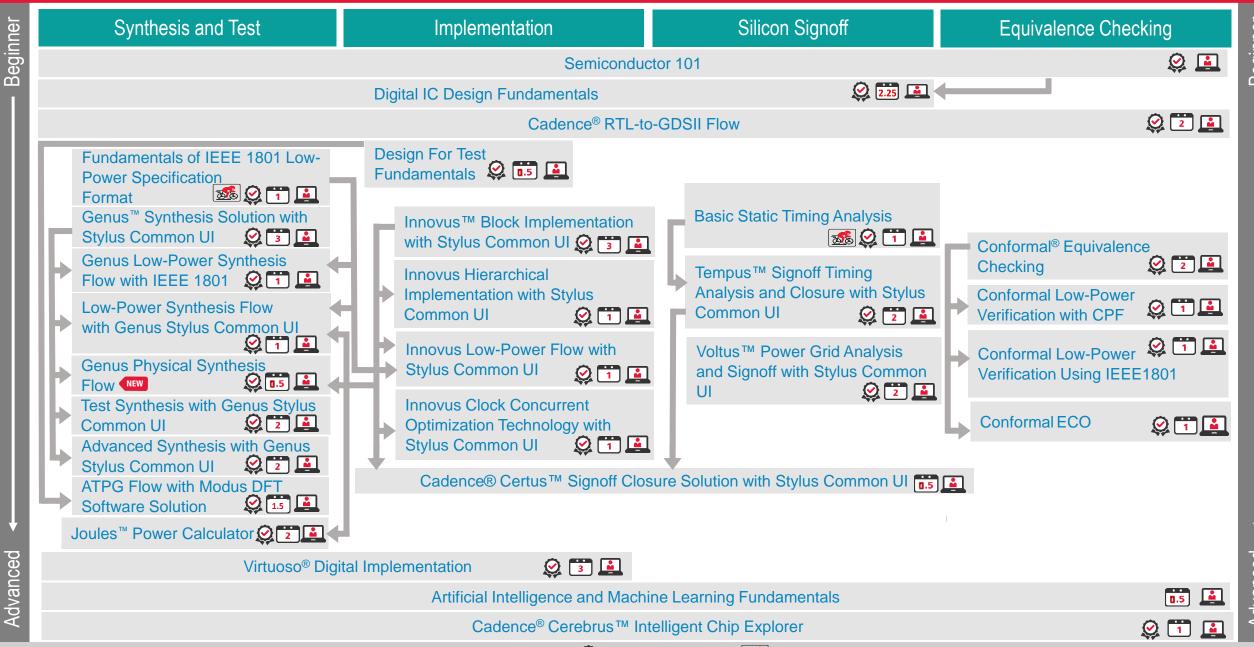
Mixed-Signal Modeling, Simulation and Verification Learning Map





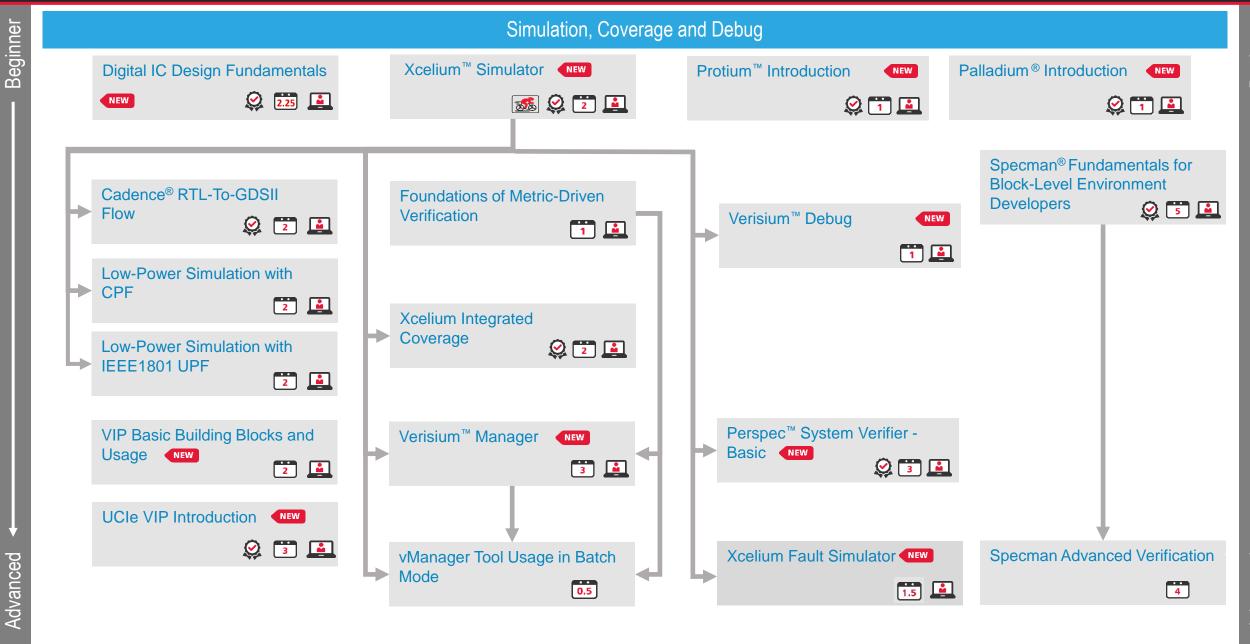


Digital Design and Signoff Learning Map

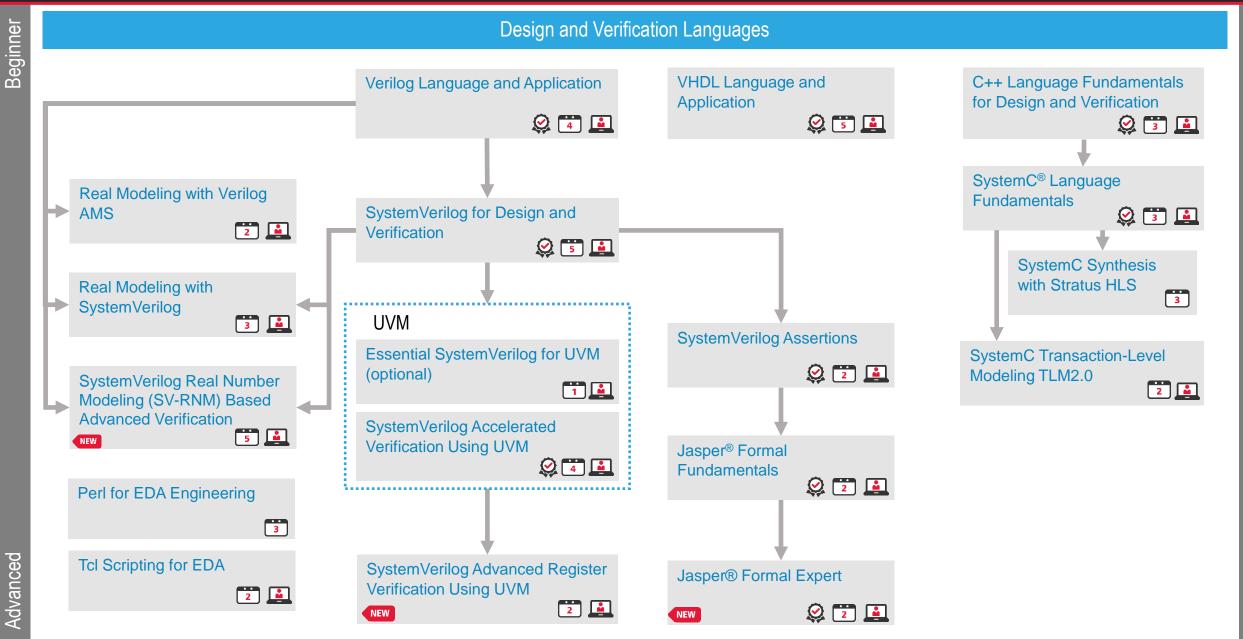


Advanced

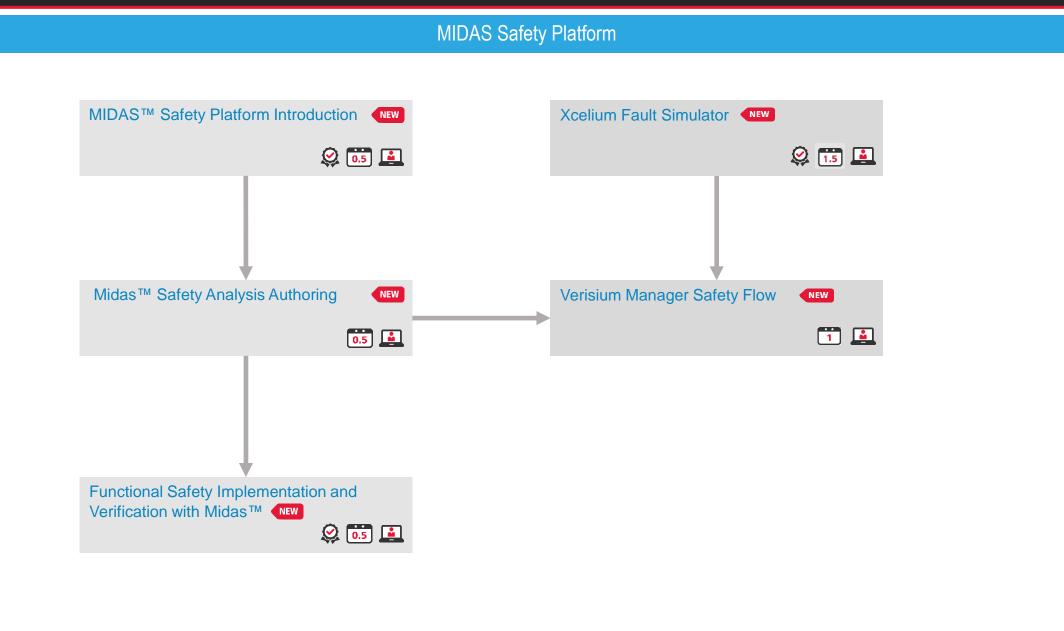
System Design and Verification Learning Map



System Design and Verification Learning Map



Safety and Reliability Platform Learning Map



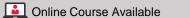


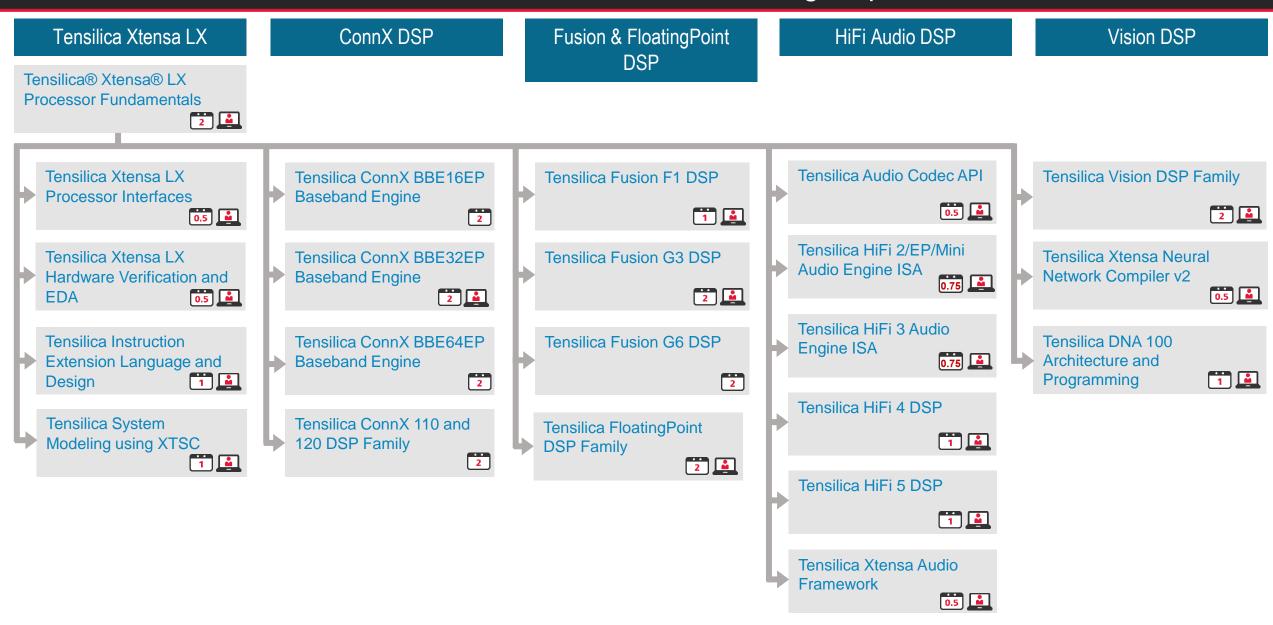
Advanced

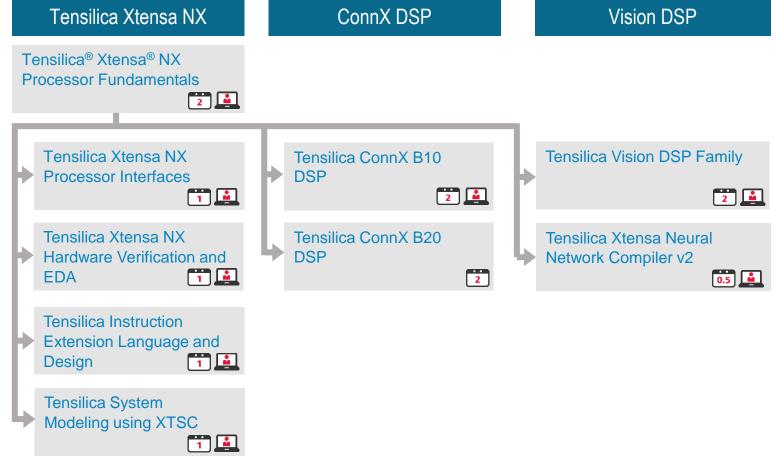




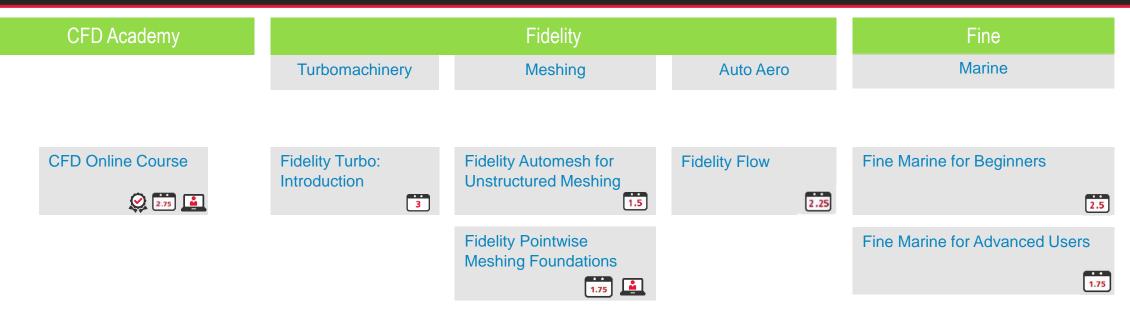








Computational Fluid Dynamics

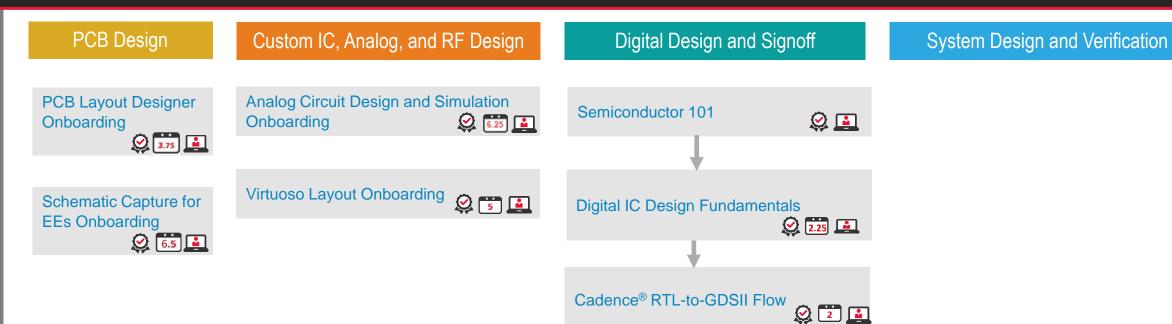


Number of days for instructor-led course

Advanced

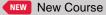


Onboarding Curricula



See also: https://www.cadence.com/en_US/home/training/bridging-the-learning-gap/onboarding-curricula.html

Advanced





© 2020 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks or cadenarks or cadenarks or cadenarks or cadenarks or cadenarks or cadenarks or service marks owned by MIPI Alliance. All PCI-SIG specifications are registered trademarks or trademarks or cadenarks or cadenary cadenary