# 19EC302: Digital System Design

Department of Electronics and Communication Engineering

**NMAM INSTITUTE OF TECHNOLOGY**

*(An Autonomous Institution affiliated to VTU, Belagavi)*

Nitte – 574110, Karkala, Udupi District, Karnataka, India

# Unit 3

# Flip Flops and its application

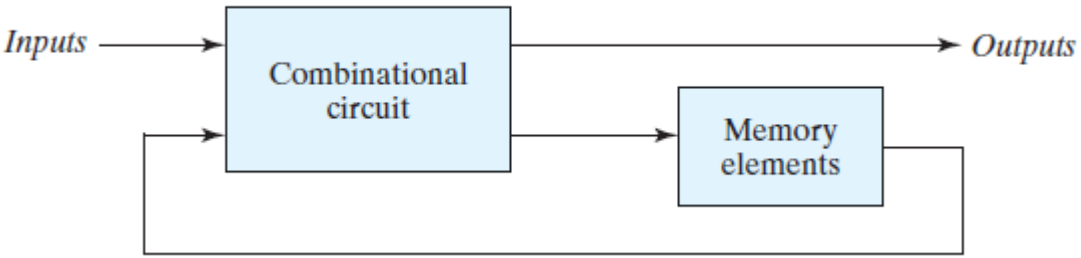
# Course Learning Objectives

After learning this unit the student should be able to

1. Understand the operation and use of Latches
2. Describe the operation of several types of pulse and edge-triggered flip-flops, such as the J-K, D-type, S-R and T-type

# Introduction

- The outputs at any instant are dependent not only upon the inputs present at that instant but also upon the past history (or sequence) of inputs
  - Sequential circuits are said to have memory
  - All sequential circuits require the existence of feedback

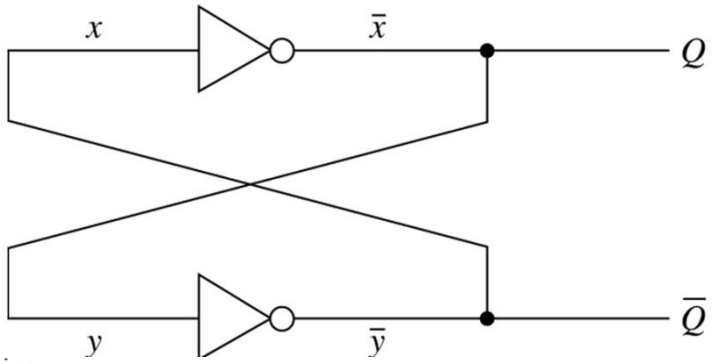


# Sequential Circuit Types

- A Synchronous Sequential Circuit is one in which its behaviour is determined by the values of signals at only discrete instants of time
  - Generally have a master-clock that effectively samples the input data to determine network behaviour
- An Asynchronous Sequential Circuit is one in which the network is immediately affected by input signal changes.

# Basic Bistable element

- Consists of two cross coupled inverters with two outputs named $Q$ and $\overline{Q}$
  - Assume x=0 initially => Q=y=1 =>$\overline{Q}$= x =0.
  - Assume x=1 initially =>Q=y=0 =>$\overline{Q}$= x =1.
- The circuit is stable in both the levels.



# Bistable Element

- It is used to store binary symbols.
- Stored symbol is referred to as *content* or *state* of the element
- When the device is storing '1' it is said to be 'set' or in '1-state'. When storing '0' it is said to be 'reset' or in '0-state'

# Latches

- Latch is an electronic logic circuit with **two stable states**.
- Latch has a **feedback** path to **retain the information**. Hence a latch can be a **memory device**.
- Latch can store one bit of information as long as the device is **powered on**.
- When enable is asserted, latch immediately changes the stored information when the input is changed i.e. they are level triggered devices. It continuously samples the inputs when the enable signal is on.

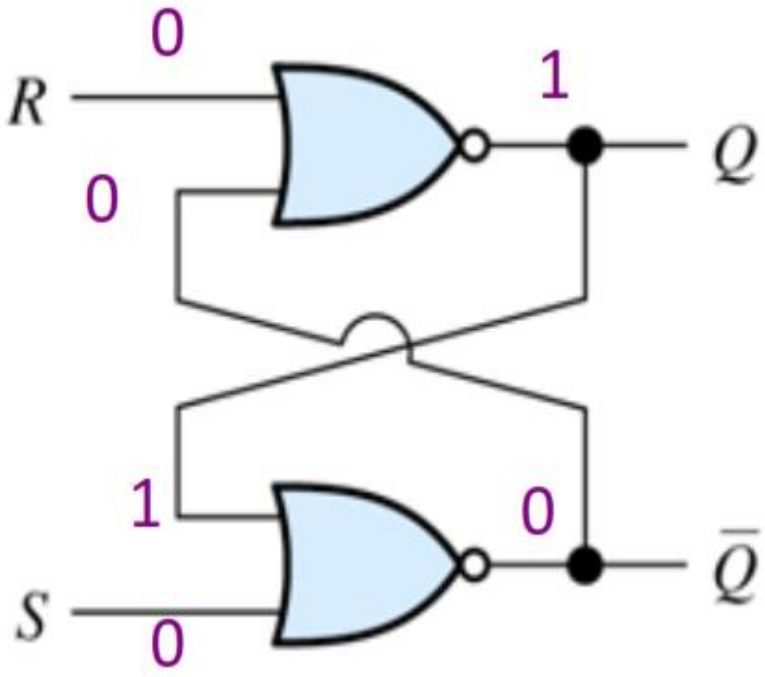
# Flip-Flop

- The Flip-flop remains in a given state as long as the **power is applied** and until **input signal** applied causes its output to change.
- Inputs to Flip-flop can be of two types
  - Synchronous or gated inputs: Signal change produces an change in output only when some control signal occurs
  - Asynchronous or direct inputs: Signal change produces an immediate change in output

# Difference between Latches and Flip Flops

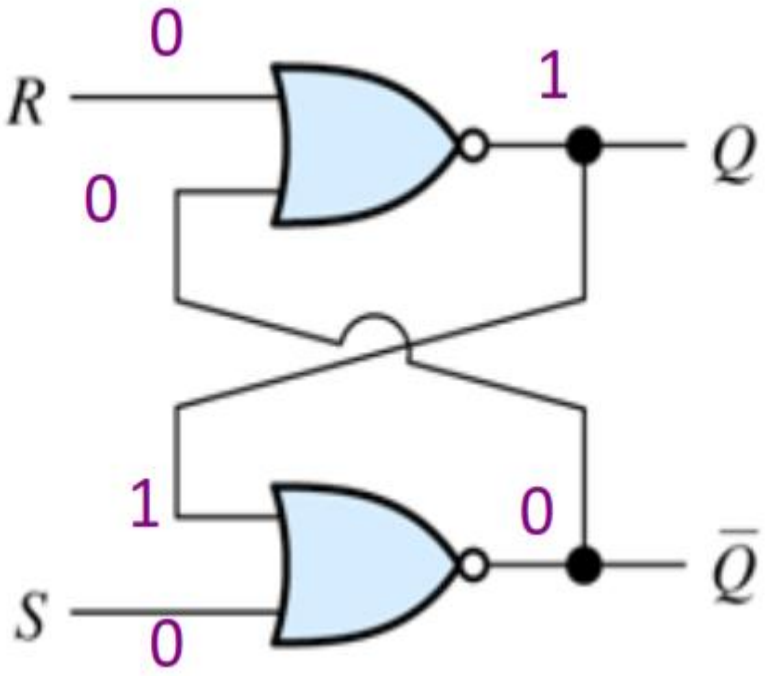
| Latches | Flip Flops |
|---|---|
| Latches are building blocks of sequential circuits and these can be built from logic gates | Flip flops are also building blocks oof sequential circuits. But, these can be built from the latches. |
| Latch continuously checks its inputs and changes its output correspondingly. | Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal |
| The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on | Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register. |
| It is based on the enable function input | It works on the basis of clock pulses |
| It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0. | It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse. |

# SR Latch Circuit: HOLD/LATCH Mode



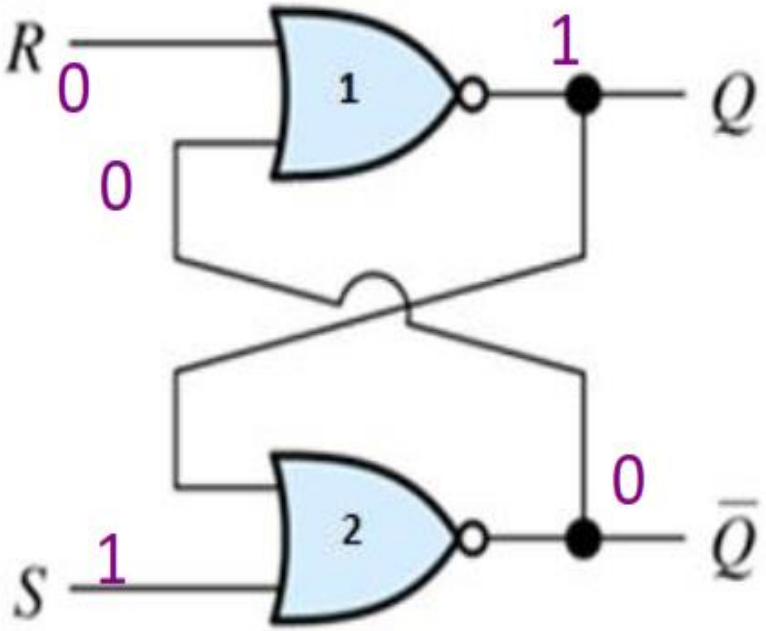

- **S = 0, R = 0**; This is the normal resting state of the circuit and it has no effect on the output states. Q and Q' will remain in **whatever state** they were in **prior** to the occurrence of this input condition. It works in HOLD (no change) mode operation.

# SR Latch
## Truth Table: HOLD/LATCH Mode



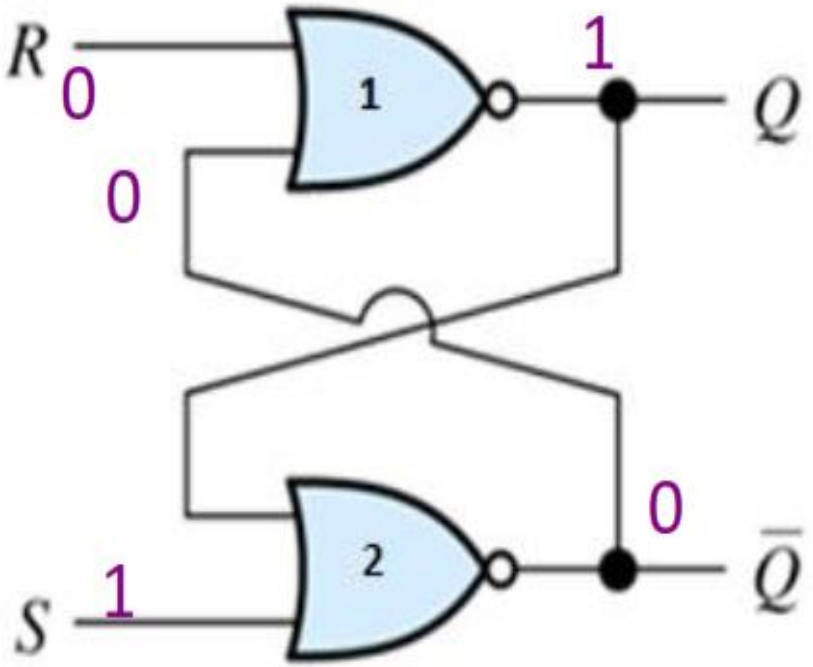

| SR-FLIP-FLOP | | | |
|---|---|---|---|
| R | S | Q | $\bar{Q}$ |
| 0 | 0 | Last state | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

# SR Latch Circuit: SET Mode



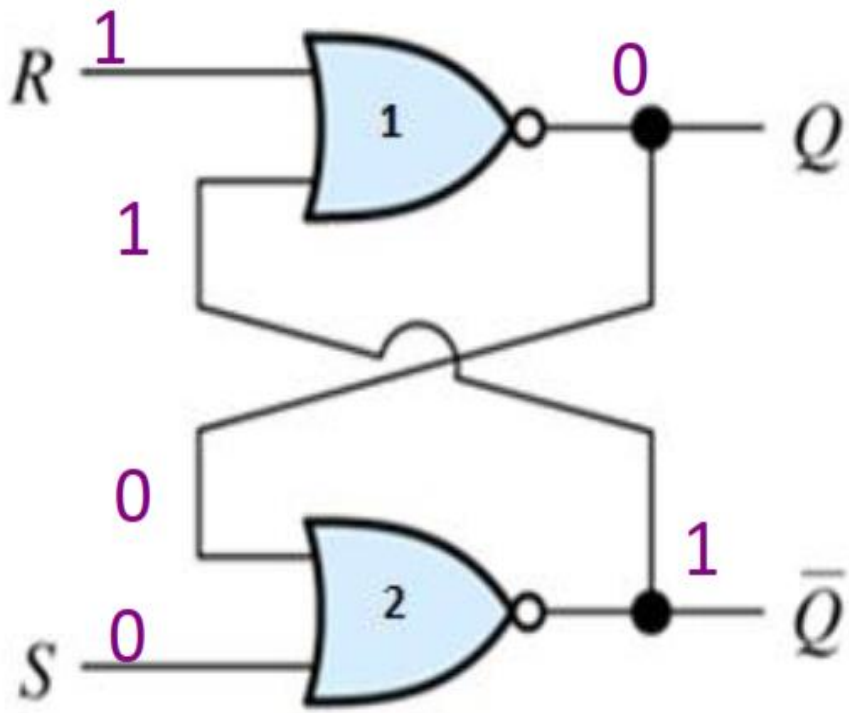

- Consider the input **S = 1**. Any time the input of a NOR gate is 1 the output is 0. So, the output of the second NOR gate is 0, i.e. Q' = 0.
- Q' = 0 is fed back into the input of the first NOR gate. So, with **R = 0**, the output of the first NOR gate is 1, i.e. Q=1.

# SR Latch
# Truth Table: SET Mode



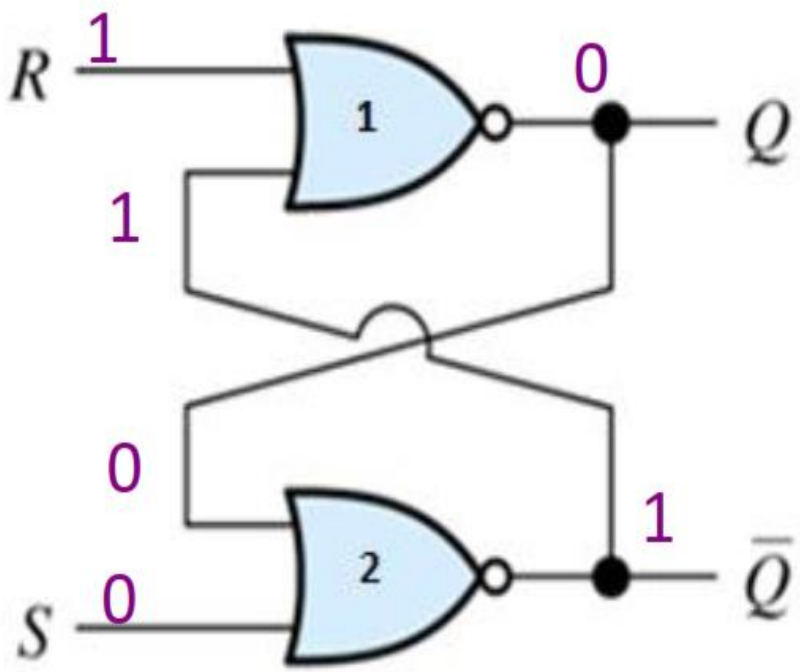

| SR-FLIP-FLOP | | | |
|---|---|---|---|
| R | S | Q | $\bar{Q}$ |
| 0 | 0 | Last state | |
| 0 | 1 | 1 | 0 |
| 1 | 0 | | |
| 1 | 1 | | |

# SR Latch Circuit: RESET Mode



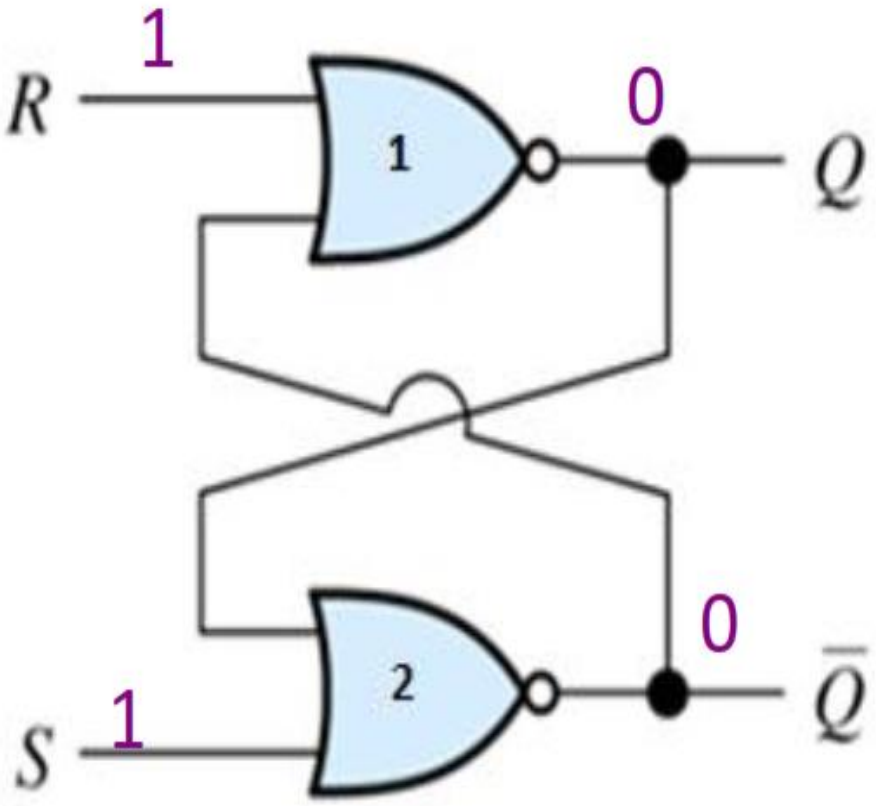

- Consider the input **R = 1**. Any time the input of a NOR gate is 1 the output is 0. So, the output of the first NOR gate is 0, i.e. Q = 0.
- Q = 0 is fed back into the input of the second NOR gate. So, with **S = 0**, the output of the second NOR gate is 1, i.e. Q'=1.

# SR Latch
# Truth Table: RESET Mode



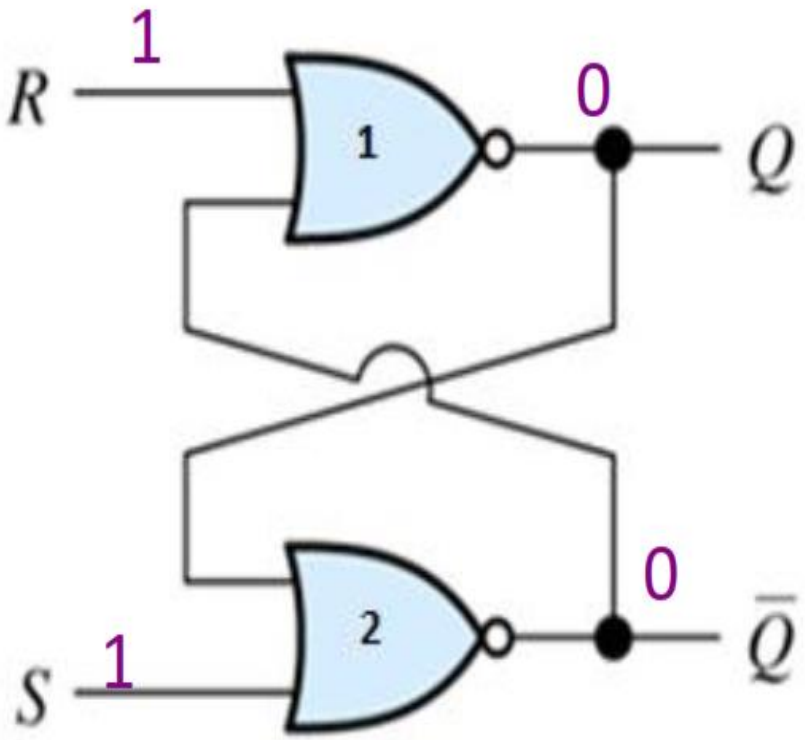

| SR-FLIP-FLOP | | | |
|---|---|---|---|
| R | S | Q | $\bar{Q}$ |
| 0 | 0 | Last state | |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | | |

# SR Latch Circuit: INVALID Mode



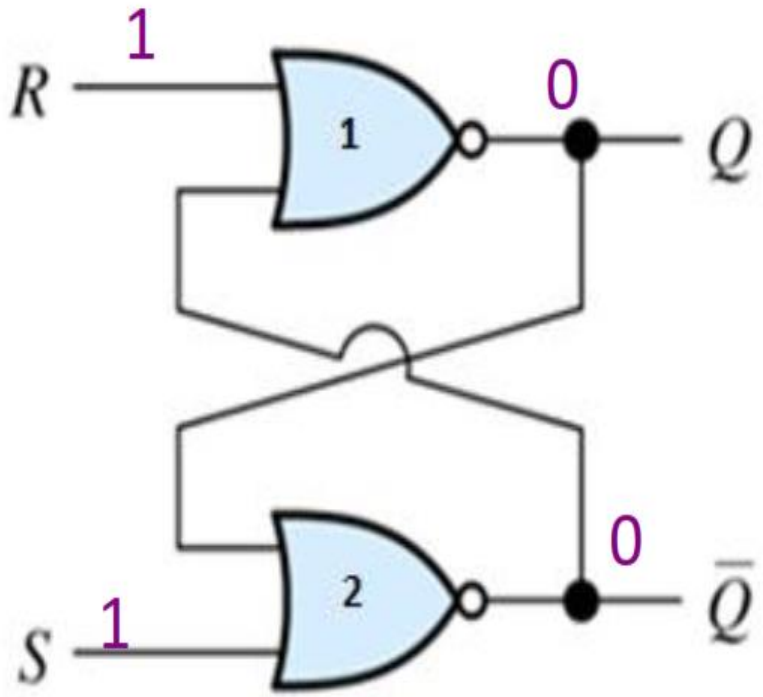

- **S = 1, R = 1**; This condition tries to set and reset the NOR gate latch at the same time, it produces **Q = Q' = 0**. This is an unexpected condition and is not used.
- The two outputs should be the inverse of each other.

# SR Latch
# Circuit: INVALID Mode




- If the inputs are returned to 1 simultaneously, the output states are unpredictable.
- This input condition should not be used and when circuits are constructed, the design should make this condition SET=RESET=1 never arises.

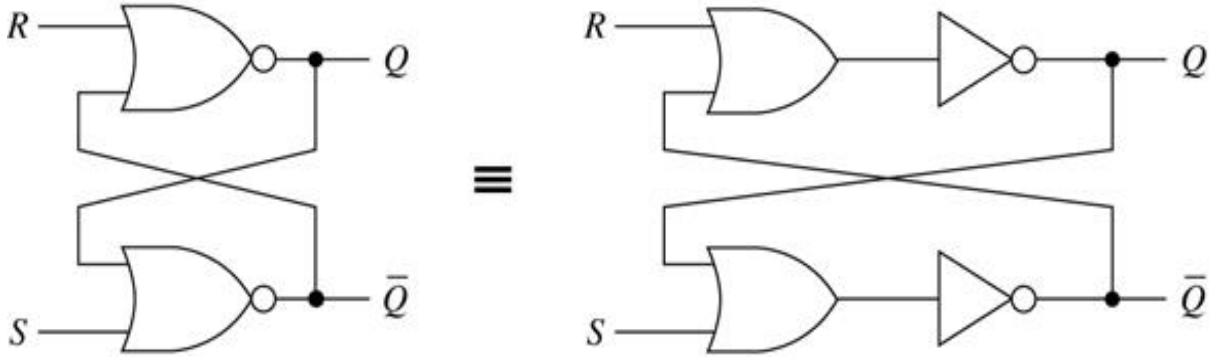
# SR Latch
# Circuit: INVALID Mode




| SR-FLIP-FLOP | | | |
|---|---|---|---|
| R | S | Q | $\bar{Q}$ |
| 0 | 0 | Last state | |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | Illegal | |

# R-S Latch [summary]

- Consists of two cross-coupled NOR gates.
- 2 inputs [R-Reset, S-Set] and 2 outputs [$Q$ , $\overline{Q}$]

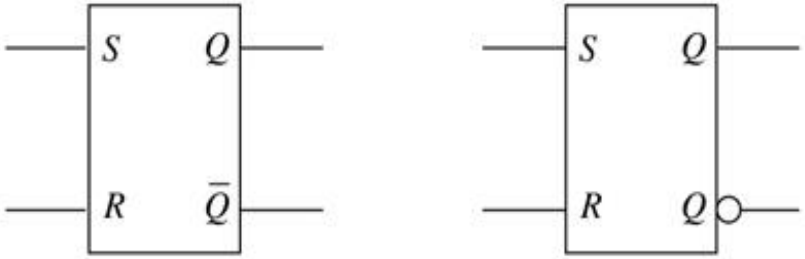



(a)

| Inputs | | Outputs | |
|---|---|---|---|
| $S$ | $R$ | $Q^+$ | $\overline{Q}^+$ |
| 0 | 0 | $Q$ | $\overline{Q}$ |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0* | 0* |

*Unpredictable behavior will result if inputs return to 0 simultaneously

(b)




(c)

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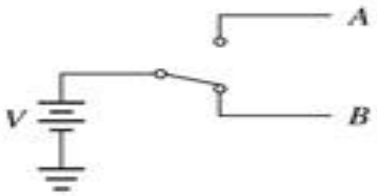
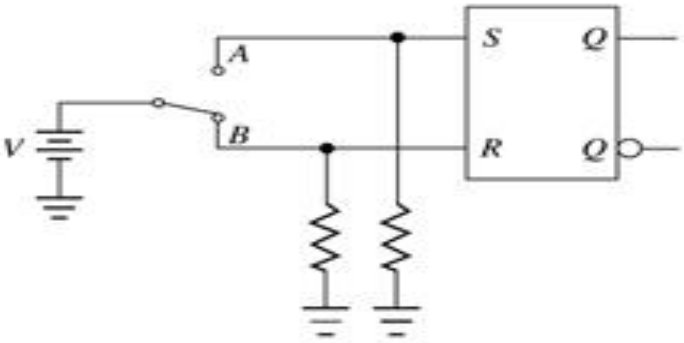
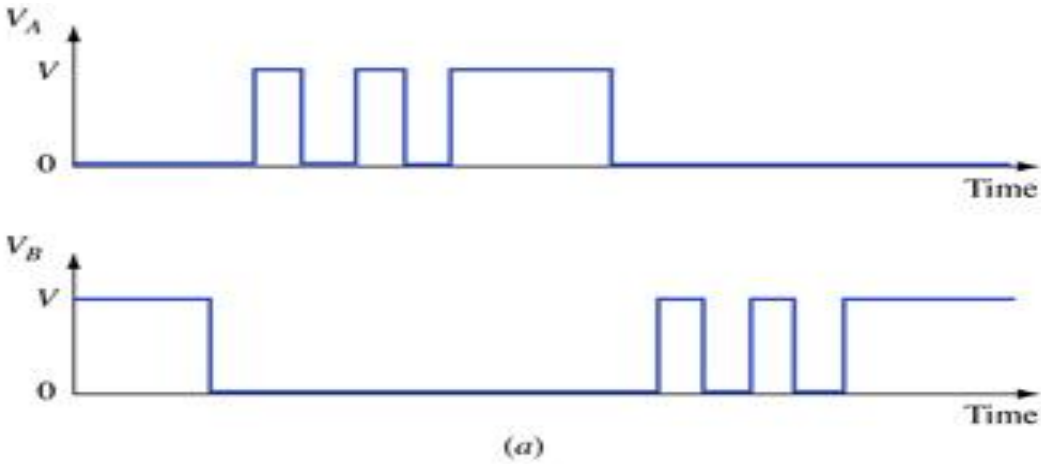
# Application of RS Latch



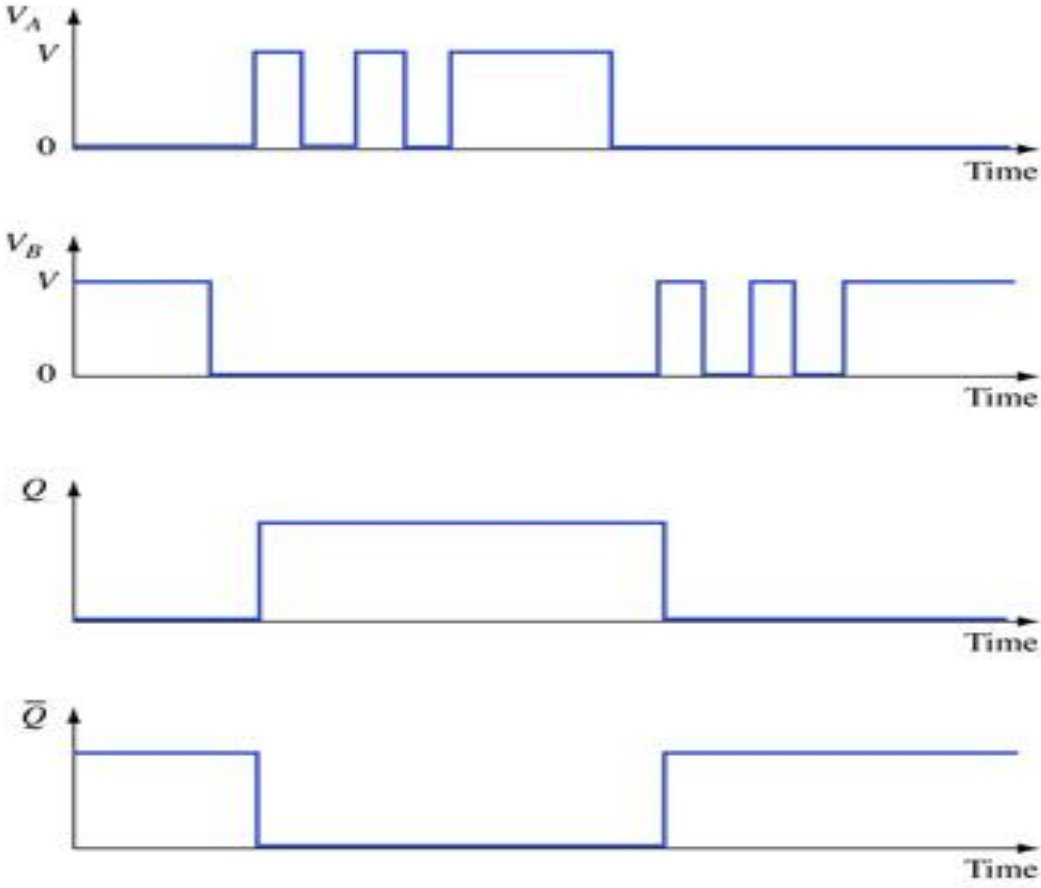

- Effects of Contact Bounce




- A Switch De-bouncer

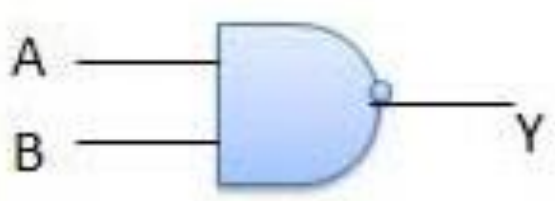



(a)



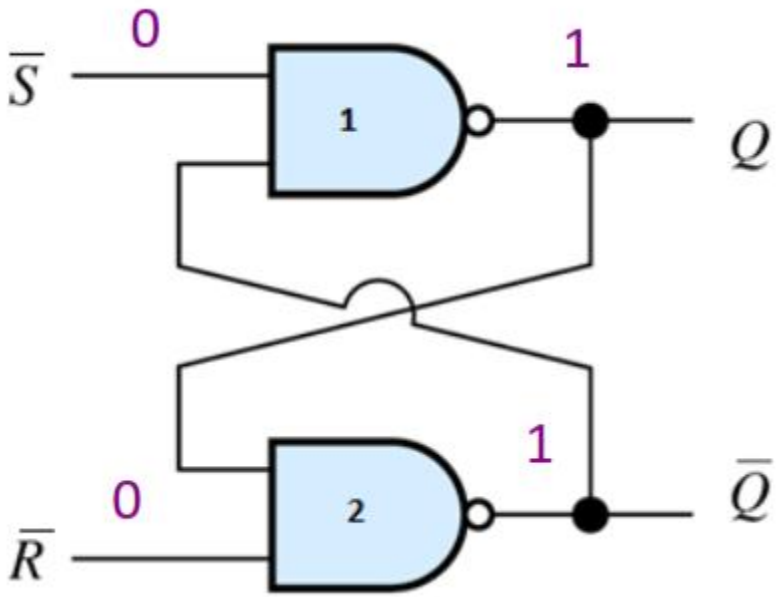

(b)

# Quick Revision
## NAND gate & Truth Table:



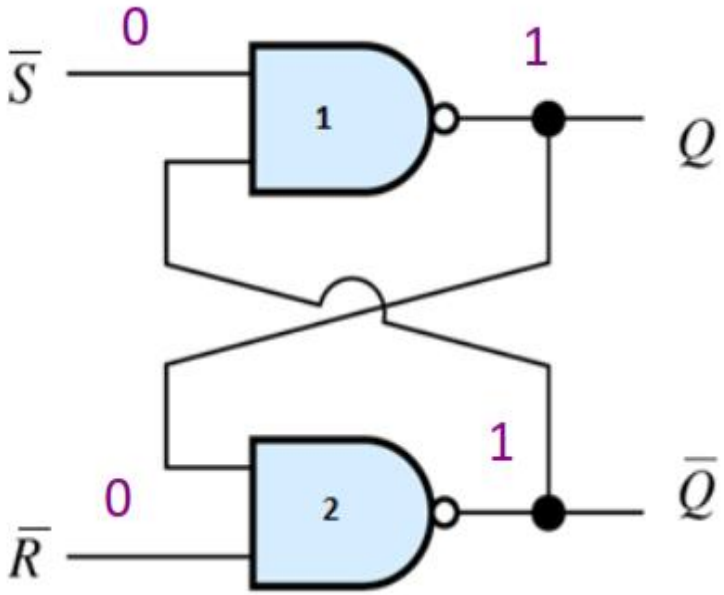

| Inputs | | Output |
|---|---|---|
| A | B | $\overline{AB}$ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# S'R' Latch
# Circuit: INVALID Mode



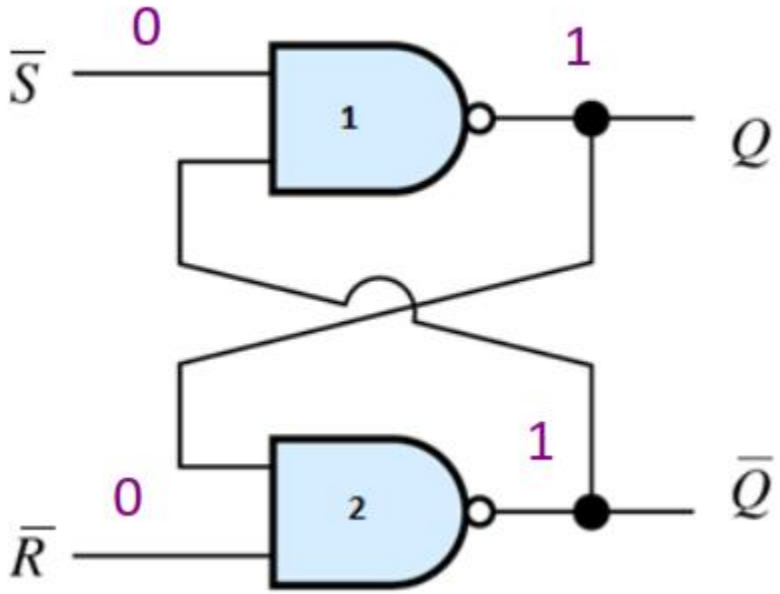

- The analysis of a SR Flip Flop NAND:
- **S = 0, R = 0**; This condition tries to set and reset the NAND gate latch at the same time.
- It produces Q = Q' =1

# S'R' Latch
# Circuit: INVALID Mode




- This is an unexpected condition, since the two outputs should be inverses of each other.
- If the inputs are returned to 1 simultaneously, the output states are unpredictable.
- This input condition should not be used and when circuits are constructed, the designer should make sure that this condition. S=R=0 never arises. It is called INVALID/ PROHIBITED

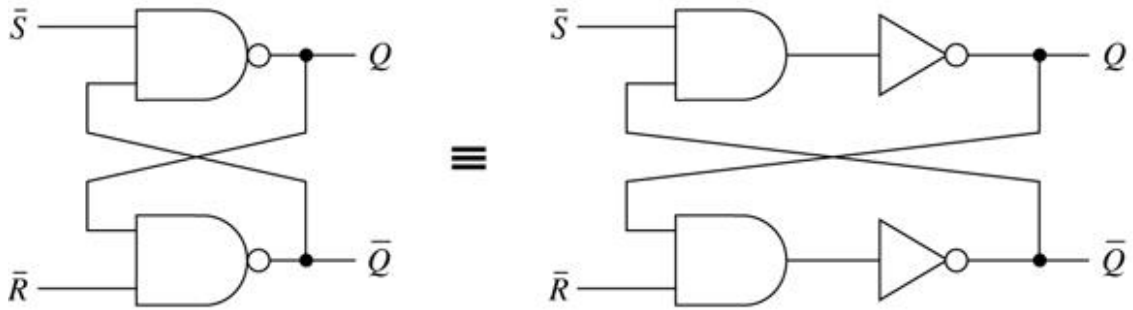
# S'R' Latch
# Circuit: INVALID Mode




| S̄R̄-FLIP-FLOP | | | |
|---|---|---|---|
| R̄ | S̄ | Q | Q̄ |
| 0 | 0 | Illegal | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

# $\overline{S}\,\overline{R}$ Latch

- Consists of two cross-coupled NAND gates.
- 2 active low inputs and 2 outputs $[Q\ ,\overline{Q}]$

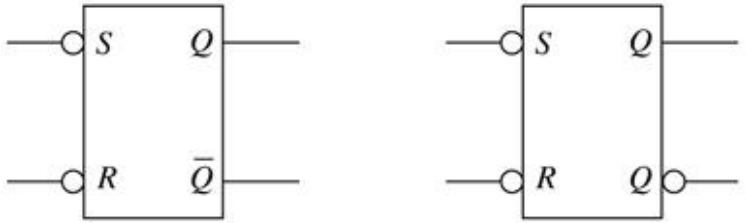



(a)

| Inputs | | Outputs | |
|---|---|---|---|
| $\bar{S}$ | $\bar{R}$ | $Q^+$ | $\bar{Q}^+$ |
| 0 | 0 | 1* | 1* |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | $Q$ | $\bar{Q}$ |

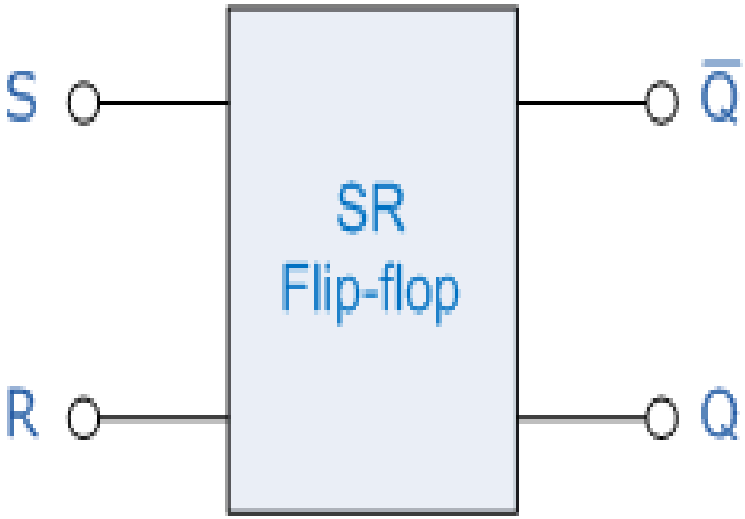
*Unpredictable behavior will result if inputs return to 1 simultaneously

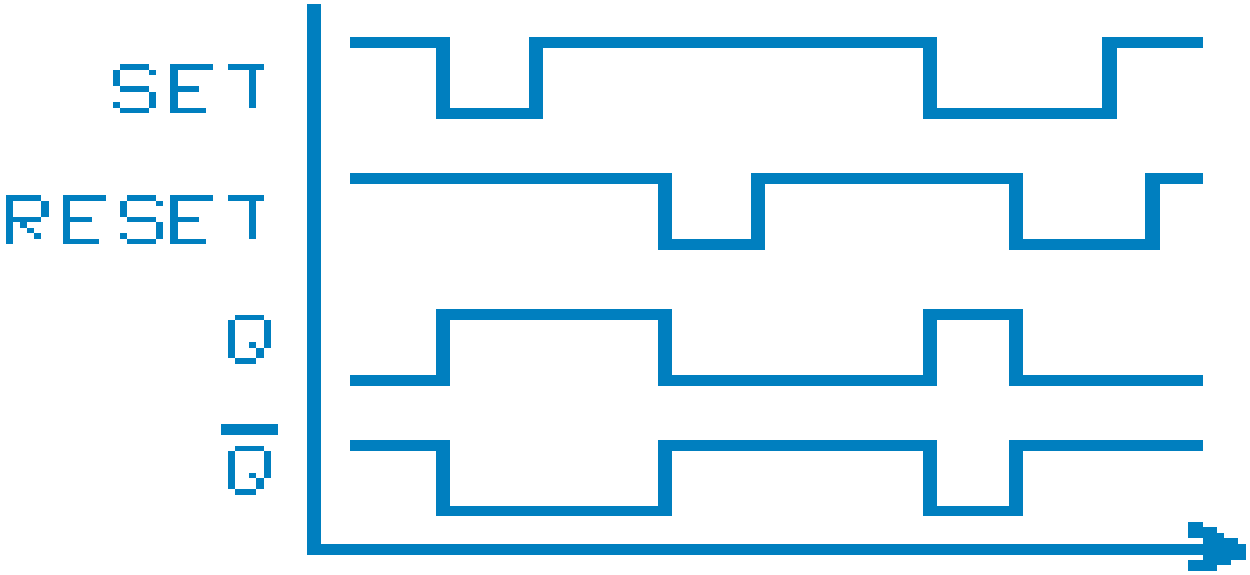
(b)




(c)

# Timing diagram for S'R' LATCH

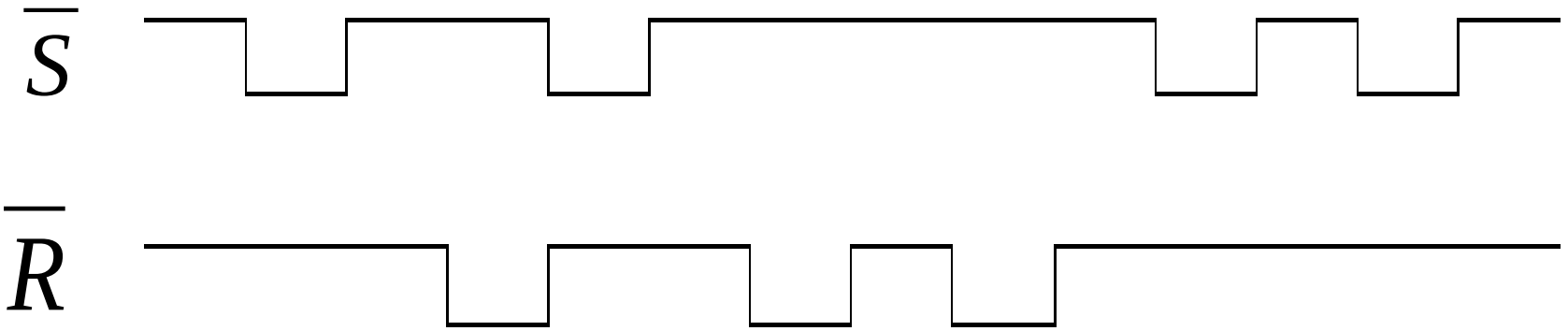


# FUNCTION OF SEQUENTIAL LOGIC

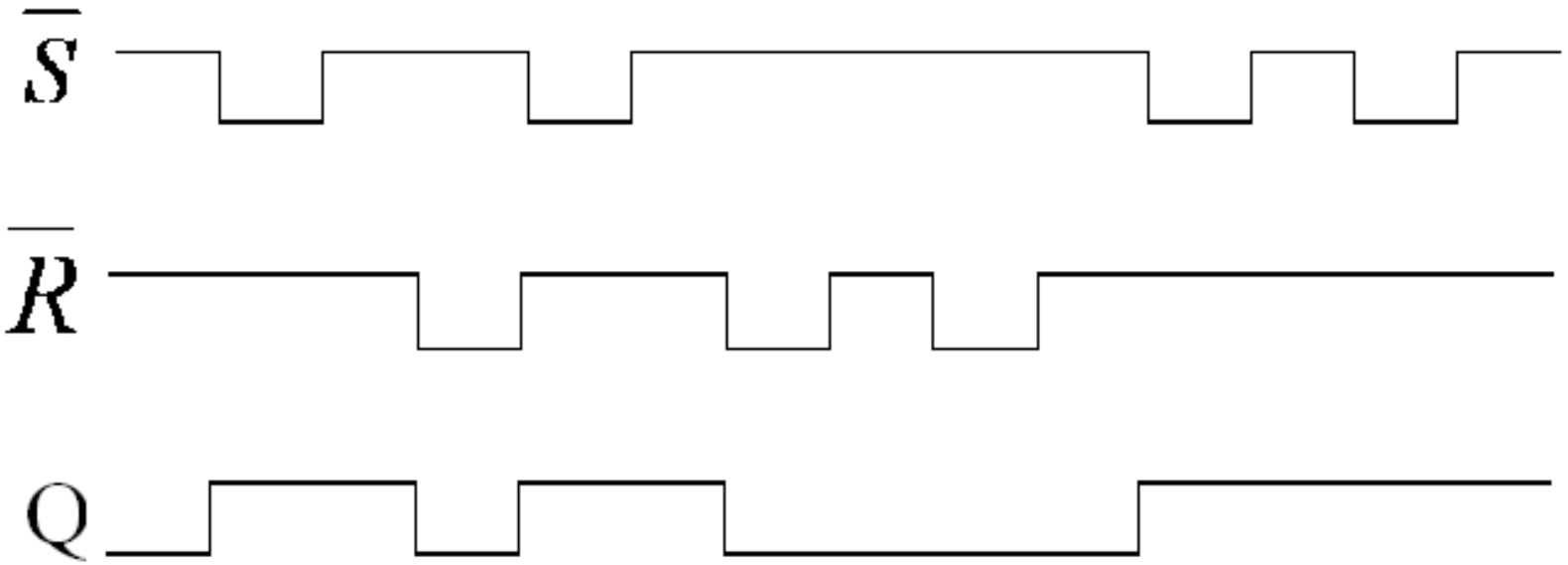
- Example:

  For a given waveform, sketch the output waveform of an active-LOW SR latch.



# FUNCTION OF SEQUENTIAL LOGIC

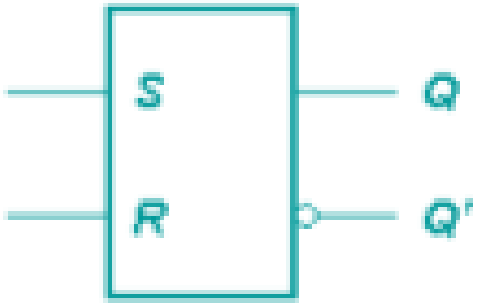
- Solution:



# SR Latch

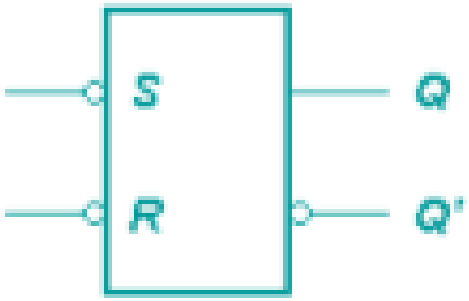
- SR with active HIGH input

| S | R | Q | Q' | |
|---|---|---|---|---|
| 0 | 0 | NC | NC | No change. Latch remained in present state. |
| 1 | 0 | 1 | 0 | Latch SET. |
| 0 | 1 | 0 | 1 | Latch RESET. |
| 1 | 1 | 0 | 0 | Invalid condition. |




- S'R' with active LOW input

| S' | R' | Q | Q' | |
|---|---|---|---|---|
| 1 | 1 | NC | NC | No change. Latch remained in present state. |
| 0 | 1 | 1 | 0 | Latch SET. |
| 1 | 0 | 0 | 1 | Latch RESET. |
| 0 | 0 | 1 | 1 | Invalid condition. |



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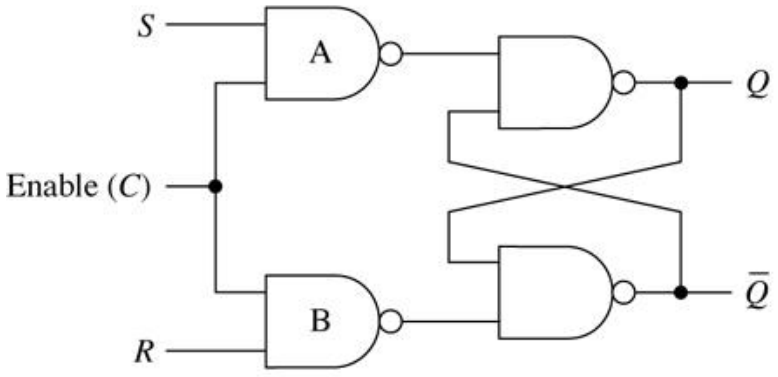
# Gated SR Latch

- Constructed by adding two Controller NAND gates to the

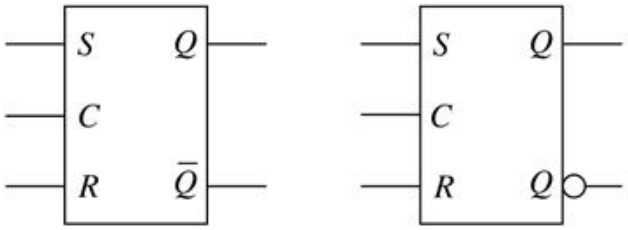


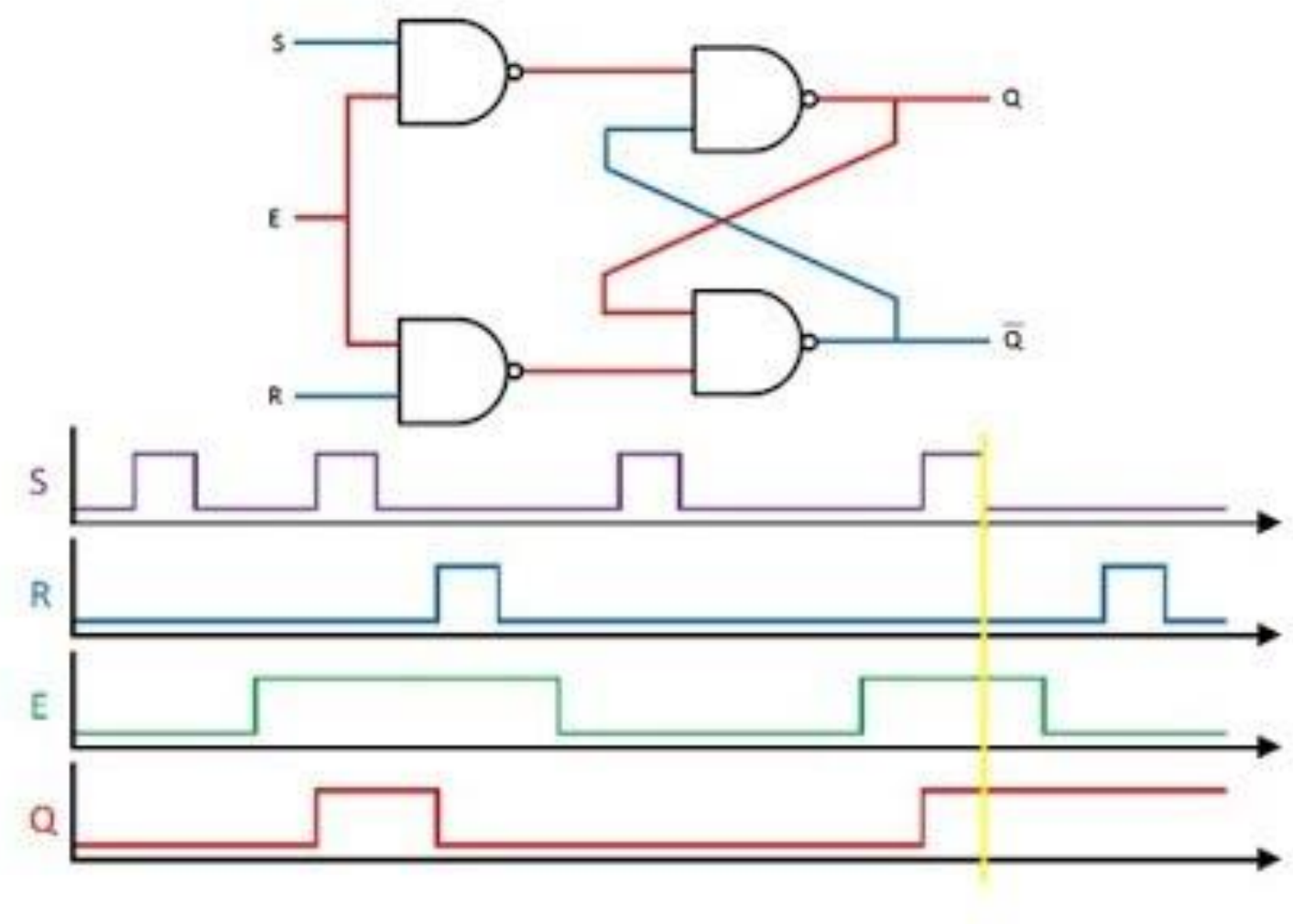

(a)

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $S$ | $R$ | $C$ | $Q^+$ | $\overline{Q}^+$ |
| 0 | 0 | 1 | $Q$ | $\overline{Q}$ |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1* | 1* |
| X | X | 0 | $Q$ | $\overline{Q}$ |

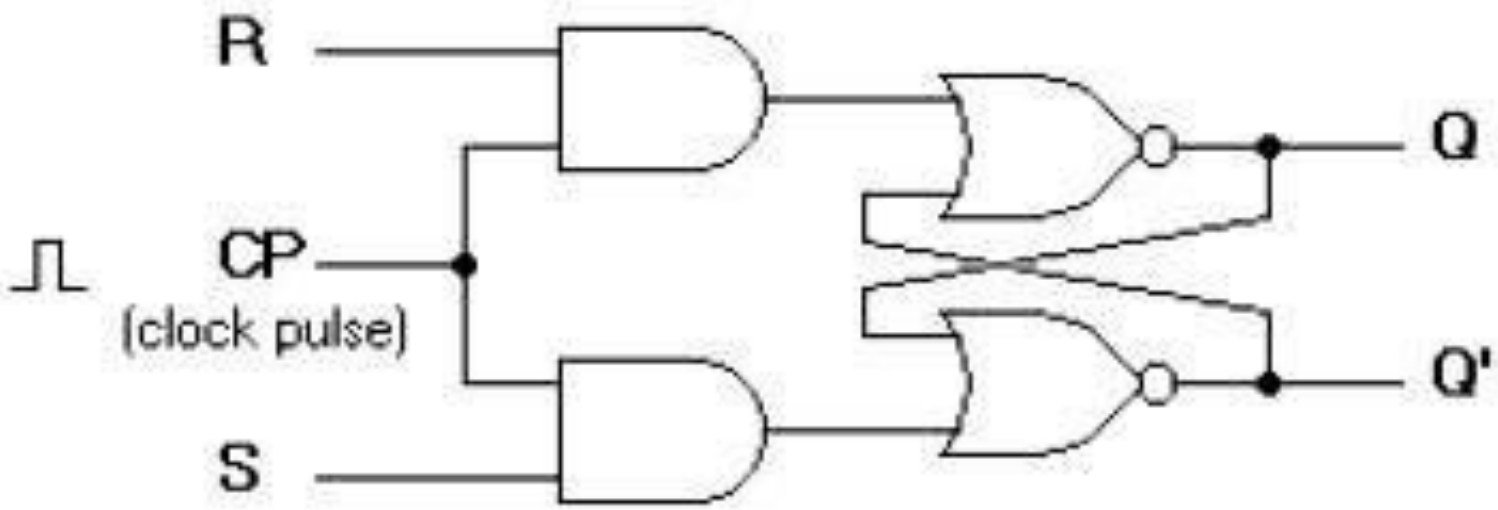
*Unpredictable behavior will result if $S$ and $R$ return to 0 simultaneously or $C$ returns to 0 while $S$ and $R$ are 1

(b)

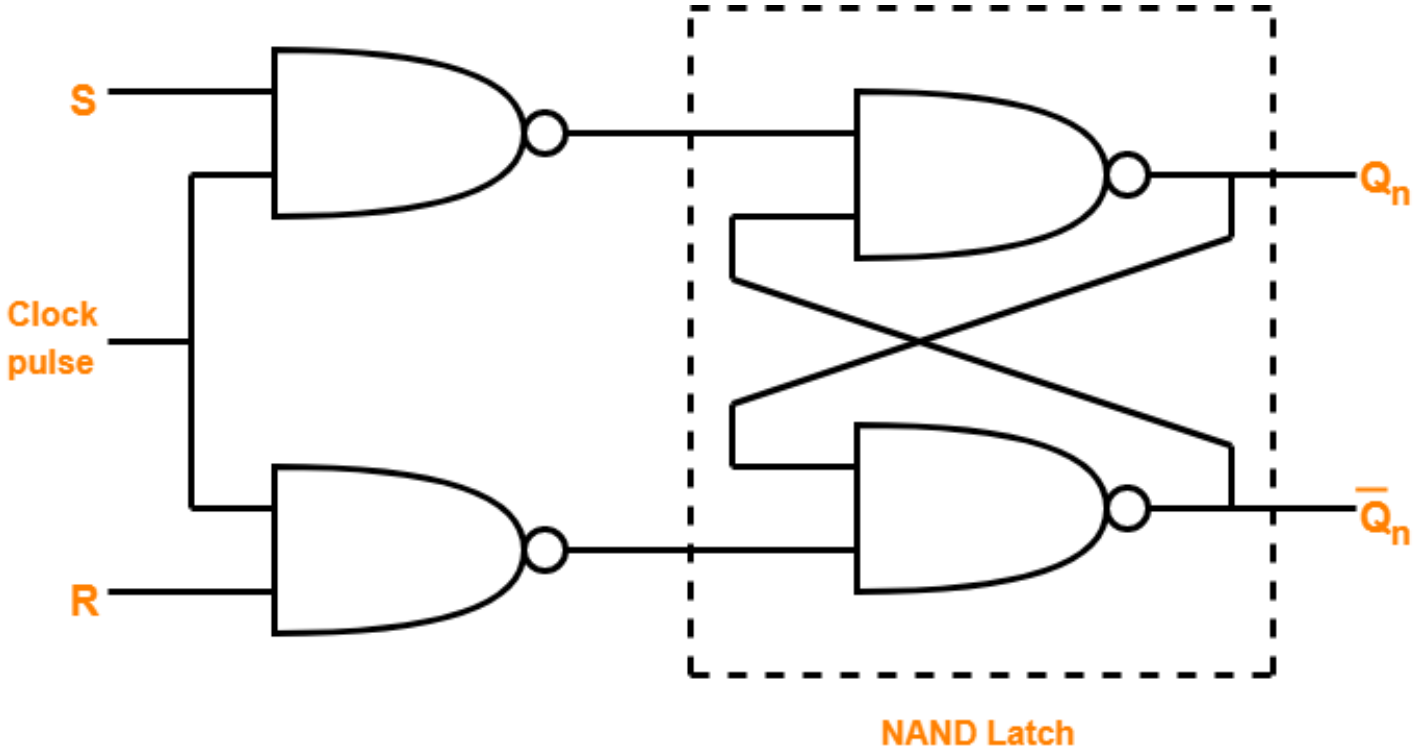



S
E
R
Q
$\overline{Q}$
S
R
E
Q

# RS flip-flop

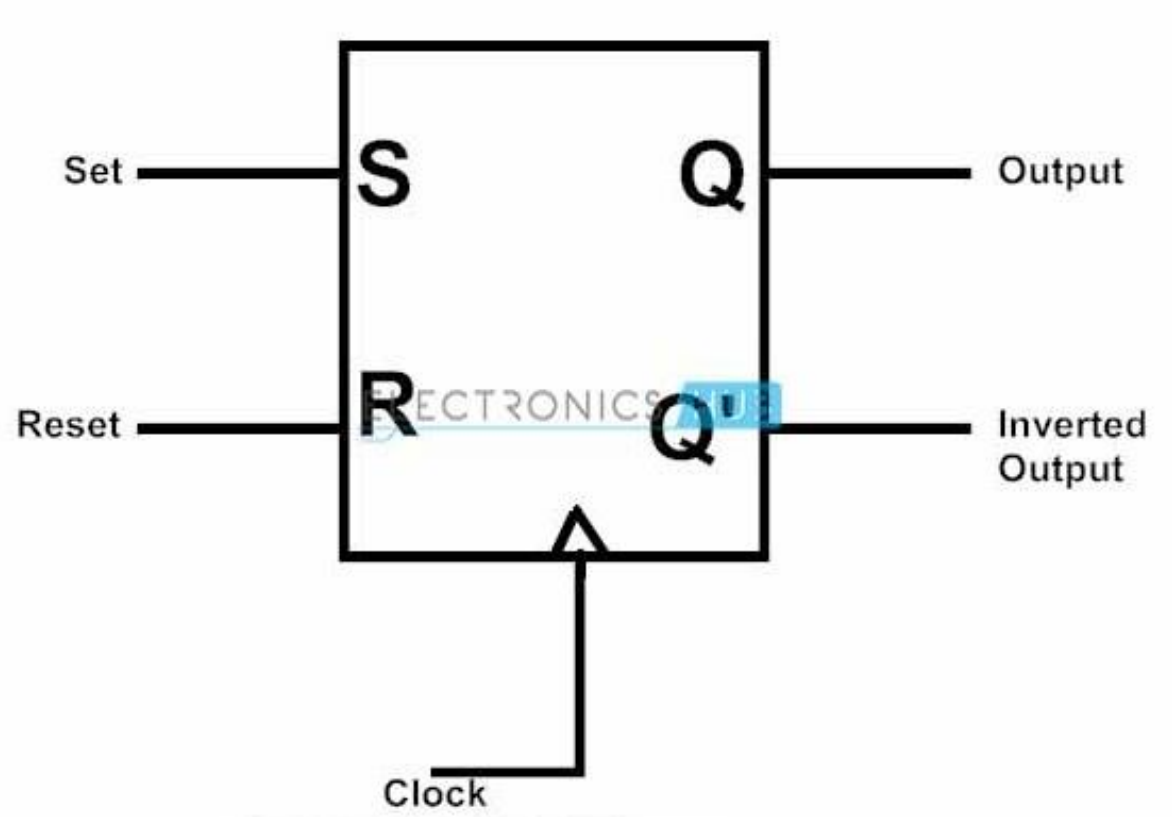


# SR flip-flop



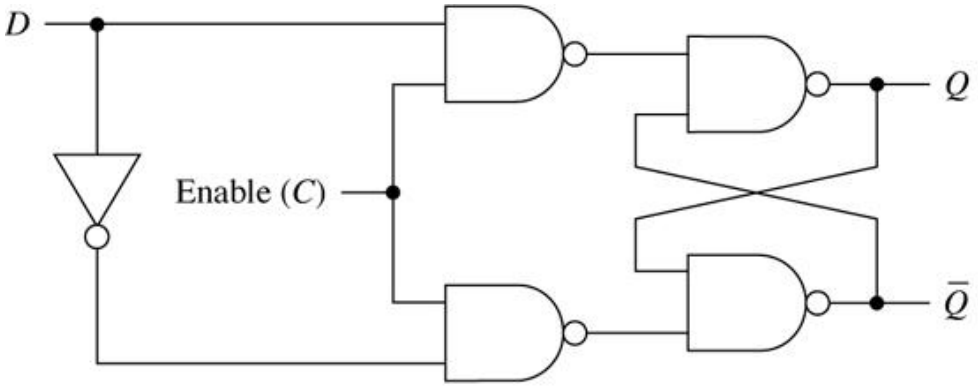

SR Flip Flop Using NAND Latch

# Symbol of SR flip-flop



# Gated D Latch

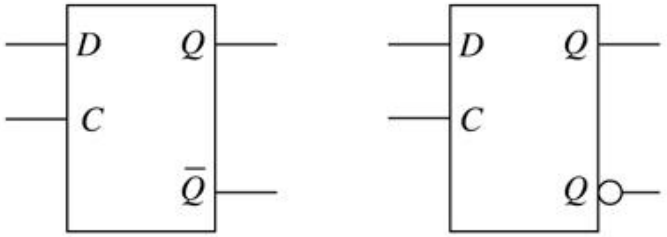
- Designed to eliminate the forbidden input problem
- Single input D and two outputs [$Q$ , $\overline{Q}$]




(a)

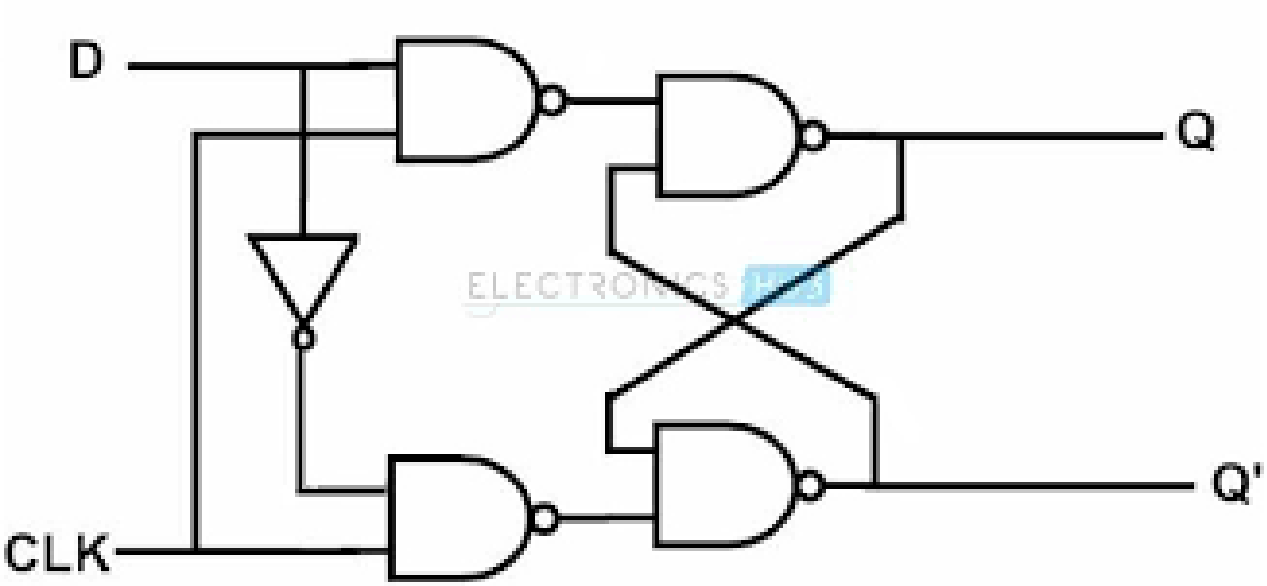
| Inputs | | Outputs | |
|---|---|---|---|
| $D$ | $C$ | $Q^+$ | $\overline{Q}^+$ |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| X | 0 | $Q$ | $\overline{Q}$ |

(b)

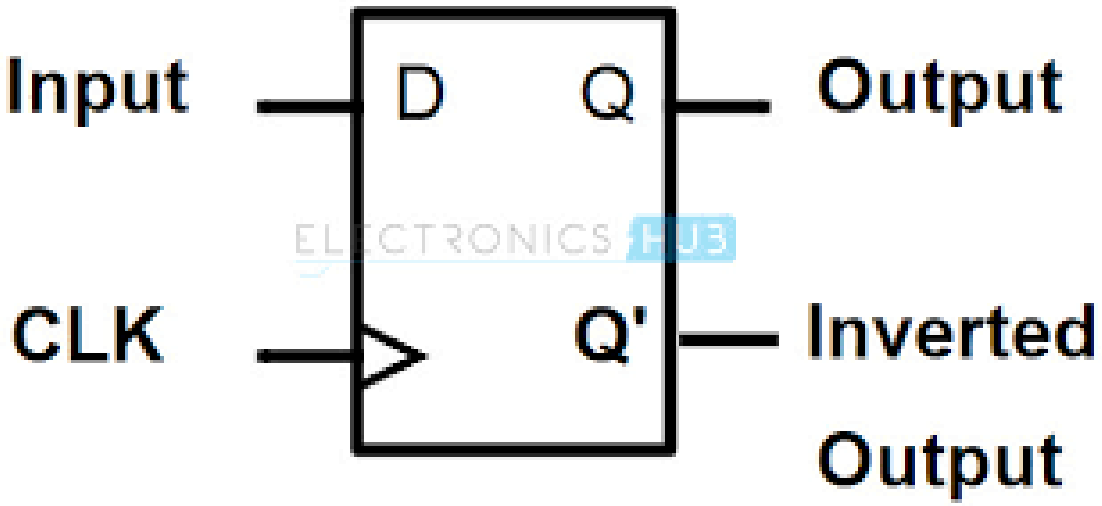



(c)

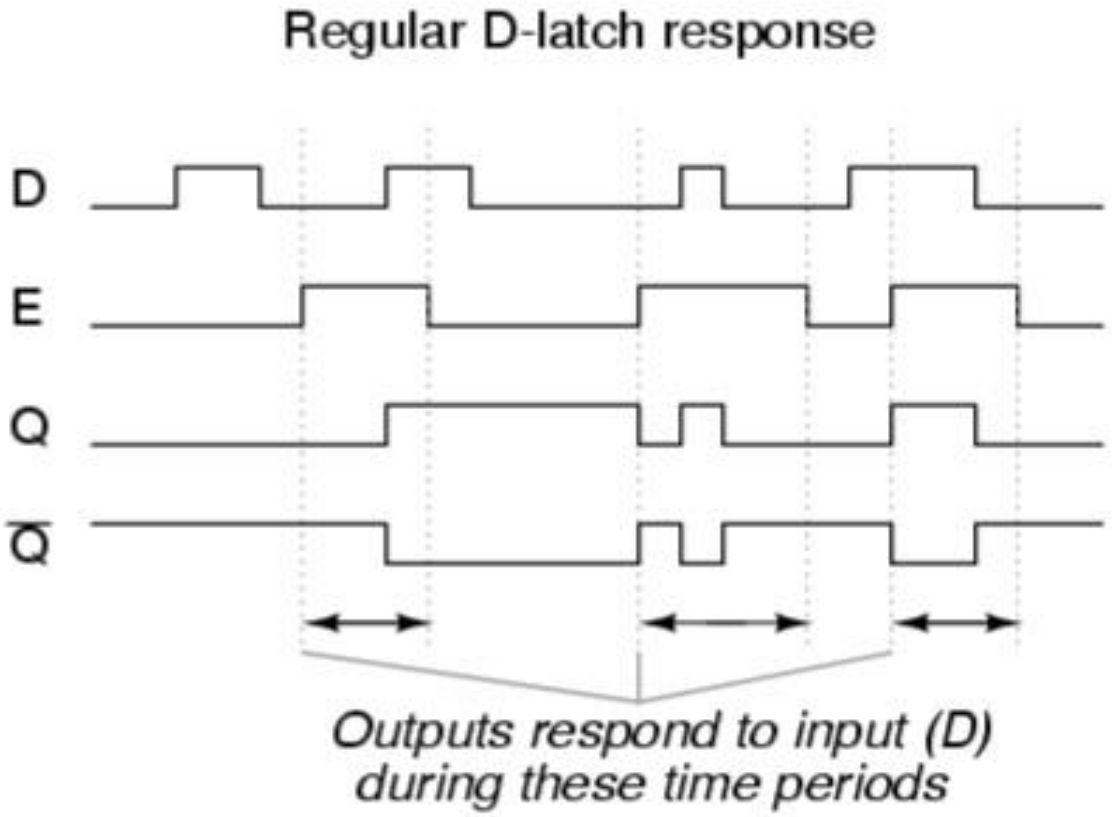
# D flip-flop



# Symbol of D flip-flop



# Timing Diagram



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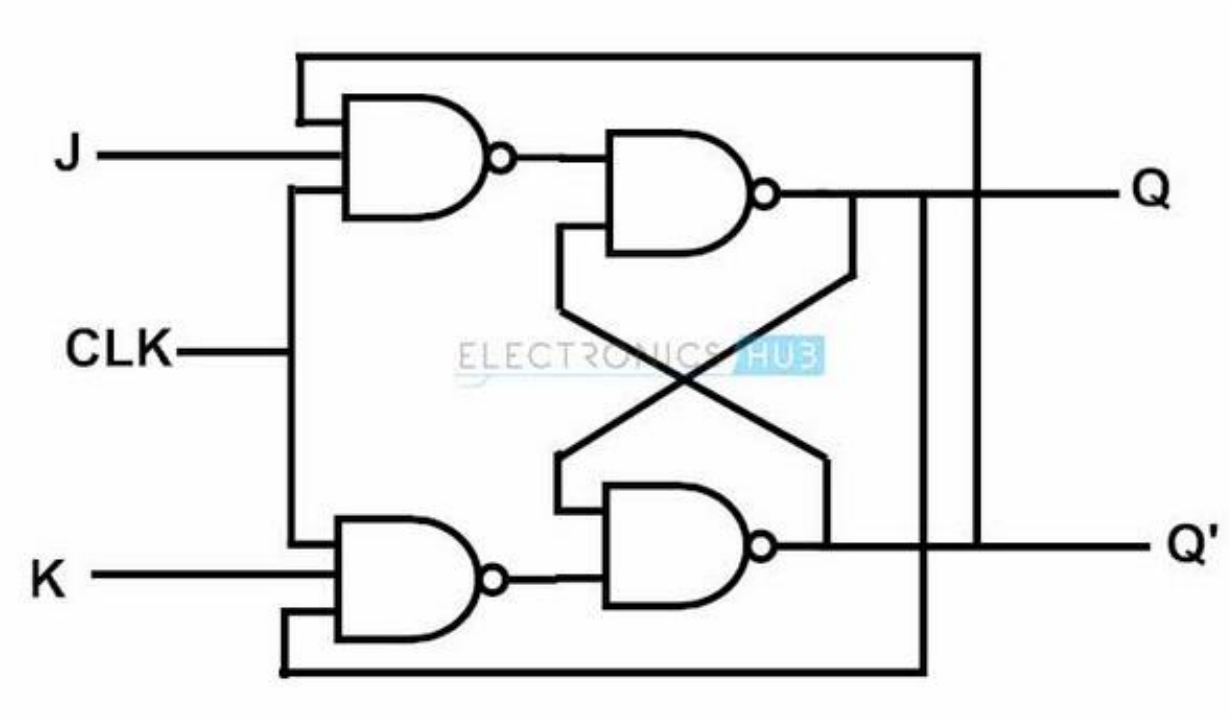
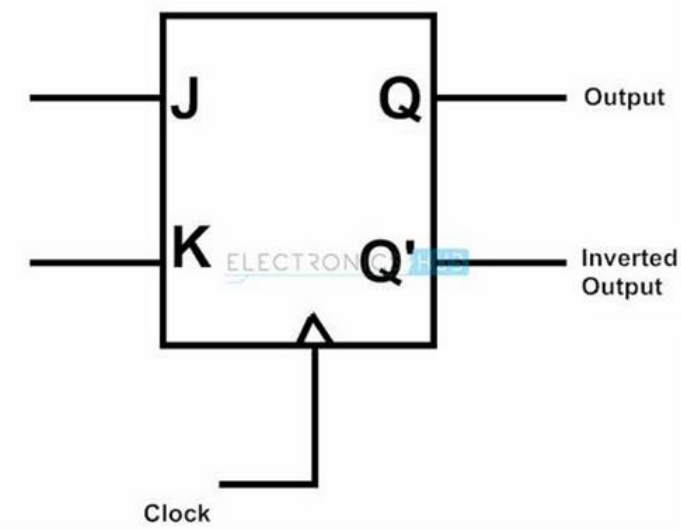
# Clocked JK Flip Flop






# Truth Table

| Clk | J | K | $Q^+$ | $\bar{Q}^+$ |
|---|---|---|---|---|
| 0 | X | X | Q | $\bar{Q}$ |
| 1 | 0 | 0 | Q | $\bar{Q}$ |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | $\bar{Q}$ | Q |

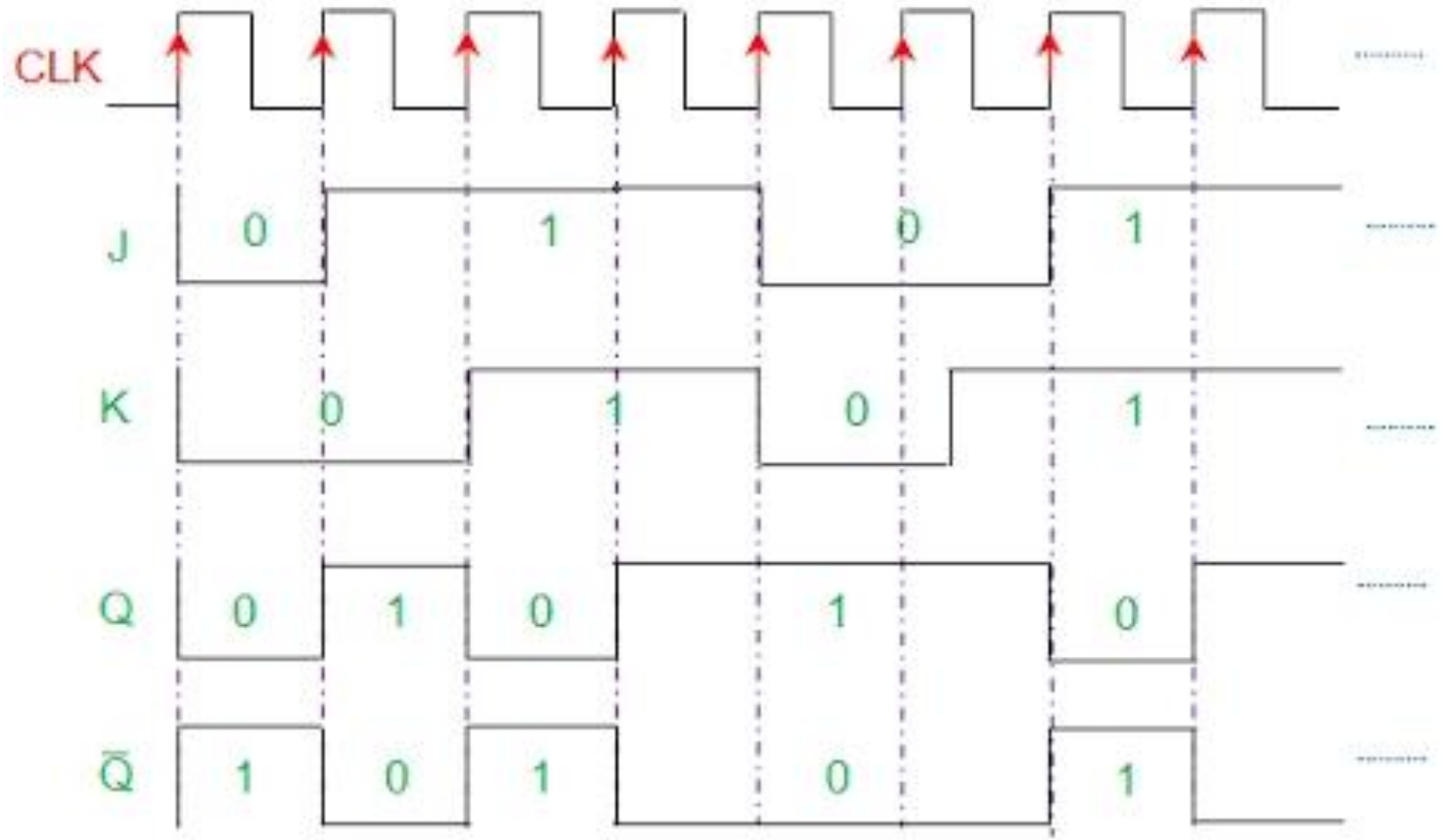
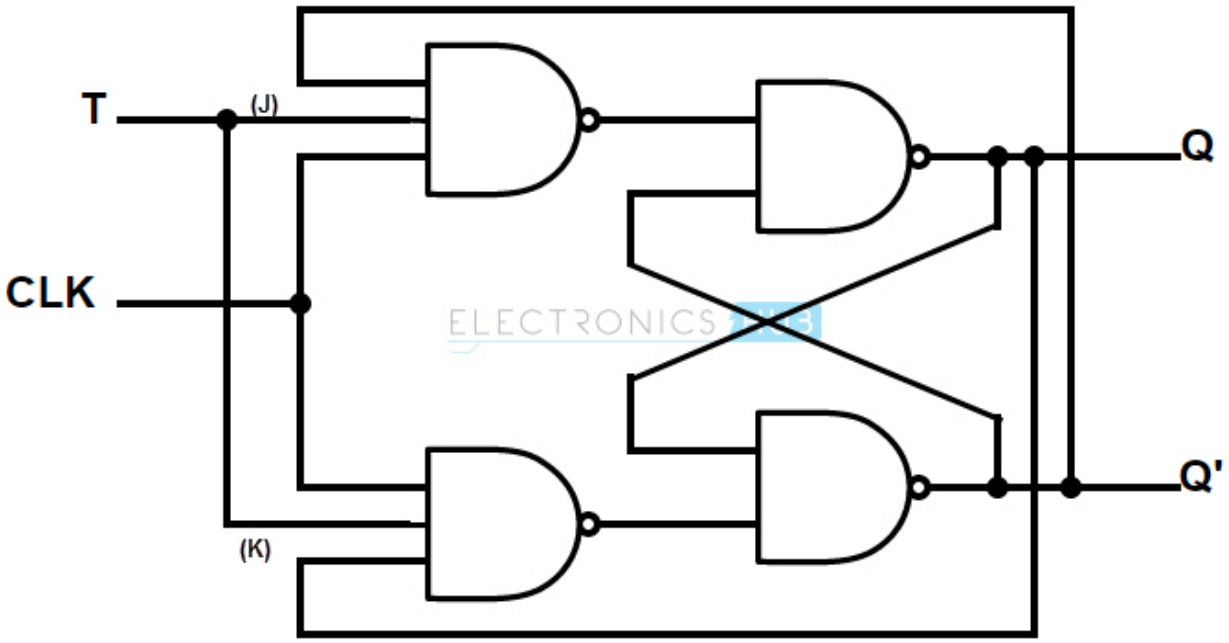
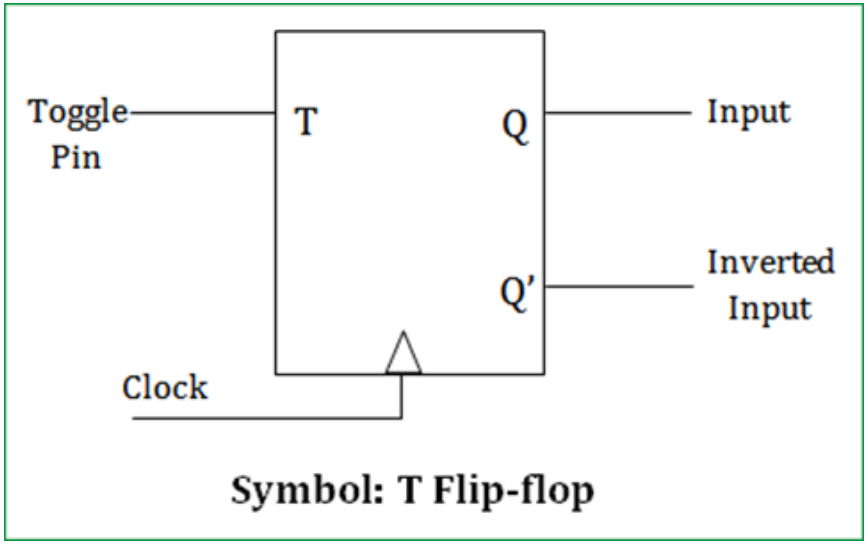



Figure 3 Timing diagram for positive edge-triggered JK flip-flop

# Clocked T-Flip Flop



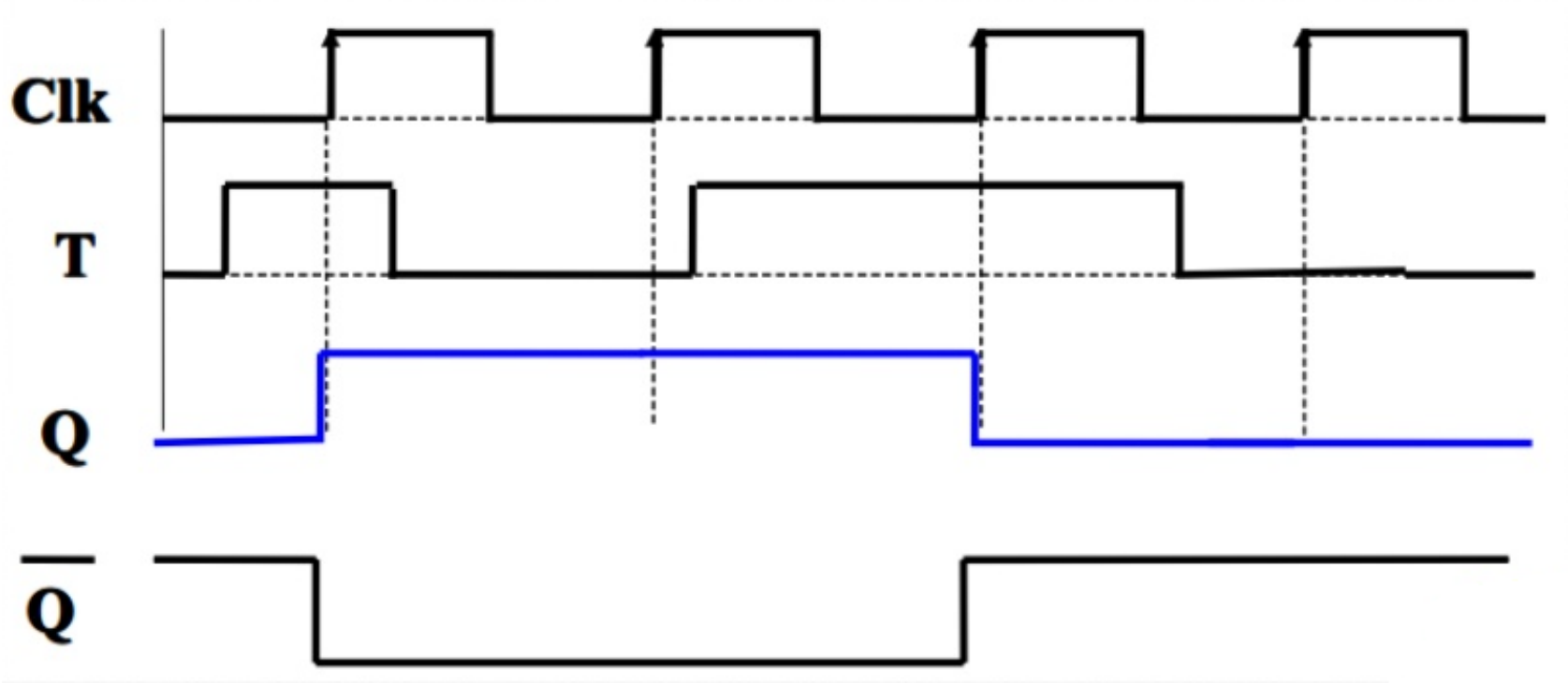



Symbol: T Flip-flop

## Truth Table

| Clk | T | $Q^+$ | $\bar{Q}^+$ |
|---|---|---|---|
| 0 | X | Q | $\bar{Q}$ |
| 1 | 0 | Q | $\bar{Q}$ |
| 1 | 1 | $\bar{Q}$ | Q |

# Timing diagram



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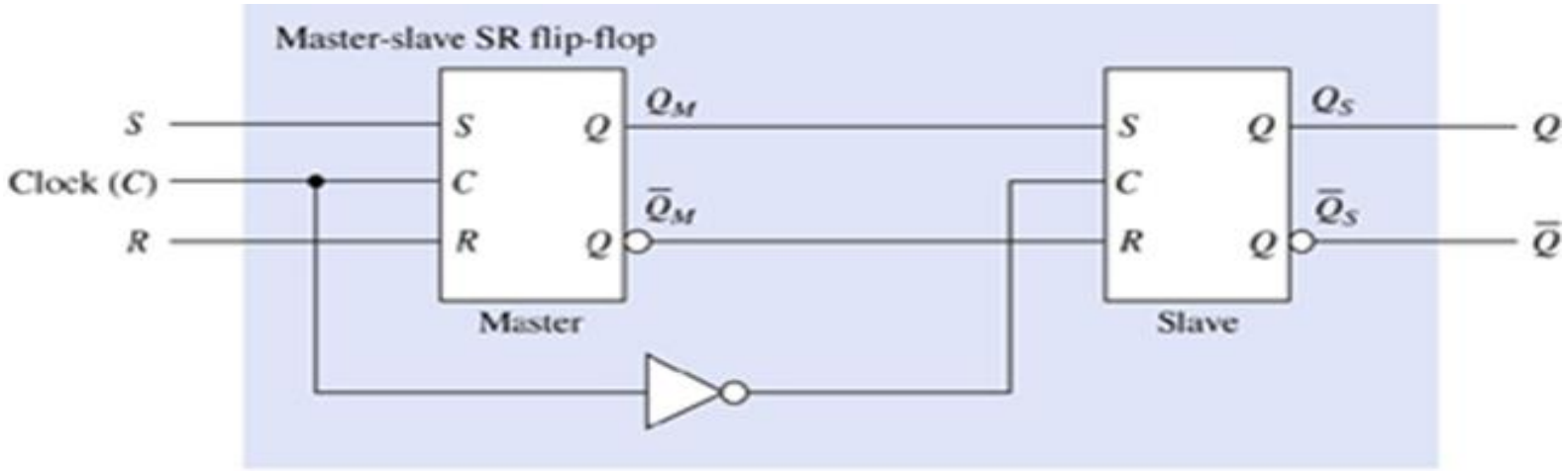
# Master-Slave Flip-Flops

- Also known as pulse-triggered flip-flops
- Necessary in case where it is necessary to sense current state while allowing new state information to be entered.
- It consists of two cascaded sections.
- First section is the master and the second is the slave
- Information is entered into the master on one edge or level of a control signal and is transferred to the slave on the next edge or level of control signal

# Master slave SR Flip-flop




(a)


(b)

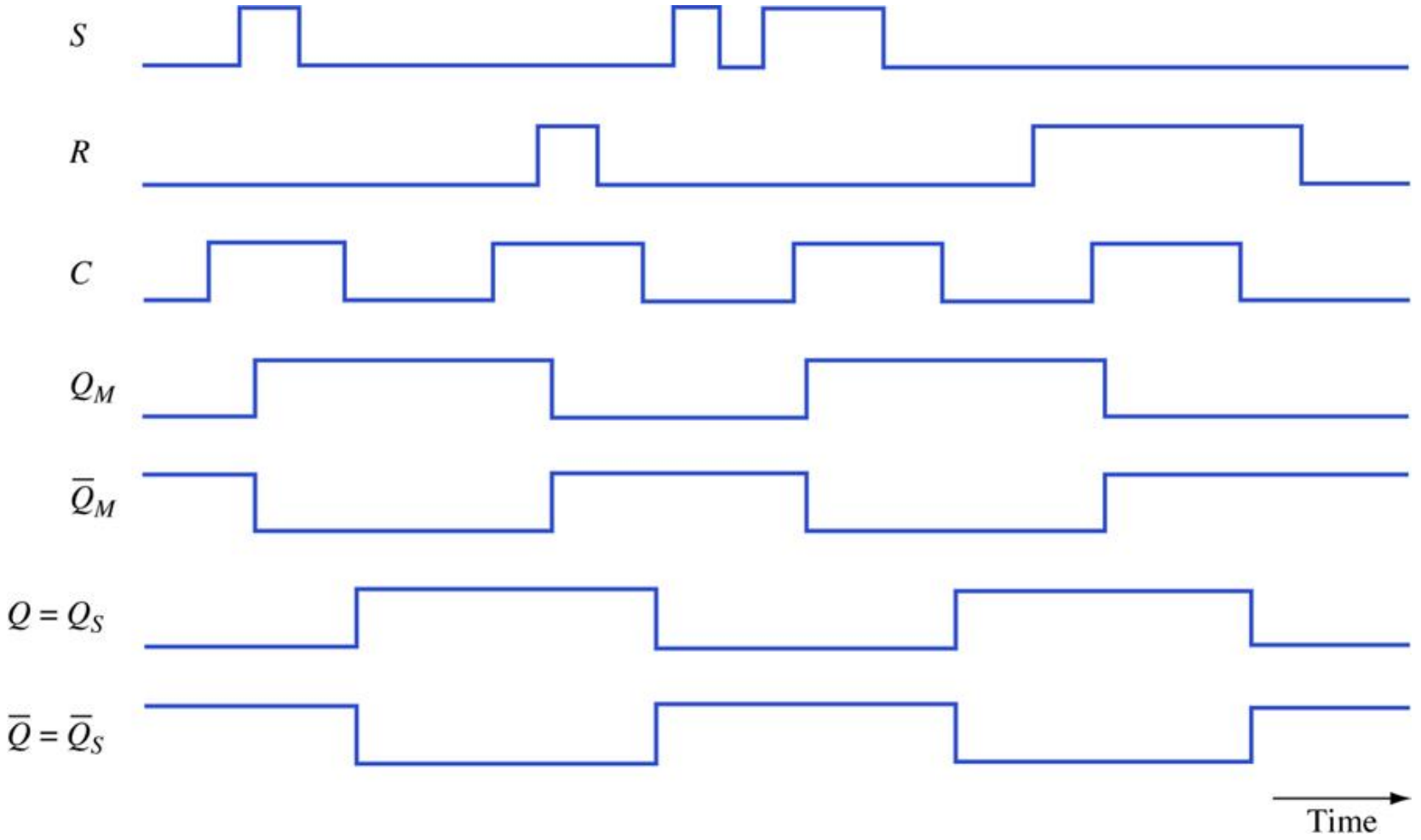
# Master slave SR Flip-flop

- Constructed from two gated SR latches and an inverter.
- Timing behaviour is referenced to the control line

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $S$ | $R$ | $C$ | $Q^+$ | $\overline{Q}^+$ |
| 0 | 0 |  | $Q$ | $\overline{Q}$ |
| 0 | 1 |  | 0 | 1 |
| 1 | 0 |  | 1 | 0 |
| 1 | 1 |  | Undefined | Undefined |
| X | X | 0 | $Q$ | $\overline{Q}$ |

(c)

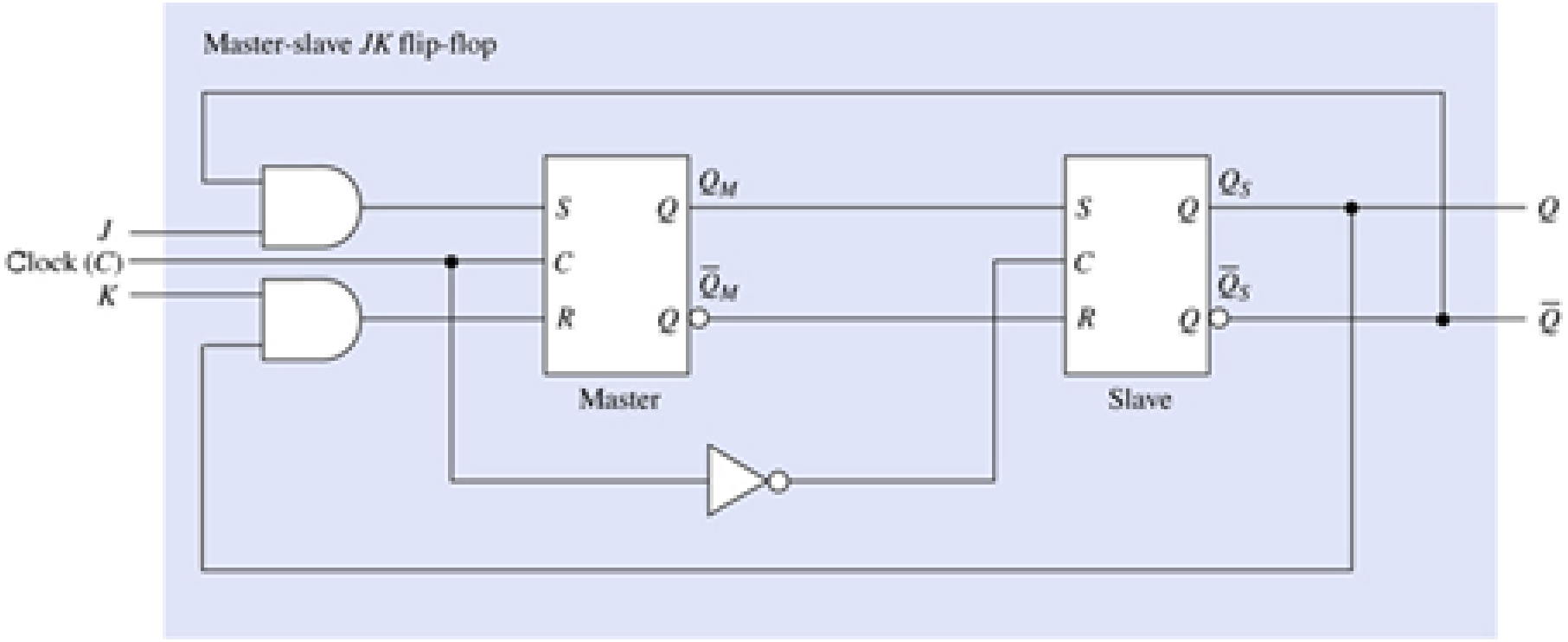
# Timing Diagram for MS SR Flip-Flop



# Master-Slave JK Flip-Flop

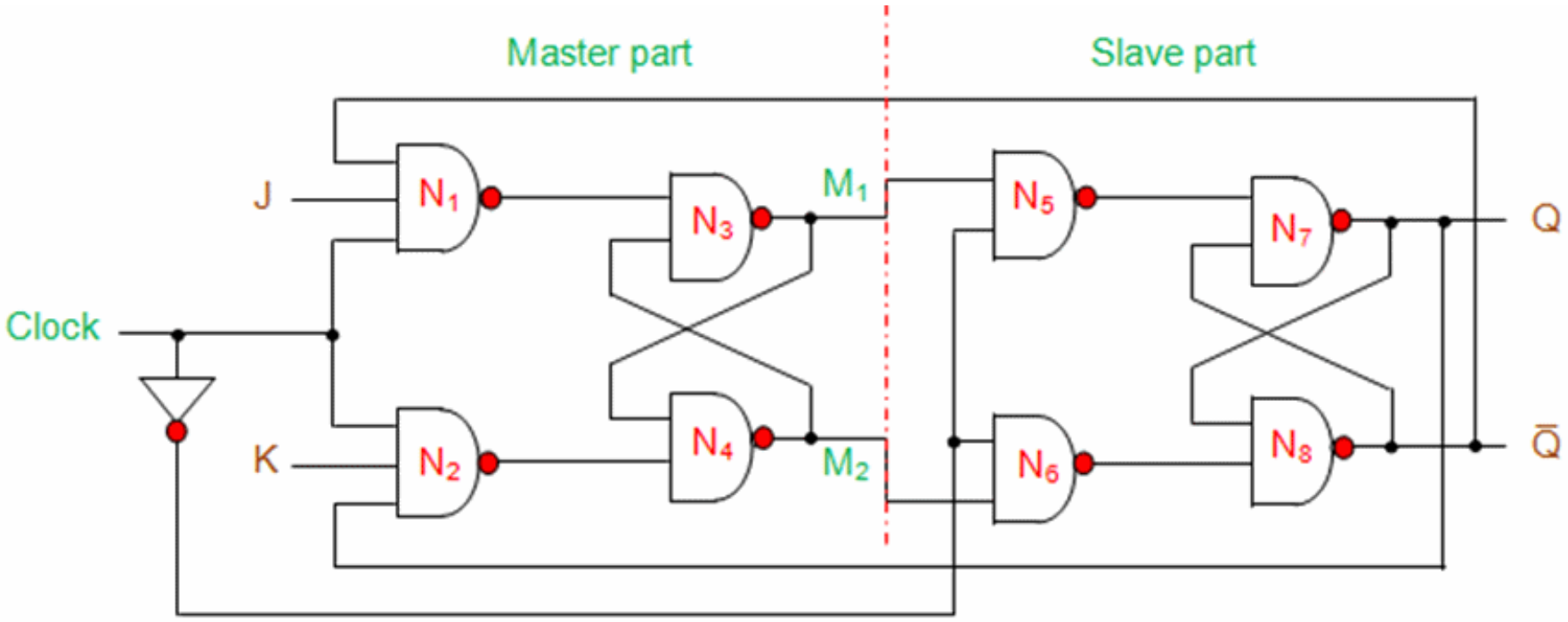
- In this J corresponds to S and K corresponds to R inputs.
- J=K=1 causes the flip-flop to toggle from the current state.
  - If present state is 1 then next state is 0
  - If present state is 0 then next state is 1
- In this 2 AND gates are used to sense and steer the state of the slave [in addition to SR MS flip-flop]

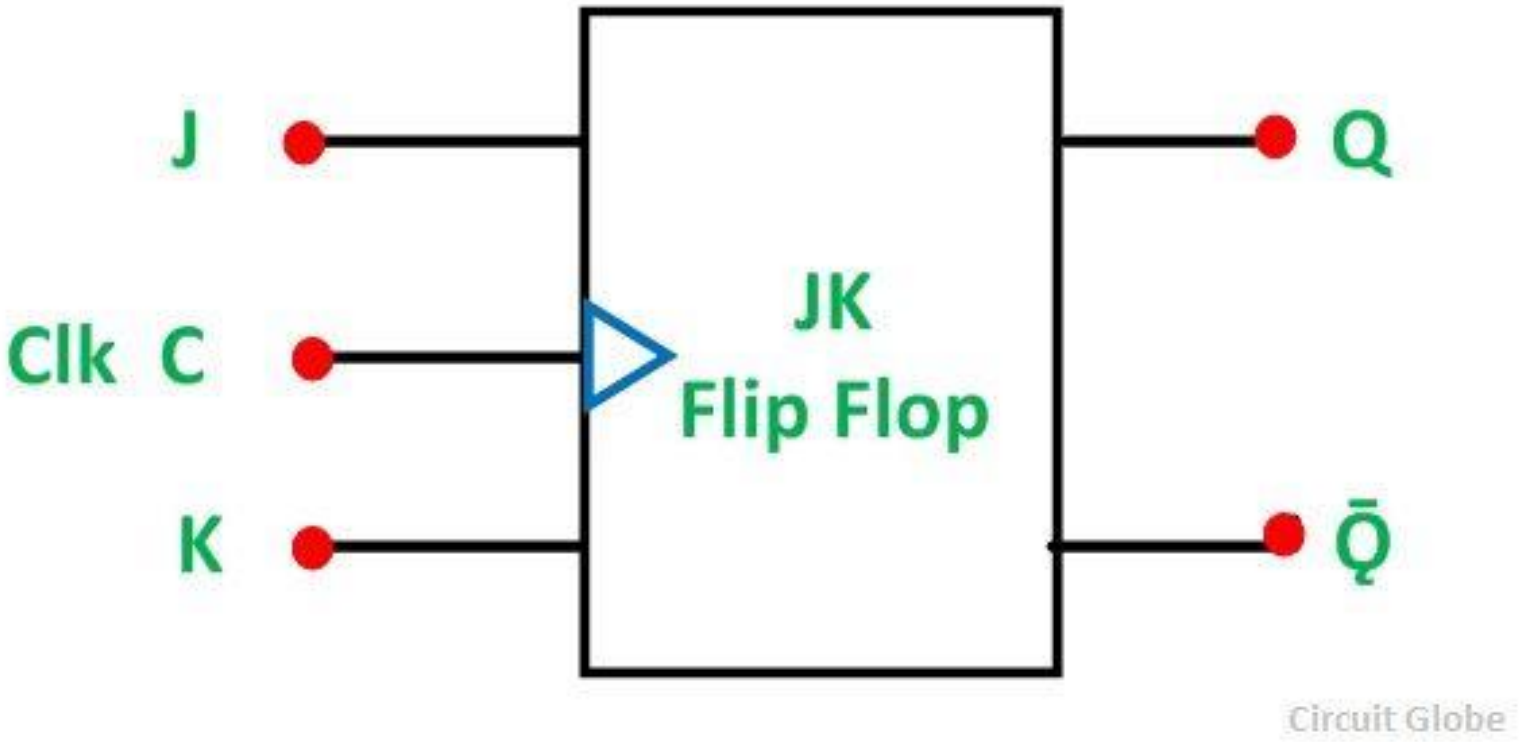
# Master-Slave JK Flip-Flop




(a)

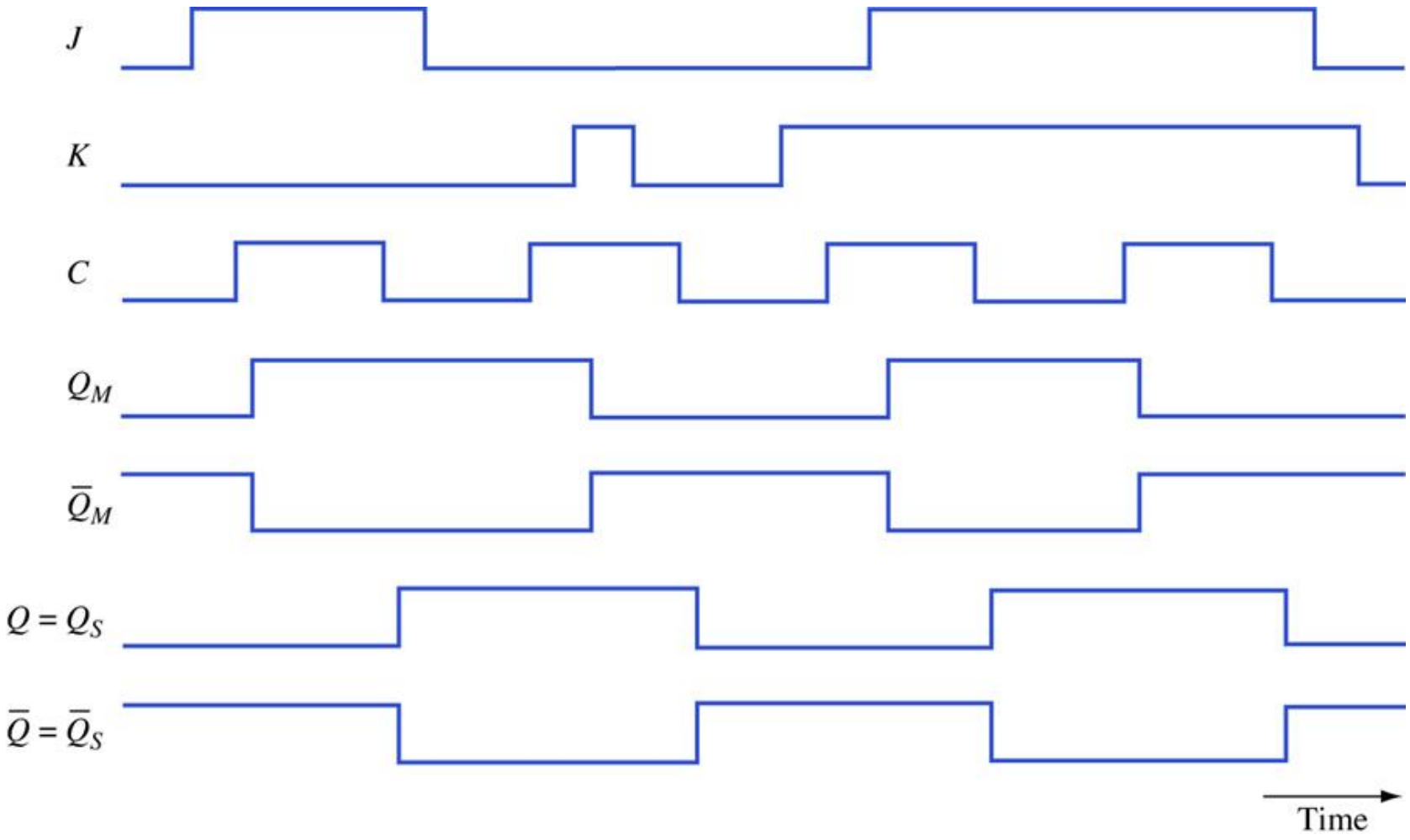
# Master Slave Flip Flop using NAND gates




J
Clk C
K
JK
Flip Flop
Q
Q̄
Circuit Globe

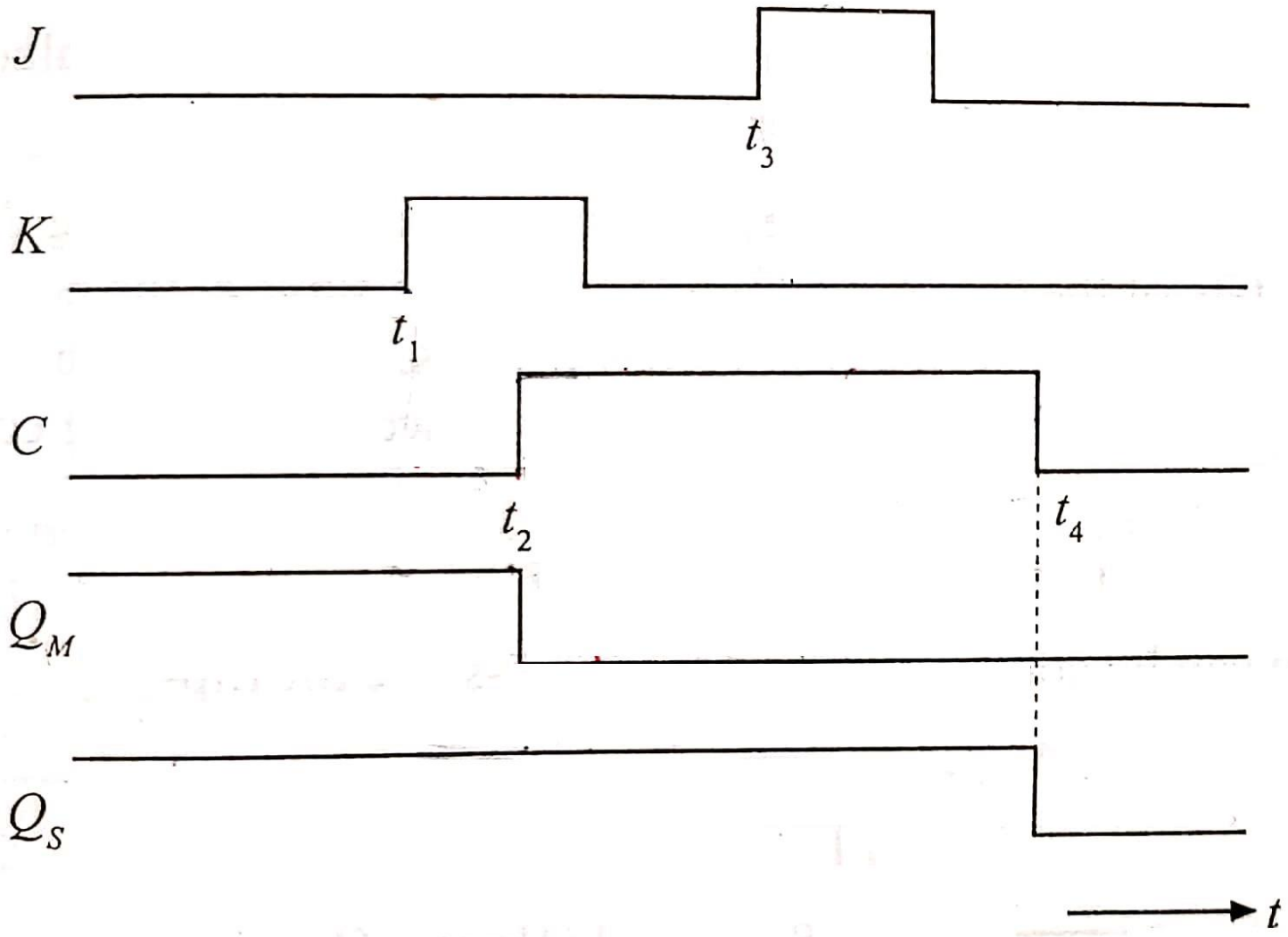
| J | K | CLK | $Q$ | $\overline{Q}$ | *Comment* |
|---|---|---|---|---|---|
| 0 | 0 | ↑ | $Q$ | $\overline{Q}$ | Latch |
| 1 | 0 | ↑ | 1 | 0 | SET |
| 0 | 1 | ↑ | 0 | 1 | RESET |
| 1 | 1 | ↑ | $\overline{Q}$ | $Q$ | TOGGLE |
| X | X | *Any Thing Else* | $Q$ | $\overline{Q}$ | *NO Change !* |

# Timing Diagram for JK MS Flip-Flop



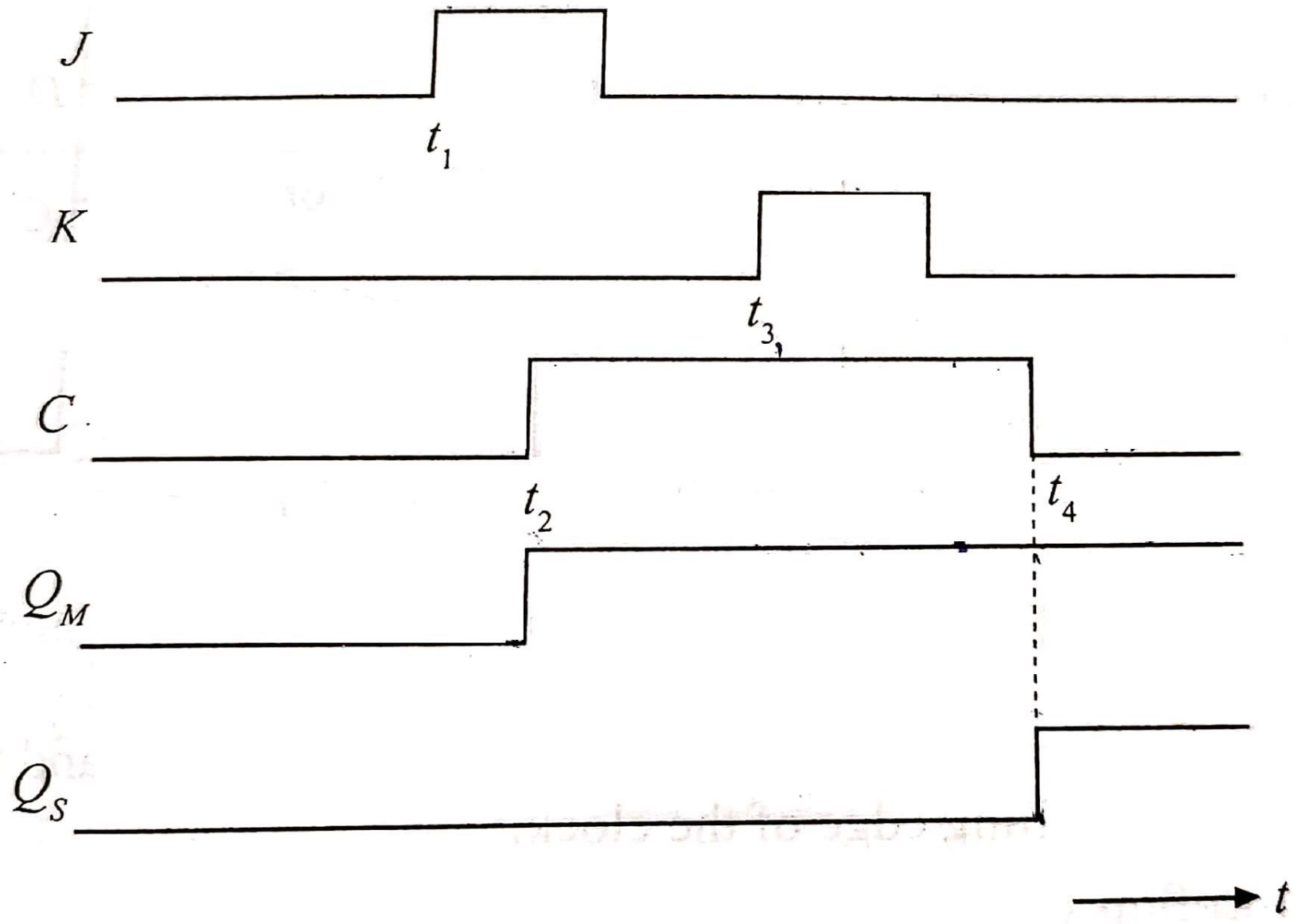
# 0's catching

- Master Latch is enabled during the entire period the control signal is 1.
  - Latch is in its 1-state, then logic-1 on K input causes the master to reset, subsequently resulting in slave reset when control signal returns to 0.
  - Once the master latch is reset, a subsequent logic-1 signal on J input during the same period in which C=1 cannot set the master.
  - This is known as 0's catching


J
t3
K
t1
C
t2
t4
QM
QS
t

# 1’s catching

- Master Latch is enabled during the entire period the control signal is 1.
  - Latch is in its 0-state, then logic-1 on J input causes the master to set, subsequently resulting in slave being set when control signal returns to 0.
  - Once the master latch is set, a subsequent logic-1 signal on K input during the same period in which C=1 cannot set the master.
  - This is known as 1’s catching


J
t1
K
t3
C
t2
t4
QM
QS
t

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# Triggering

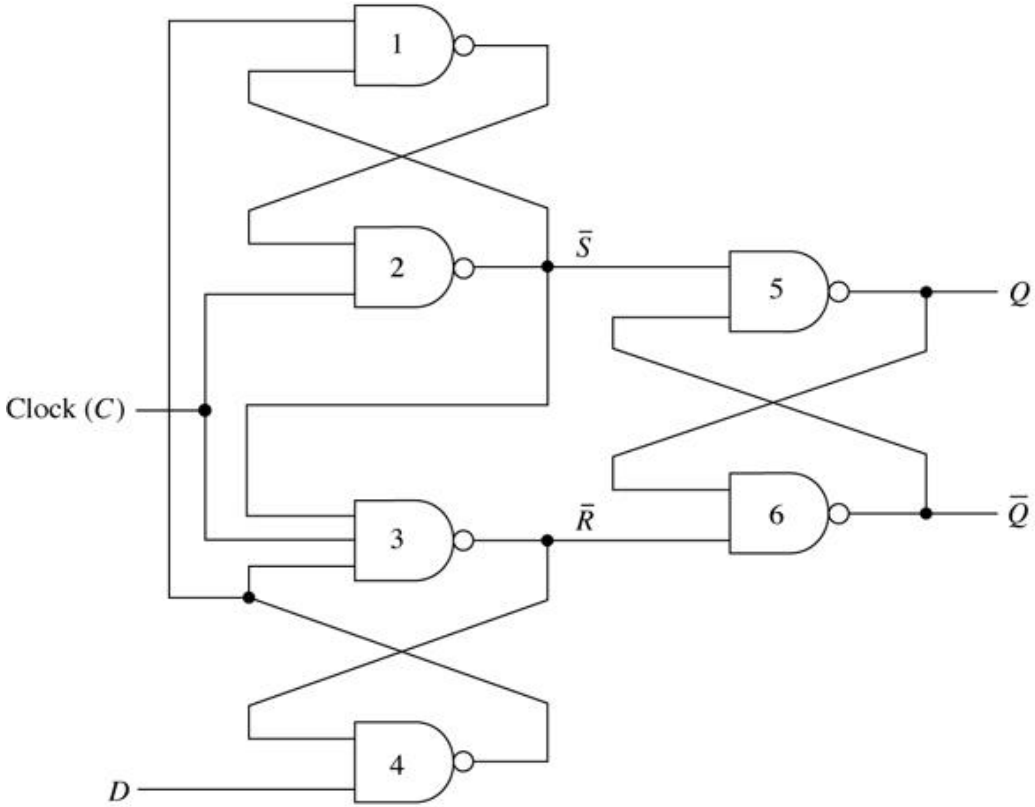
- Triggering means making the circuit active [allow it to receive inputs]
- Triggering makes a circuit synchronous
- Triggering is given in the form of clock or gate signal
- Depending on the type of triggering used circuit becomes active at specific states of clock pulse
  - Level Triggering: Circuit becomes active when gating or clock pulse is at a particular level
  - Edge Triggering: Circuit becomes active at the negative edge or positive edge of the clock signal

# Edge Triggered Flip-Flops

- Uses just one of the edges of the control to affect the reading of information on input lines.
- Designed to use either the positive or negative edge of the clock.
- Once triggering edge occurs the flip-flop remains unresponsive to information input changes until the next triggering edge.

# Positive Edge Triggered D Flip-Flop

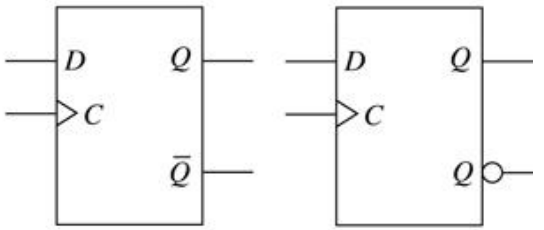
- Setting or Resetting of the flip-flop is established by the rising, or positive, edge of the control signal.




(a)

| Inputs | | Outputs | |
|---|---|---|---|
| $D$ | $C$ | $Q^+$ | $\bar{Q}^+$ |
| 0 | ↑ | 0 | 1 |
| 1 | ↑ | 1 | 0 |
| X | 0 | $Q$ | $\bar{Q}$ |
| X | 1 | $Q$ | $\bar{Q}$ |

(b)

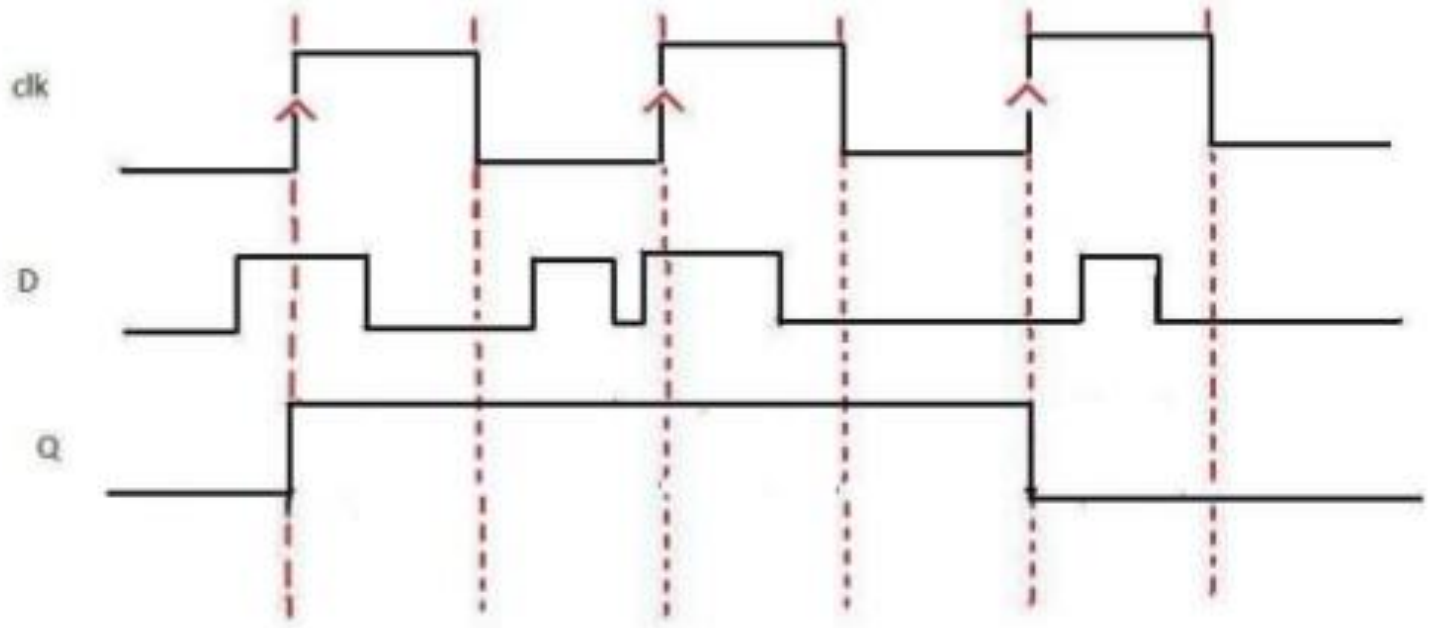



(c)

- NAND gates 5 and 6 serve as an $\bar{S}\bar{R}$ latch
- Assume C = 0
  - Regardless of input at D, the outputs of NAND gates 2 and 3 are 1.
  - Assume D = 0. NAND4 output is 1 causing output of NAND1 to be 0.
- If clock goes from 0-to-1 [+ve edge], all three inputs to NAND3 become 1, causing its output to change to 0.
- NAND2 output is maintained at 1 as NAND1 output is still 0.
- The Flip-Flop is reset.
- As NAND3 output is fedback to input of NAND4, any subsequent change in D while C=1 has no effect.

- Assume C = 0
  - Regardless of input at D, the outputs of NAND gates 2 and 3 are 1.
  - Assume D = 1. NAND4 output is 0 causing output of NAND1 to be 1.
- If clock goes from 0-to-1 [+ve edge], both inputs to NAND2 become 1, causing its output to change to 0.
- NAND3 output is maintained at 1 as NAND4 output is still 0.
- The Flip-Flop is set.
- As NAND2 output serves as input of NAND1 and NAND3, any subsequent change in D while C=1 has no effect.

# Timing Diagram for Positive Edge Triggered D Flip Flop

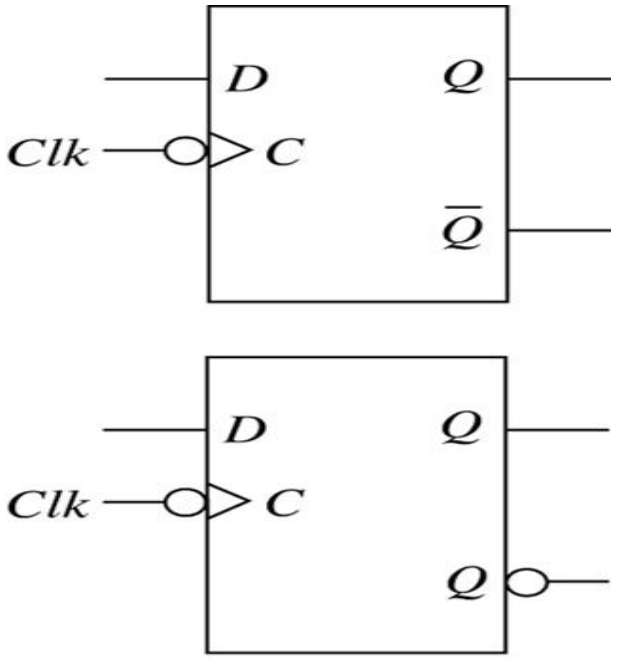


# Negative Edge Triggered D Flip-Flop

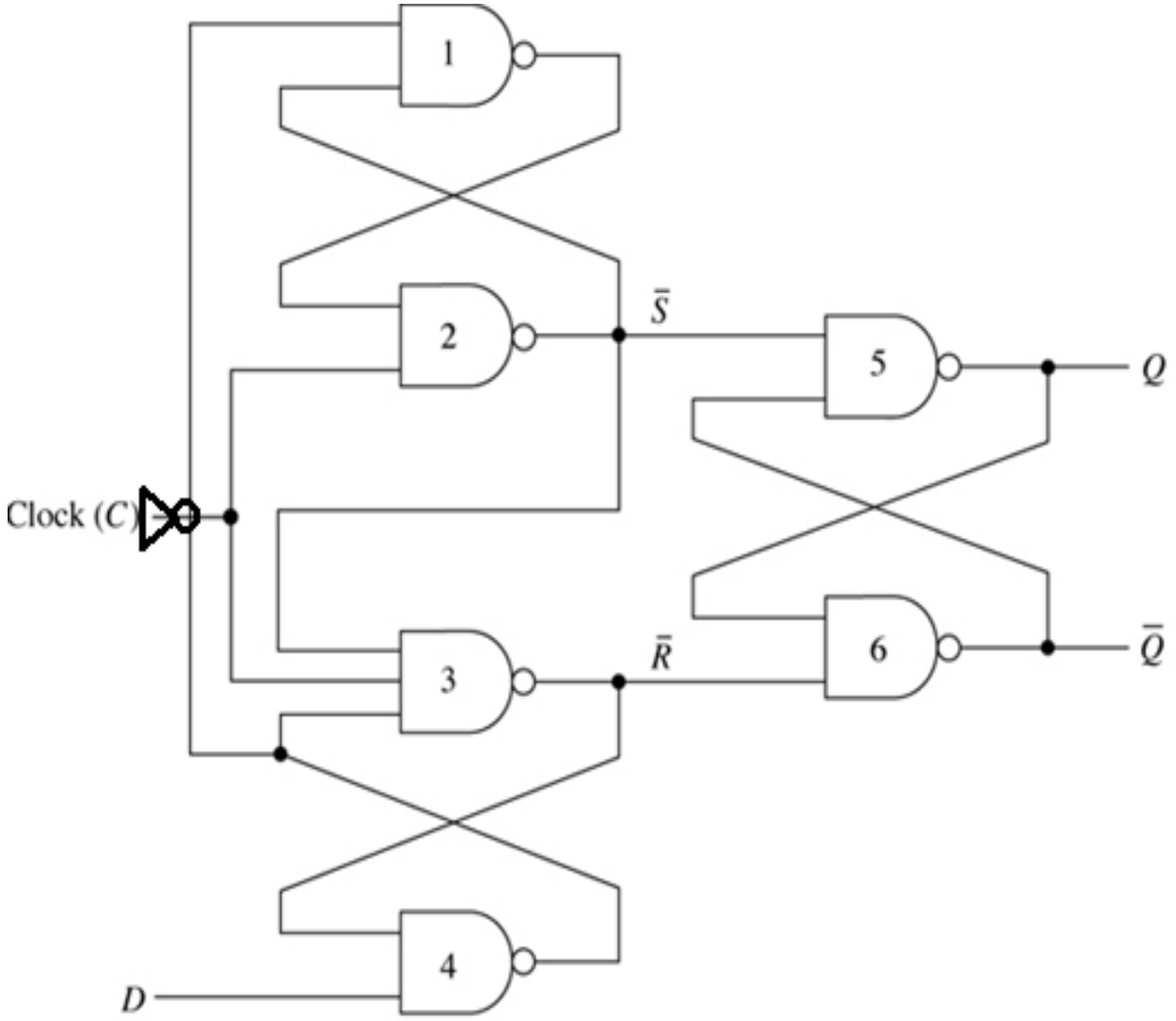
- Falling edge is used to sample the D input .
- Achieved by using an inverter at the control input of the flip-flop.

| Inputs | | Outputs | |
|---|---|---|---|
| $D$ | $Clk$ | $Q^+$ | $\overline{Q}^+$ |
| 0 | ↓ | 0 | 1 |
| 1 | ↓ | 1 | 0 |
| X | 0 | $Q$ | $\overline{Q}$ |
| X | 1 | $Q$ | $\overline{Q}$ |

(a)




(b)




(a)

| Inputs | | Outputs | |
|---|---|---|---|
| $D$ | $C$ | $Q^+$ | $\bar{Q}^+$ |
| 0 | ↓ | 0 | 1 |
| 1 | ↓ | 1 | 0 |
| X | 0 | $Q$ | $\bar{Q}$ |
| X | 1 | $Q$ | $\bar{Q}$ |

(b)

- NAND gates 5 and 6 serve as an latch
- Assume C = 1
- Regardless of input at D, the outputs of NAND gates 2 and 3 are 1.
- Assume D = 0. NAND4 output is 1 causing output of NAND1 to be 0.
- If clock goes from 1-to-0 [-ve edge], all three inputs to NAND3 become 1, causing its output to change to 0.
- NAND2 output is maintained at 1 as NAND1 output is still 0.
- The Flip-Flop is reset.
- As NAND3 output is fedback to input of NAND4, any subsequent change in D while C=0 has no effect.

- Assume C = 1
- Regardless of input at D, the outputs of NAND gates 2 and 3 are 1.
- Assume D = 1. NAND4 output is 0 causing output of NAND1 to be 1.
- If clock goes from 1-to-0 [-ve edge], both inputs to NAND2 become 1, causing its output to change to 0.
- NAND3 output is maintained at 1 as NAND4 output is still 0.
- The Flip-Flop is set.
- As NAND2 output serves as input of NAND1 and NAND3, any subsequent change in D while C=0 has no effect.

# Draw the timing diagram for negative edge triggered D flip flop

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# Characteristic Equations

- Algebraic description of the next state table of a flip-flop.
- Obtained by constructing the K-Map for Q+ in terms of present state and information input variables.

Function tables of *SR*, *JK*, *D* and *T* flip-flops

| $S$ | $R$ | $Q^+$ |
|---|---|---|
| 0 | 0 | Q |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | – |

(a)

| $J$ | $K$ | $Q^+$ |
|---|---|---|
| 0 | 0 | Q |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\bar{Q}$ |

(b)

| $D$ | $Q^+$ |
|---|---|
| 0 | 0 |
| 1 | 1 |

(c)

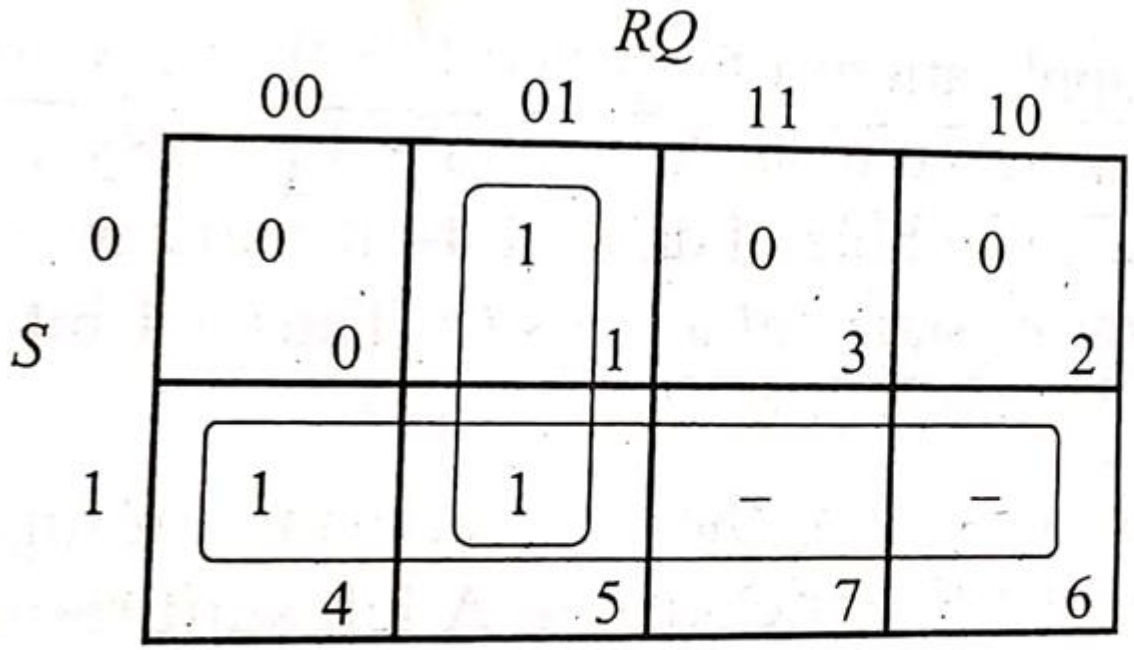
| $T$ | $Q^+$ |
|---|---|
| 0 | Q |
| 1 | $\bar{Q}$ |

(d)

# Next state table of SR flip-flop

| *Row no.* | $S$ | $R$ | $Q$ | $Q^+$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | – |
| 7 | 1 | 1 | 1 | – |

# Characteristic equation of SR flip-flop



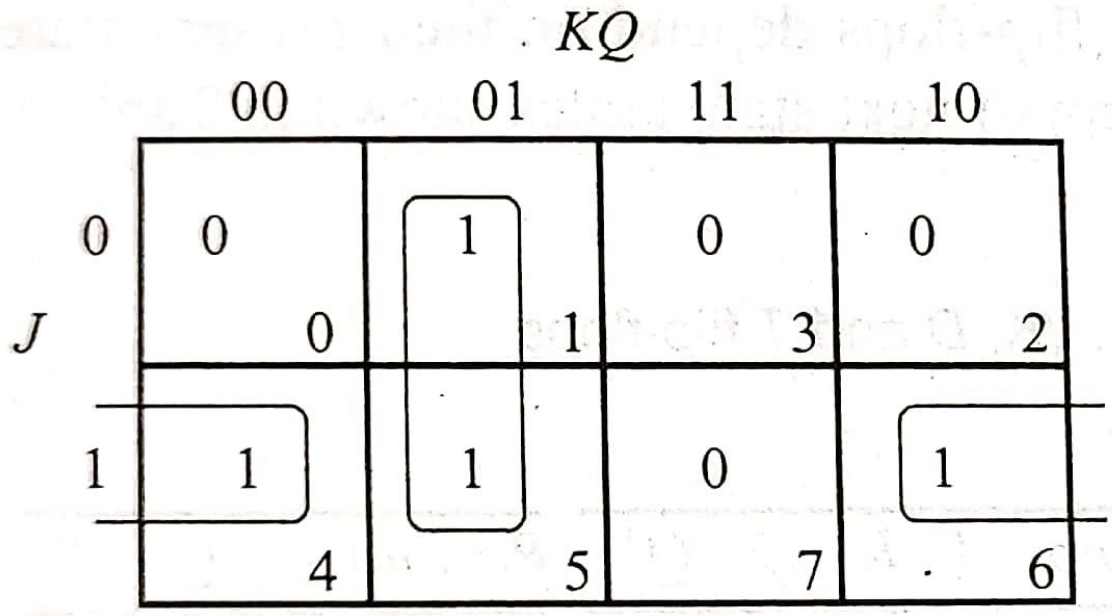

$Q^+ = S + \overline{R}\,Q$
subject to $SR = 0$

Karnaugh map for next state table of $SR$ flip-flop

# Next state table of JK flip-flop

| *Row no.* | $J$ | $K$ | $Q$ | $Q^+$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 0 |

# Characteristic equation of JK flip-flop

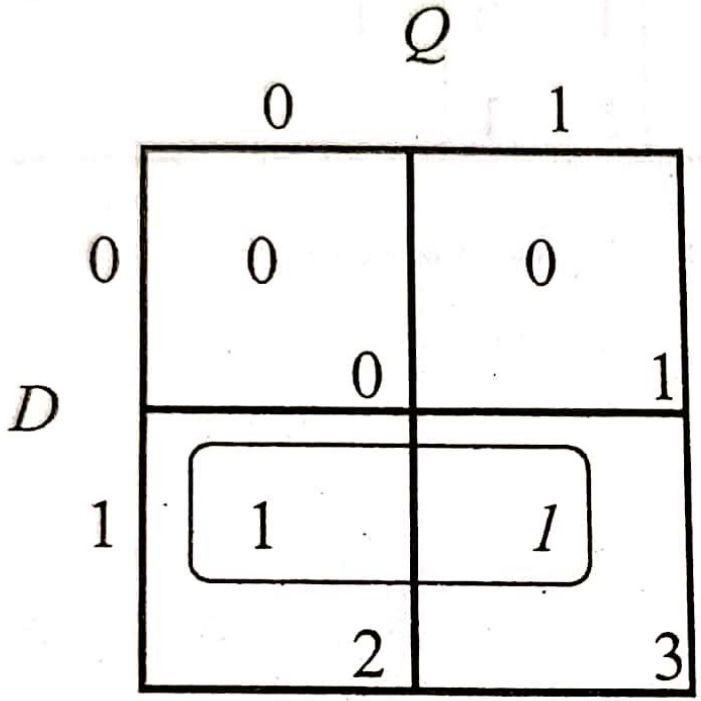



$$Q^{+} = J\overline{Q} + \overline{K}Q$$

# Next state table of D flip-flop

| *Row no.* | $D$ | $Q$ | $Q^+$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 2 | 1 | 0 | 1 |
| 3 | 1 | 1 | 1 |

# Characteristic equation of D flip-flop

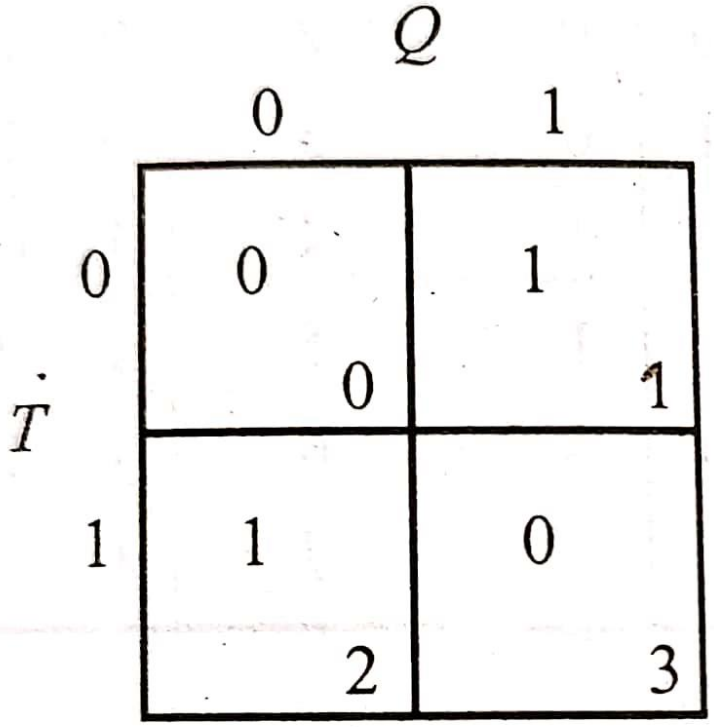



$$Q^+ = D$$

# Next state table of T flip-flop

| *Row no.* | $T$ | $Q$ | $Q^+$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 2 | 1 | 0 | 1 |
| 3 | 1 | 1 | 0 |

# Characteristic equation of T flip-flop




$$Q^+ = \bar{T}Q + T\bar{Q} = T \oplus Q$$

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# Verilog code SR Flip Flop in behavioral modeling

```
module srff_behave(s,r,clk, q,
qbar);
input s,r,clk;
output reg q, qbar;
always@(posedge clk)
begin
if(s == 1)
begin
q = 1;
qbar = 0;
end
else if(r == 1)
        begin
        q = 0;
        qbar =1;
        end
else if(s == 0 && r == 0)
        begin
        q <= q;
        qbar <= qbar;
        end
        end
        endmodule
```

# Verilog code D Flip Flop in behavioral modeling

```
module d_ff( d , clk , reset , q ,qb);
input d, clk, reset ;
output q,qb;
reg q,qb;
always @ ( posedge clk or
posedge reset)
begin
if (reset)
begin
q = 1'b0;
qb=~q;
end
else
begin
q = d;
qb=~q;
end
end
endmodule
```

# Verilog code JK Flip Flop in behavioral modeling

```
module jk_f_f(j,k,clk,reset,q,qb);
input j,k;
input clk;
input reset;
output q,qb;
reg q,qb;
always@(posedge clk)
begin
if (reset==1'b1)
q = 1'd0 ;
else
begin
case({j,k})
2'b00 : q = q ;
2'b01 : q = 1'd0 ;
2'b10 : q = 1'd1 ;
2'b11 : q = ~ q ;
endcase
end
qb = ~q;
end
endmodule
```

# Verilog code T Flip Flop in behavioral modeling

```
module T_f_f(clk,reset,t,q,qb);
input clk;
input reset;
input t;
output q;
output qb;
reg q,qb;
always@(posedge clk)
begin
if (reset==1'b1)
begin
q=1'b0;
qb=1'b1;
end
else
begin
if(t==1'b1)
q = ~q;
else
q = q;
end
qb=~q;
end
endmodule
```

# Lecture 30 and 31 - Introduction to Xilinx Tool and simulate the programs