Sequential Circuits - Counters and Shift Registers

Assignment - 7

1.A shift register has eight flip-flops. What are the largest binary, decimal and hexadecimal numbers that can be stored in it?

Ans :

Binary - 11111111

Decimal - 256

Hexadecimal - 0xFF

How many flip-flops are needed in a shift register to store

(a) 6-bit binary numbers?

(b) Decimal numbers up to 24?

(c) Hexadecimal numbers up to E?

Ans :

a. 6 flip flops

b. 5 flip flops

c. 4 flip flops

2. A shift register has eight flip-flops. What is the largest binary, decimal and hexadecimal numbers that can be stored in it?

Ans :

Binary - 11111111

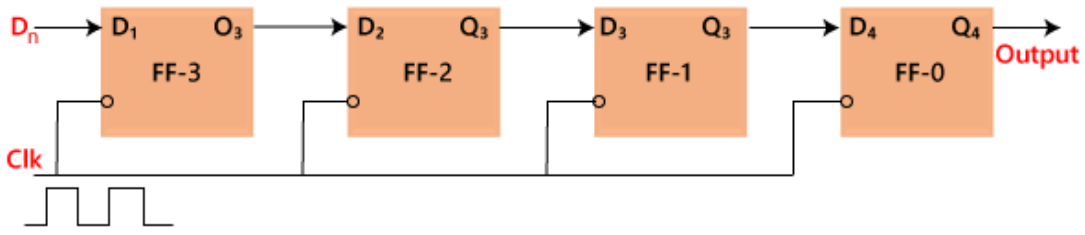
Decimal - 256

Hexadecimal - 0xFF

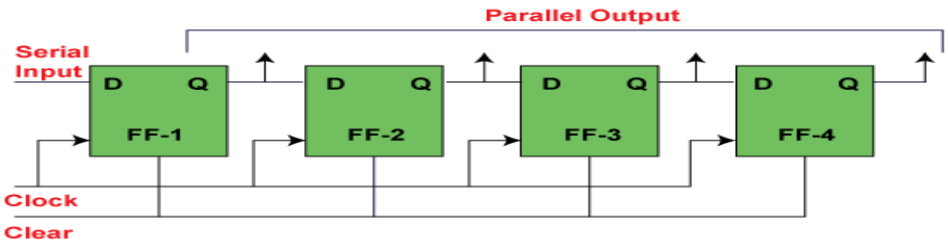
3. Name the four types of shift registers. Draw their block diagrams.

Ans:

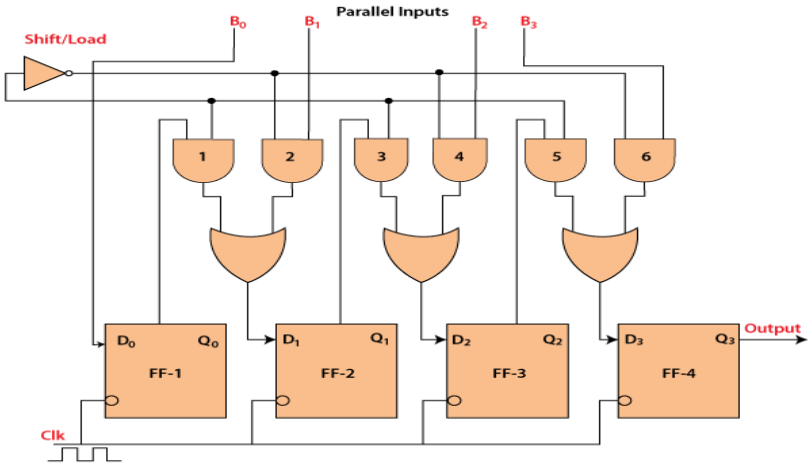
Serial In Serial Out



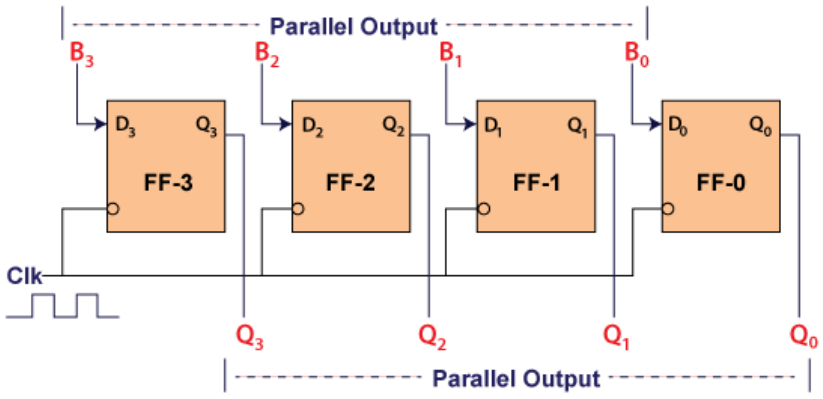
Serial In Parallel Out



Parallel In Serial Out



Parallel In Parallel Out



4. How many flip-flops are needed for (a) Mod-128 counter, (b) Mod-64 counter, and (c) Mod-32 counter?

Ans:

a. 7 flip flops
b. 6 flip flops
c. 5 flip flops

5. What is the Mod of the counter to store Hexadecimal number AE
Ans : Mod-256

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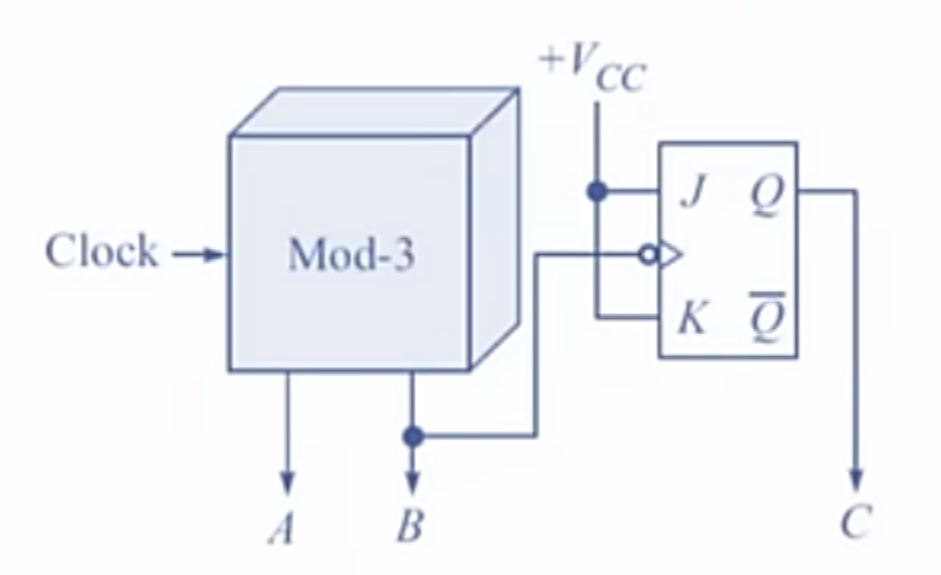
6. A 6-bit ripple down counter has the following states: (SKIP)
(a) 101010 (b) 001100 (c) 110000

7. Design a mod-3 counter (non-linear).

8. Convert Mod-3 counter to a Mod-6 counter.



9. Explain shift registers with examples.
Ans:
A shift register is a type of digital circuit designed by cascading flip-flops where the output of one flip-flop is connected to the input of the next. Ex: SISO SIPO PISO PIPO

10. Distinguish between synchronous and asynchronous counters.

Ans:

Synchronous counters	Asynchronous counters
All flip-flops (or stages) change state simultaneously, triggered by the same clock signal.	An asynchronous counter, also known as ripple counter, does not rely on a common clock signal to trigger state changes in all stages.
The clock signal acts as a	Each stage of an asynchronous

synchronous input, meaning that all changes in the counter occur at the same time, typically on the rising or falling edge of the clock.	counter changes state based on the output of the previous stage.

11. How many flip-flops would be required for a shift register to store (a) 0.7-bit number? (b) decimal number up to 64? (c) hexadecimal numbers up to 1?

Ans :

a. depends on how many bits we are going to represent the floating point number (Ex if it is 32 bits, we need 32 ff's, 10 bits we need 10 ff's)

b. 6 ff

c. 4 ff

12. A shift register has 12 flip-flops. What is the largest (a) decimal number, and (b) hexadecimal number that can be stored in it?

Ans :

a. 4095

b. FFF

13. Four D flip-flops are connected to form a shift register. The register is initially empty. The number 1001 is shifted into the register.

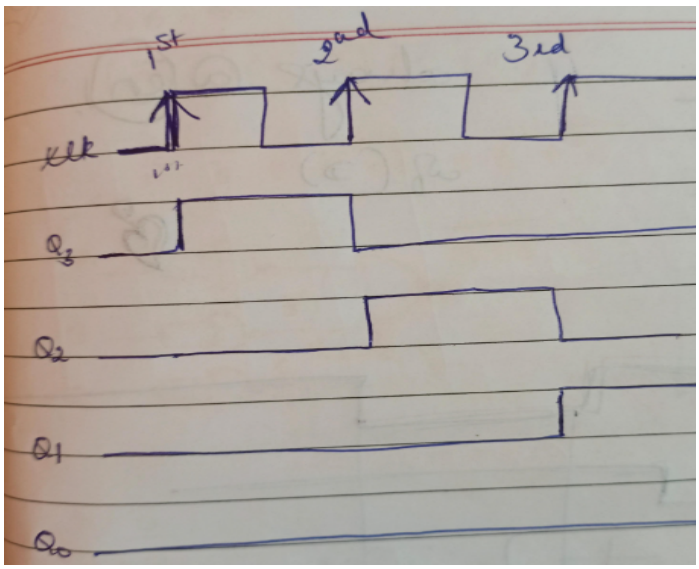
Complete the following table.

Data 1001 | Pulse No. | Q3 | Q2 | Q1 | QO

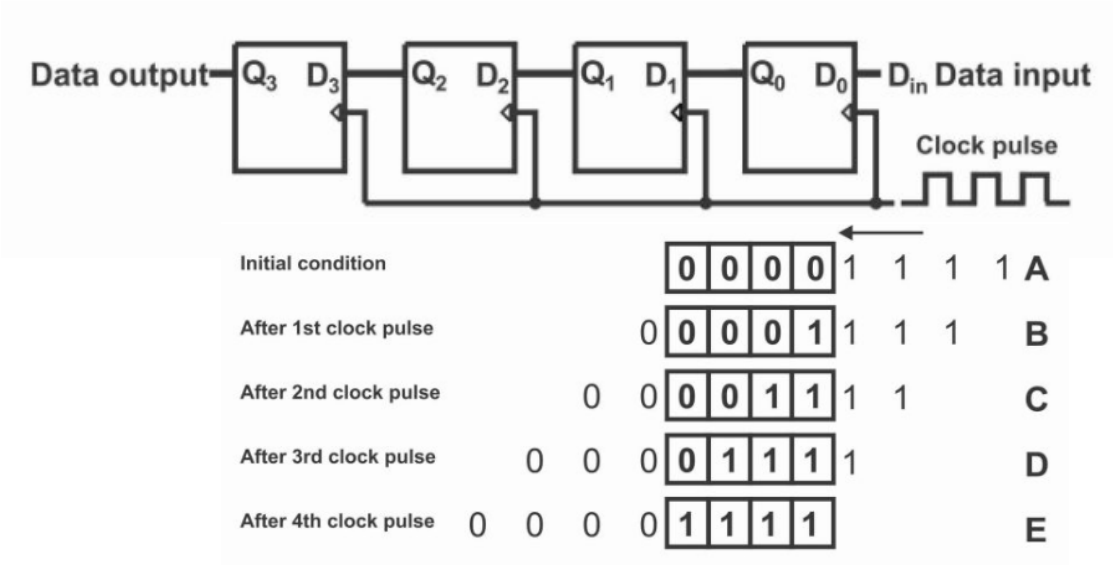
Also draw the waveform at the third clock transition.

Ans:

Data	Pulse No.	Q3	Q2	Q1	QO
1001	0	0	0	0	0
	1	1	0	0	0
	2	0	1	0	0
	3	0	0	1	0
	4	1	0	0	1



15. Using four D flip-flops design a shift-left register and explain its operation.
Ans:

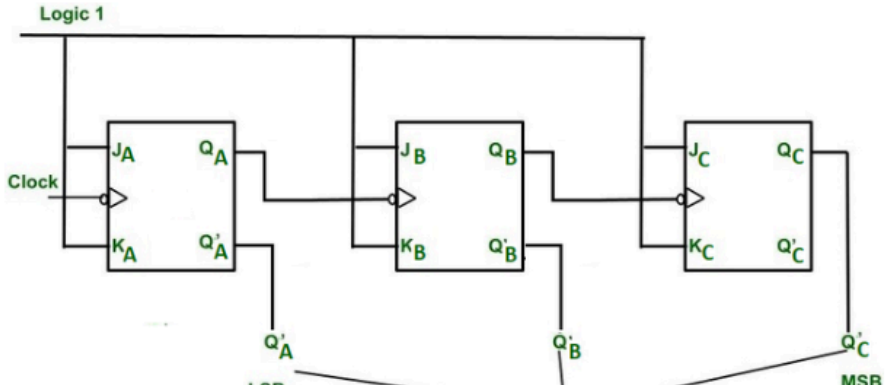


16. Draw the schematic of four JK flip-flops. Design an asynchronous down counter and write its truth table.
Ans :

Truth Table :

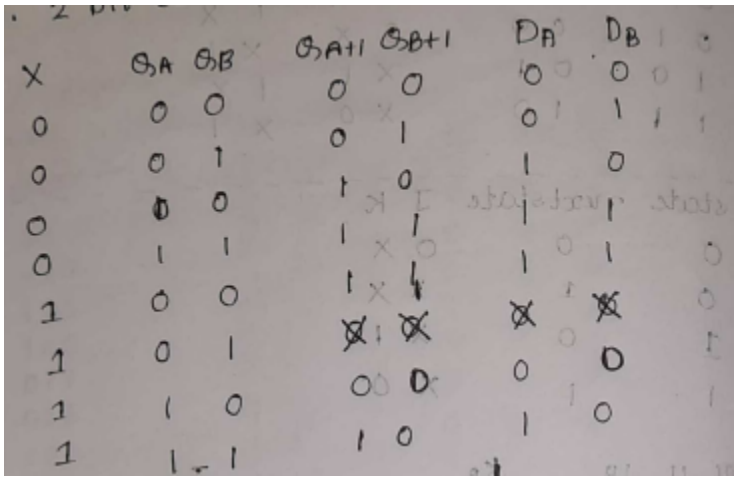
Clock	Q_C	Q_B	Q_A	Q'_C	Q'_B	Q'_A
Initially	0	0	0	1	1	1
1st	0	0	1	1	1	0
2nd	0	1	0	1	0	1
3rd	0	1	1	1	0	0
4th	1	0	0	0	1	1
5th	1	0	1	0	1	0
6th	1	1	0	0	0	1
7th	1	1	1	0	0	0

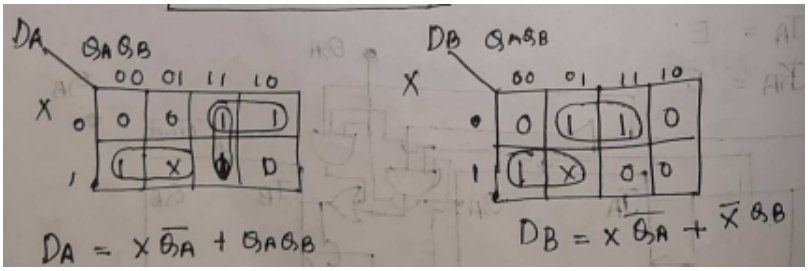
Circuit :

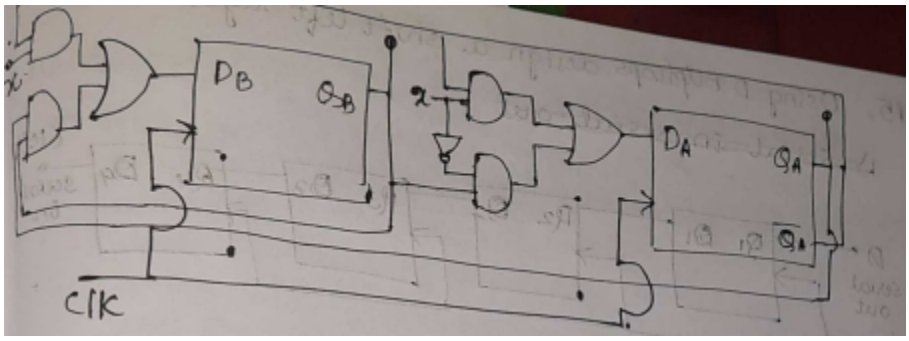


17. Design a 2-bit count-down counter. This is a sequential circuit with two FFs, and one input x. When x = 0, the state of the FFs does not change. When x = I, the state sequence is 11, 10, 00, 11, and repeat.

Ans:







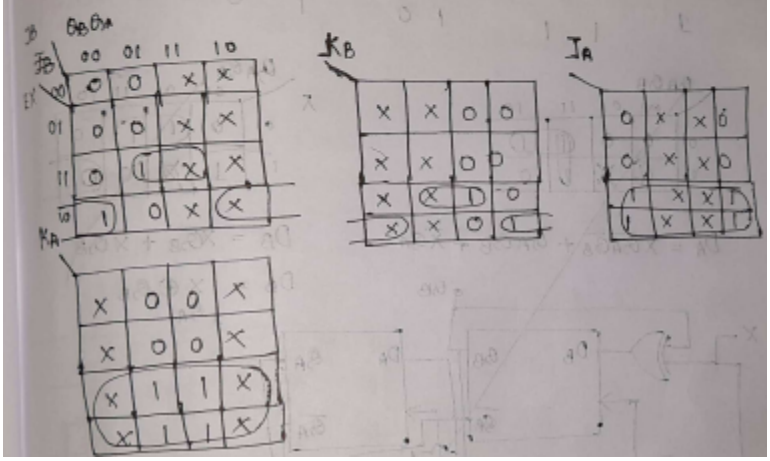
18. Design a sequential circuit with two JK FFs A and B and two inputs E and x. If E = 0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to II back to 00, and repeat. When E = I and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.

18. Two JK Flipflops → A and B and inputs E and X

De	E	X	present state $Q_B\ Q_A$	next state $Q_{B+1}\ Q_{A+1}$	J_B	K_B	J_A	K_A
0	0	0	0 0	0 0	0	X	0	X
1	0	1	0 1	0 1	0	X	X	0
2	0	0	1 0	1 0	X	0	0	X
3	0	0	1 1	1 1	X	0	X	0
4	0	1	0 0	0 0	0	X	0	X
5	0	1	0 1	0 1	0	X	X	0
6	0	1	1 0	1 0	X	0	0	X
7	0	1	1 1	1 1	X	0	X	0
12	1	1	0 0	0 1	0	X	1	X
13	1	1	0 1	1 0	1	X	X	1
14	1	1	1 0	1 1	X	0	1	X
15	1	1	1 1	0 0	X	1	X	1

X	Q_B	Q_A	Q_{B+1}	Q_{A+1}	J_B	K_B	J_A	K_A
0	0	0	1	1	1	X	1	X
0	0	1	0	0	0	X	X	1
0	1	0	0	1	X	1	1	X
0	1	1	1	0	X	0	X	1

present state	next state	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

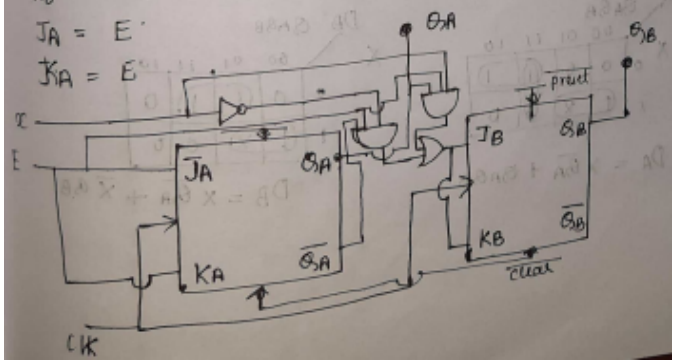


$J_B = E\bar{X}\bar{Q_A} + EXQ_A$

$K_B = E\bar{X}\bar{Q_A} + EXQ_A$

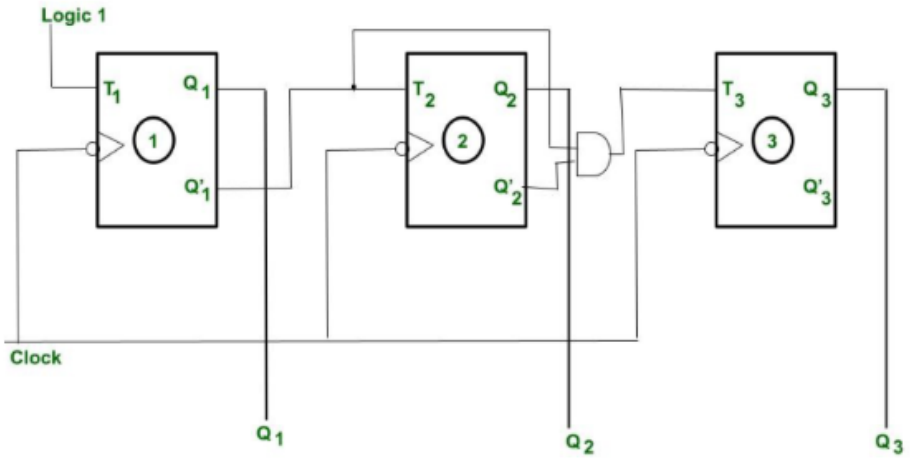
$J_A = E$

$K_A = E$

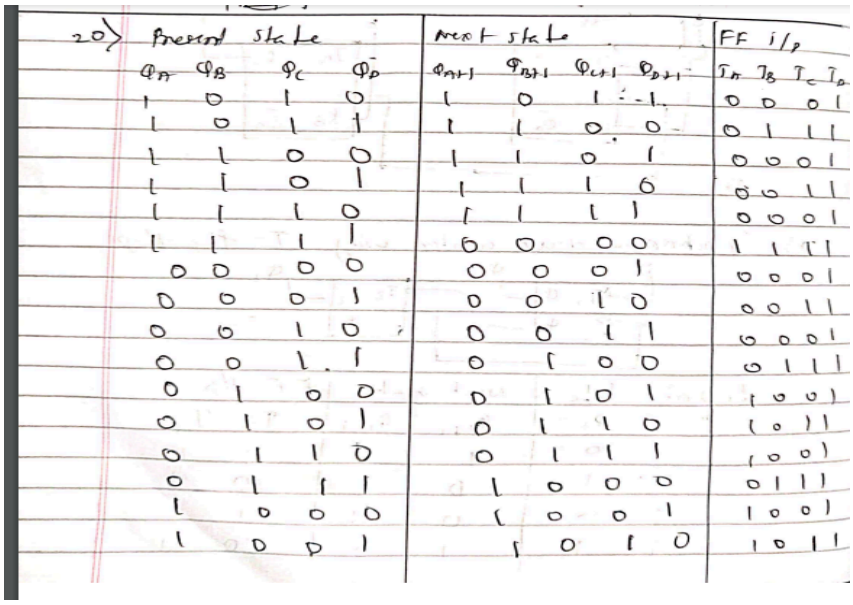


19. Draw the schematic of a model synchronous down counter using T flip-flops and prepare its truth table.
Ans :
Truth Table

Previous state			Next state					
Q_3	Q_2	Q_1	Q^*_3	Q^*_2	Q^*_1	T_3	T_2	T_1
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1



20. The synchronous up/down, mod-16 by additional logic circuitry is preset at 1O1O. Write its truth table as clock pulses are applied for up count from this state.



21. An up counter, 6-bit binary, has the following states:

(a) 1101010 (b) 001100 (c) 110000
Determine the number of flip-flops which would be complemented after application of one clock pulse
Ans:
a. 1 flip flop
b. 1 flip flop
c. 1 flip flop

22. What is the largest decimal number and largest hexadecimal number that can be stored in the Mod-64 counter?

Ans: MOD-64 counter consists of 64 states. Hence, the largest decimal number and the largest hexadecimal number which can be stored is 63 and 0x3F respectively.