Lab3)

Design

module mult\_if\_improved(a, b\_is\_late, c, d, sel, z);

input a, b\_is\_late, c, d;

input [3:0] sel;

output z;

reg z, z1;

always @(a or b\_is\_late or c or d or sel)

begin

z1 = 0;

if (sel[0])

z1 = a;

if (sel[2])

z1 = c;

if (sel[3])

z1 = d;

if (sel[1] & ~(sel[2]|sel[3]))

z = b\_is\_late;

else

z = z1;

end

Endmodule

Schematic

