

Quantum Galton Board (QGB) as a Universal Statistical Simulator

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Problem Statement

- **What:** We built a Quantum Galton Board (QGB) that acts as a universal statistical simulator mapping a Galton box to a quantum circuit; a single pass creates a superposition of all trajectories and outputs a target distribution.
- **Why it matters:** Sampling dominates Monte Carlo and many high-dimensional simulations. QGBs provide an intuitive path to quantum speedups and a clean testbed for NISQ noise/mitigation with relevance to transport, finance, and UQ.

Objectives

- 1 Generalize the QGB to n layers.
- 2 Reproduce three targets: Hadamard walk, classical/binomial, exponential.
- 3 Build a reliable benchmarking harness (noiseless vs. noisy) with robust post-processing and metrics.

Approach

- Modular circuit design: one-peg & multi-peg; measurements on odd-indexed “bin” qubits; total qubits = $2(n + 1)$ including coin.
- Fixed subtle right-bias by removing $CX(\text{position} \rightarrow \text{coin})$; enforce H-then-shift with control-on-0 for left branch.
- Full-grid embedding to quantify leakage; standardized endianness so 000...001 is the rightmost bar.

Targets

- Hadamard (unbiased), Classical/Binomial (verification), Exponential (per-peg $R_x(\theta)$ schedule).

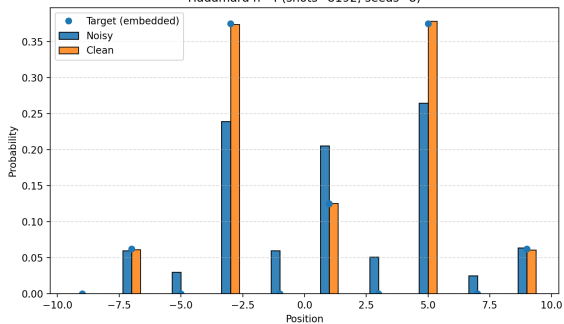
Metrics

- TVD, KL, Hellinger, leakage (mass off support), integrity (one-hot fraction). We fix $n = 4$ and average over seeds.

Results & Impact: Unbiased vs Classical (n=4)

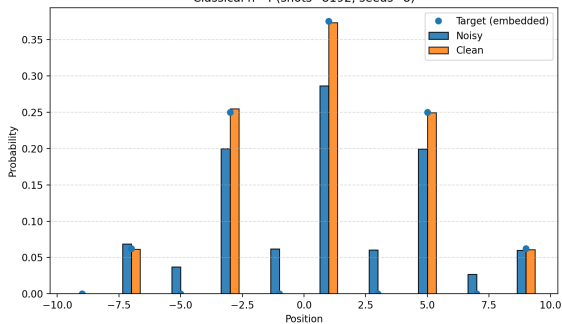
Hadamard (Unbiased)

Hadamard n=4 (shots=8192, seeds=8)



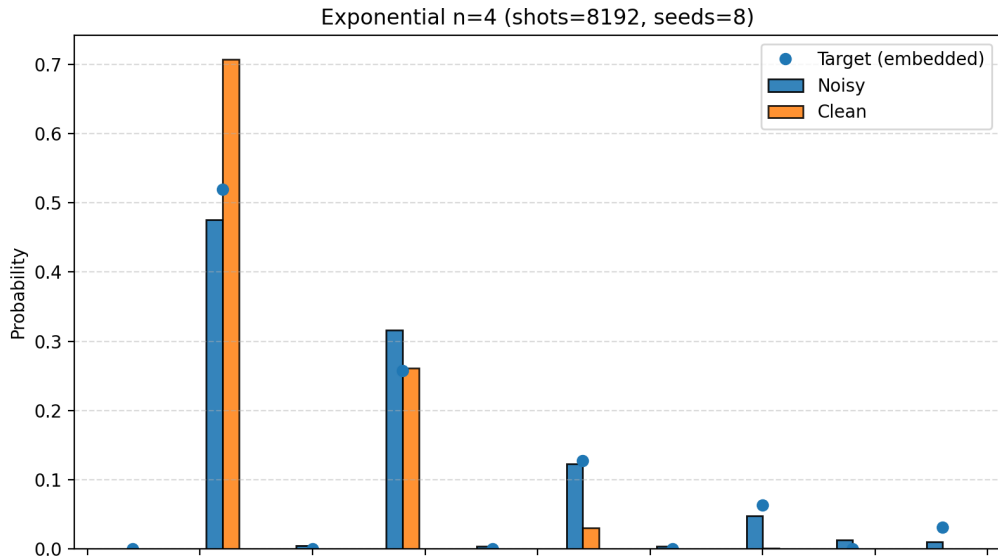
Classical / Binomial

Classical n=4 (shots=8192, seeds=8)



Clean vs analytic TVD ≈ 0.0046 (binomial); noisy vs clean TVD ≈ 0.19 – 0.25 with leakage driven by readout and CSWAP decomposition depth.

Results & Impact: Biased / Exponential (n=4)



- Reference-quality, symmetric QGB step others can reuse.
- Target-agnostic benchmarking harness with leakage/integrity—makes noise optimization measurable.
- Clear pathway from circuits \rightarrow distributions for Monte Carlo-style tasks.

- Noise optimization: layout constraints, CSWAP decompositions, dynamical decoupling, readout mitigation, transpiler tuning.
- Per-layer θ calibration for exponential target; explore uniformly controlled rotations & mid-circuit measure/reuse (MCMR/RUS).
- Real-hardware validation as access permits.

Thank You

Questions?

