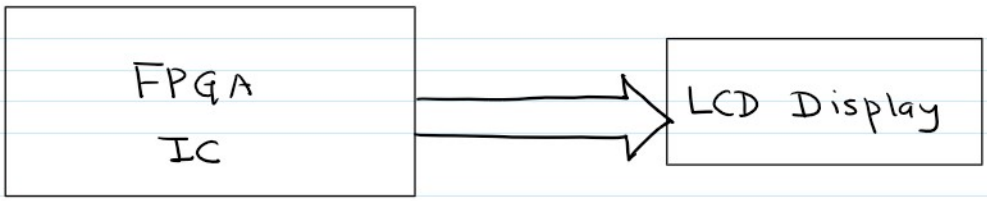
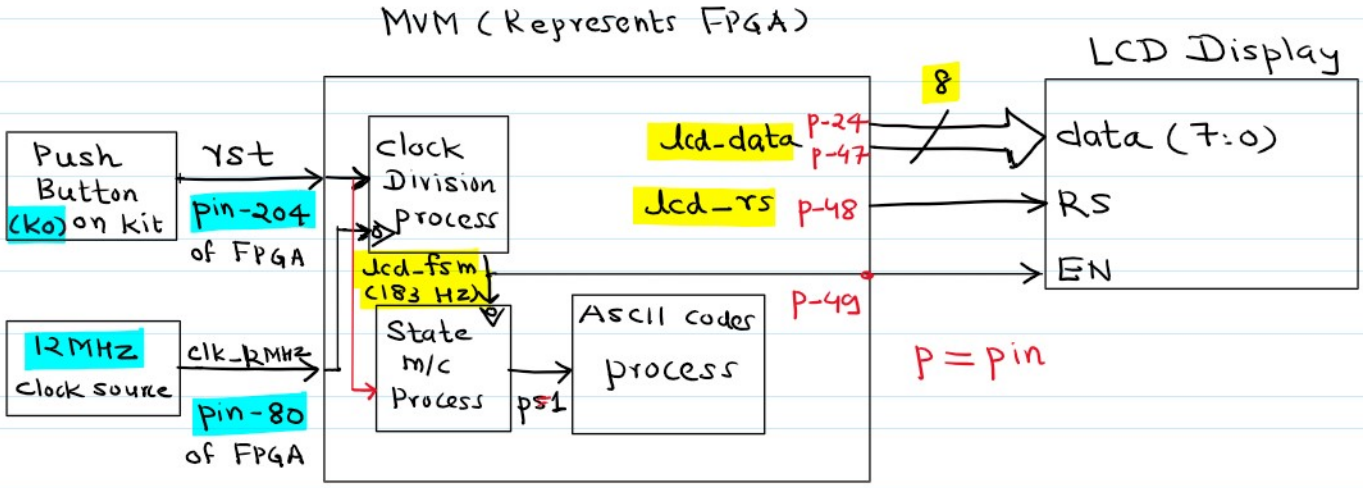
S8_22-09-2021

22 September 2021 08:56

Assignment : A.4 : FPGA-LCD Interfacing

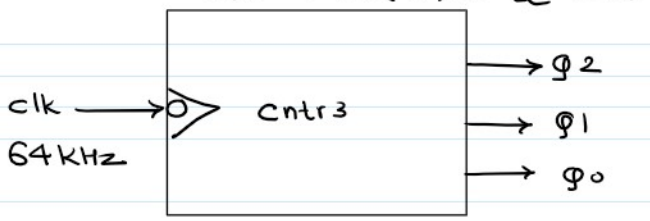


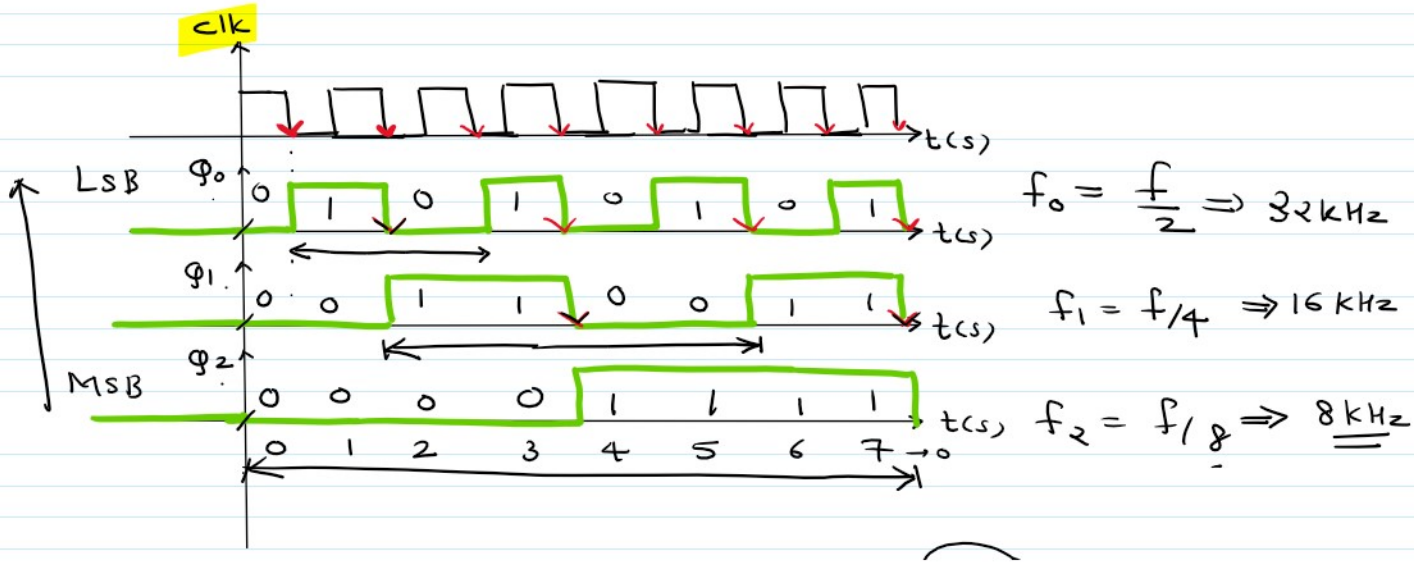


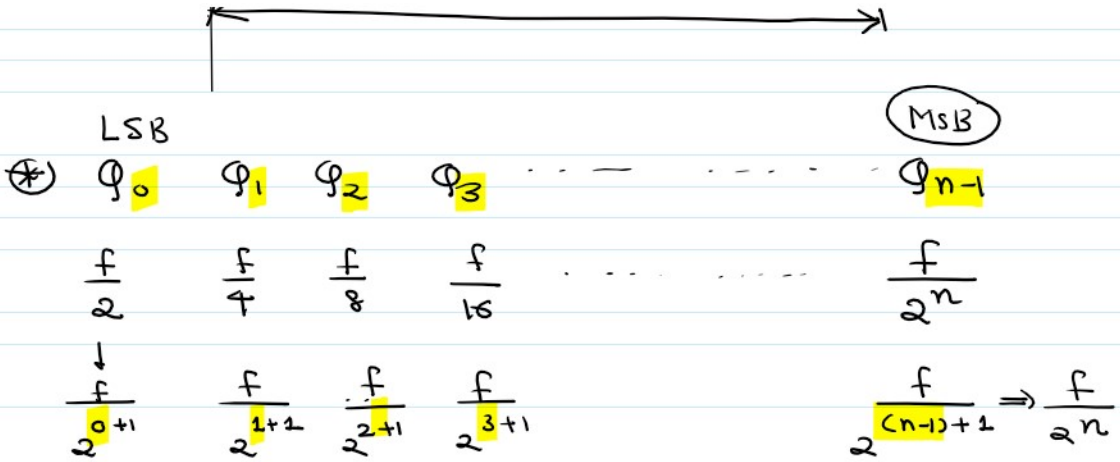
⊛ Frequency of individual bits of n-bit ↑/↓ counter driven by a clock of freq. 'f' Hz

Ans :- Consider a 3-bit ↑ counter as follows:-

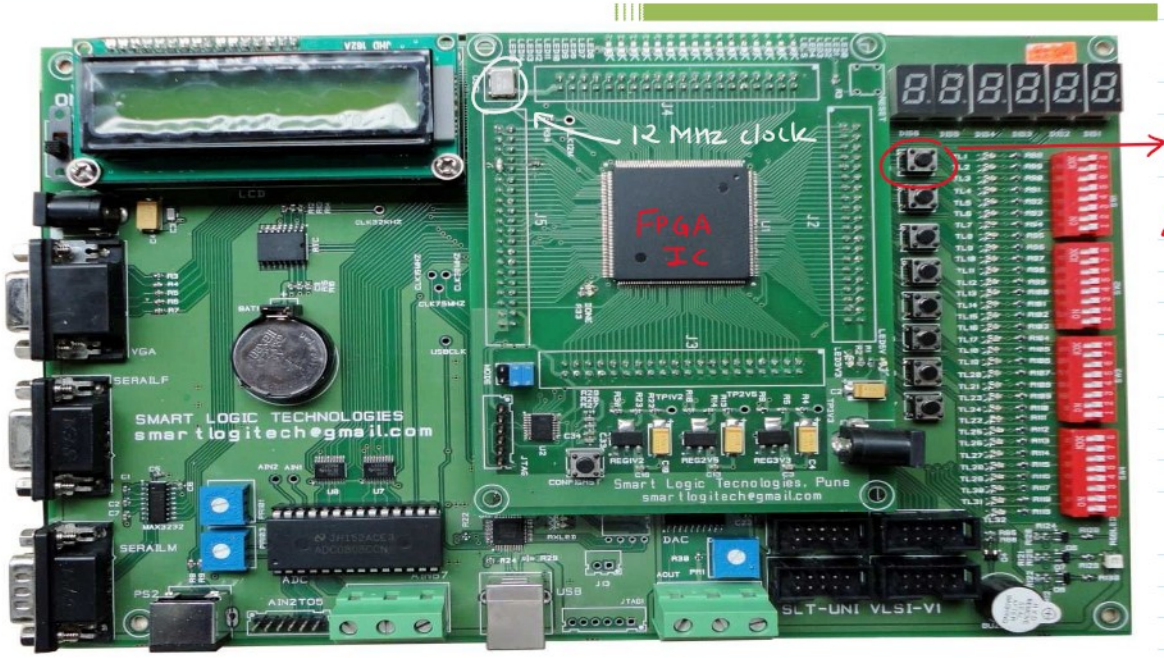
$000 \longrightarrow 111\ (8) \Rightarrow 2^3 = 2^n$







- We have defined a 16-bit Dummy signal "div"
- In Process-1; 16-bit UP counter sensitive to ↓ of 12 MHz clock
- MSB of "div" is assigned to Dummy signal dcd_fsm
- ∴ Freq. of dcd_fsm $= \frac{f_{clk}}{2^{16}} = \frac{12\ MHz}{65536} = 183\ Hz$
- Process-2 is sensitive to rst & clk_fsm & it defines state m/c Transitions.



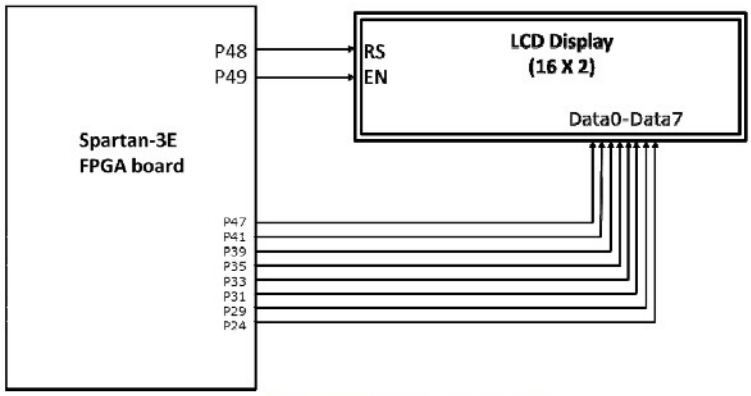


Figure 2.1: Interfacing of LCD with FPGA on kit

Pin Assignment (UCF Location) for Pushbuttons:

Signal Name	XC3S250E-PQ208	XCS6LX9-TQG144
K0	P204	P27
K1	P194	P16
K2	P184	P15
K3	P183	P14
K4	P174	P7
K5	P175	P8
K6	P169	NC
K7	P159	NC

Table 5.1: Pin Assignment (UCF) for Pushbuttons

Pin Assignment (UCF Location) for Clock Sources:

Signal Name	XC3S250E-PQ208	XC6SLX9-TQG144
RESET	--	P32
Clock_12MHz	P80	P55
Clock_7.5MHz	P78	NC
Clock_15MHz	P77	NC
Clock_30MHz	P83	NC
Clock_32kHz	P75	NC
Clock_555	P132	P120

Table 12.1: Pin Assignment (UCF) for Clock sources

LCD_FSM.ucf - Notepad
File Edit Format View Help

```
# PlanAhead Generated physical constraints

NET "clk_12Mhz" LOC = P80;
NET "rst" LOC = P204;

NET "lcd_rs" LOC = P48;
NET "lcd_en" LOC = P49;
NET "lcd_data[0]" LOC = P47;
NET "lcd_data[1]" LOC = P41;
NET "lcd_data[2]" LOC = P39;
NET "lcd_data[3]" LOC = P35;
NET "lcd_data[4]" LOC = P33;
NET "lcd_data[5]" LOC = P31;
NET "lcd_data[6]" LOC = P29;
NET "lcd_data[7]" LOC = P24;
```

Fig: 12.1

Fig: 5.1

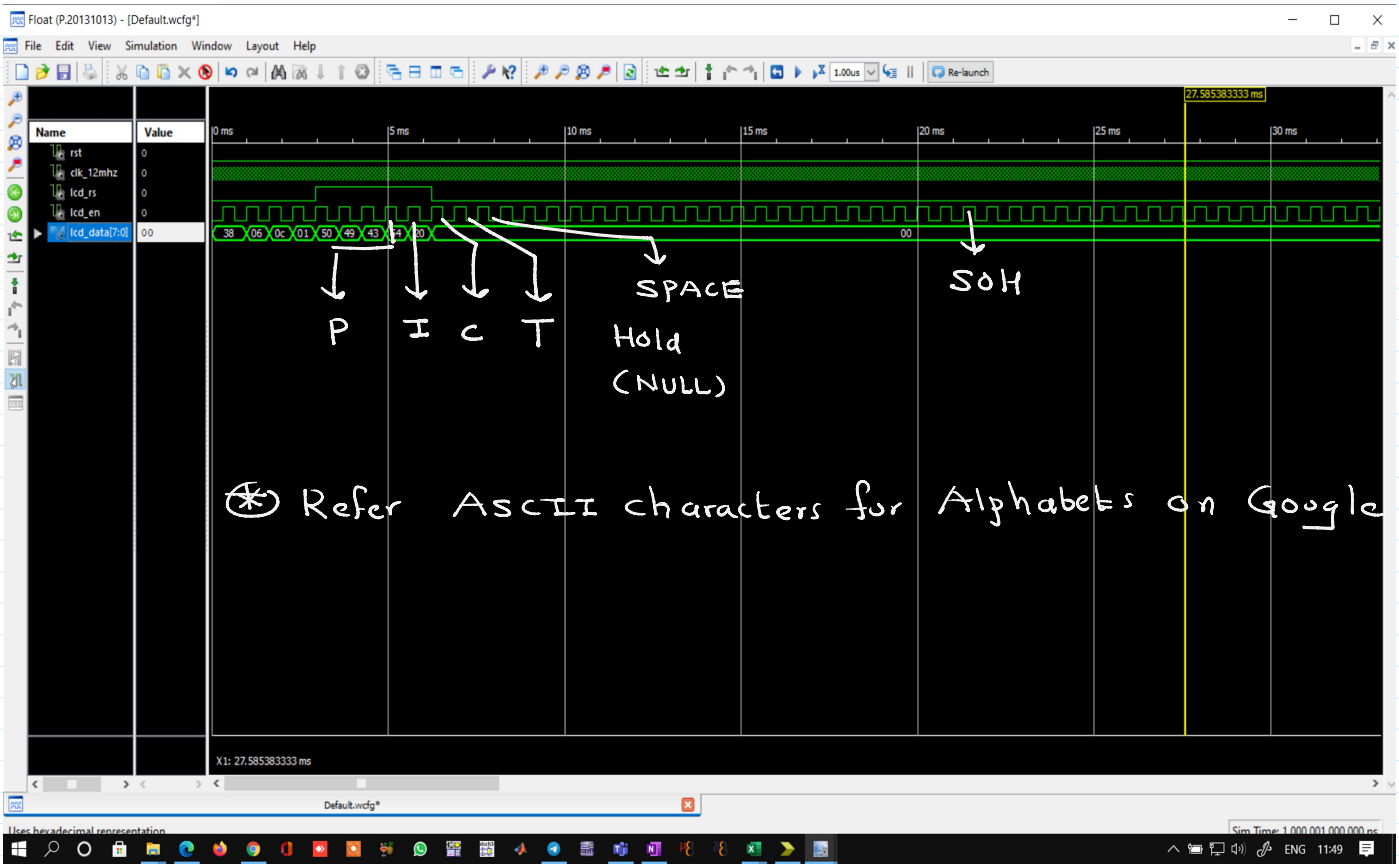
User Constrainst File (*.ucf)

RS of Display

EN of Display

Fig: - 2.1

ISim Waveforms for TVM Simulation



* Video Tutorial Link:-

PRACTICAL-10 : FPGA-LCD INTERFACING