

2.6 INTEL 8085 INSTRUCTIONS

2.6.1. Data Transfer Group

This group of instructions transfers data to and from registers and memory. Condition flags are not affected by any instruction in this group.

MOV r1, r2 (Move Register)
 $(r1) \leftarrow (r2)$

The content of register r2 is moved to register r1.

0	1	D	D	D	S	S	S
---	---	---	---	---	---	---	---

Cycles : 1
States : 4
Addressing : register
Flags : none

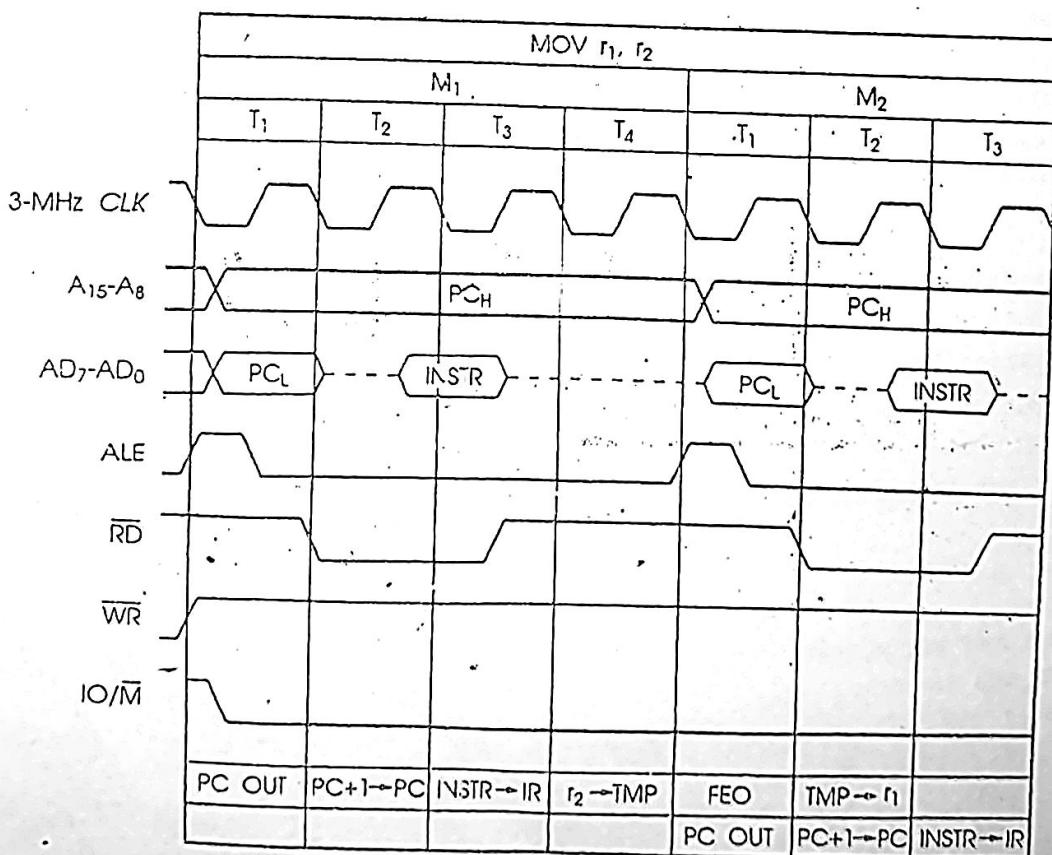


Fig. 2.1. Timing diagram for **MOV r1, r2**.

MOV r, M (Move from memory)

$(r) \leftarrow ((H)(L))$

The content of the memory location, whose address is in register H and L, is moved to register r.

0	1	D	D	D	1	1	0
---	---	---	---	---	---	---	---

Cycles : 2

States : 7

Addressing : reg. indirect

Flags : none

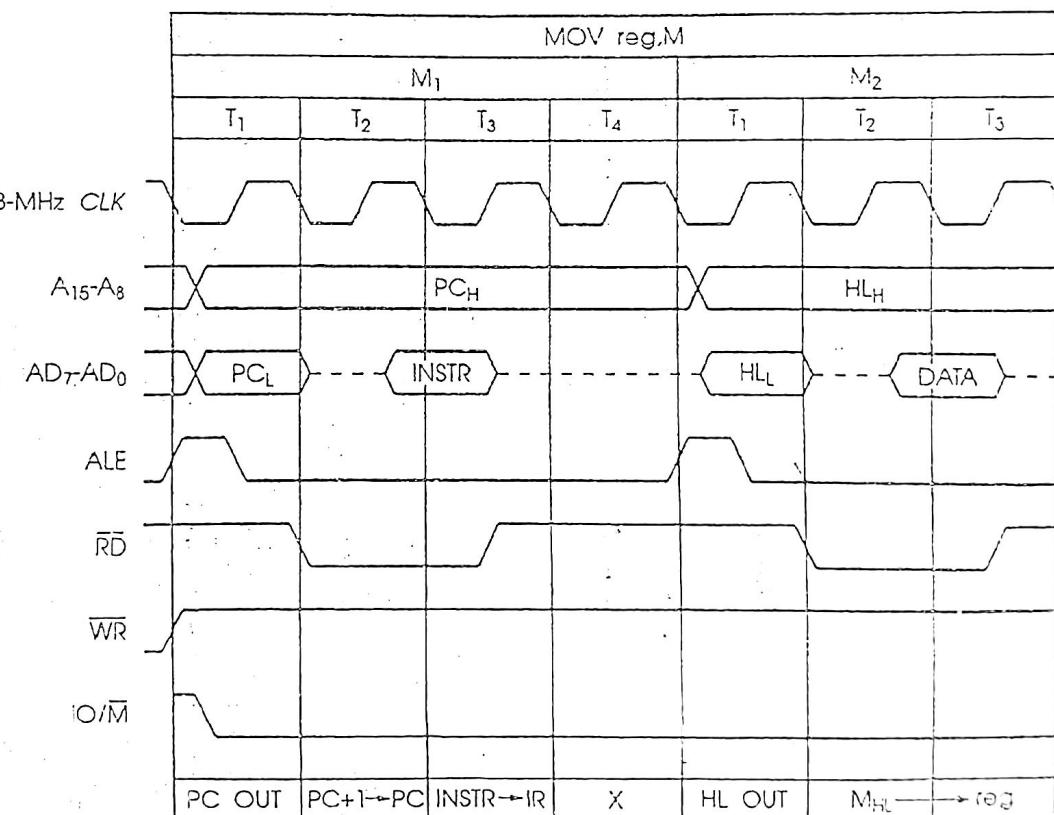


Fig. 2.2. Timing diagram for **MOV r, M**.

Cycles : 4
 States : 13
 Addressing : direct
 Flags : none

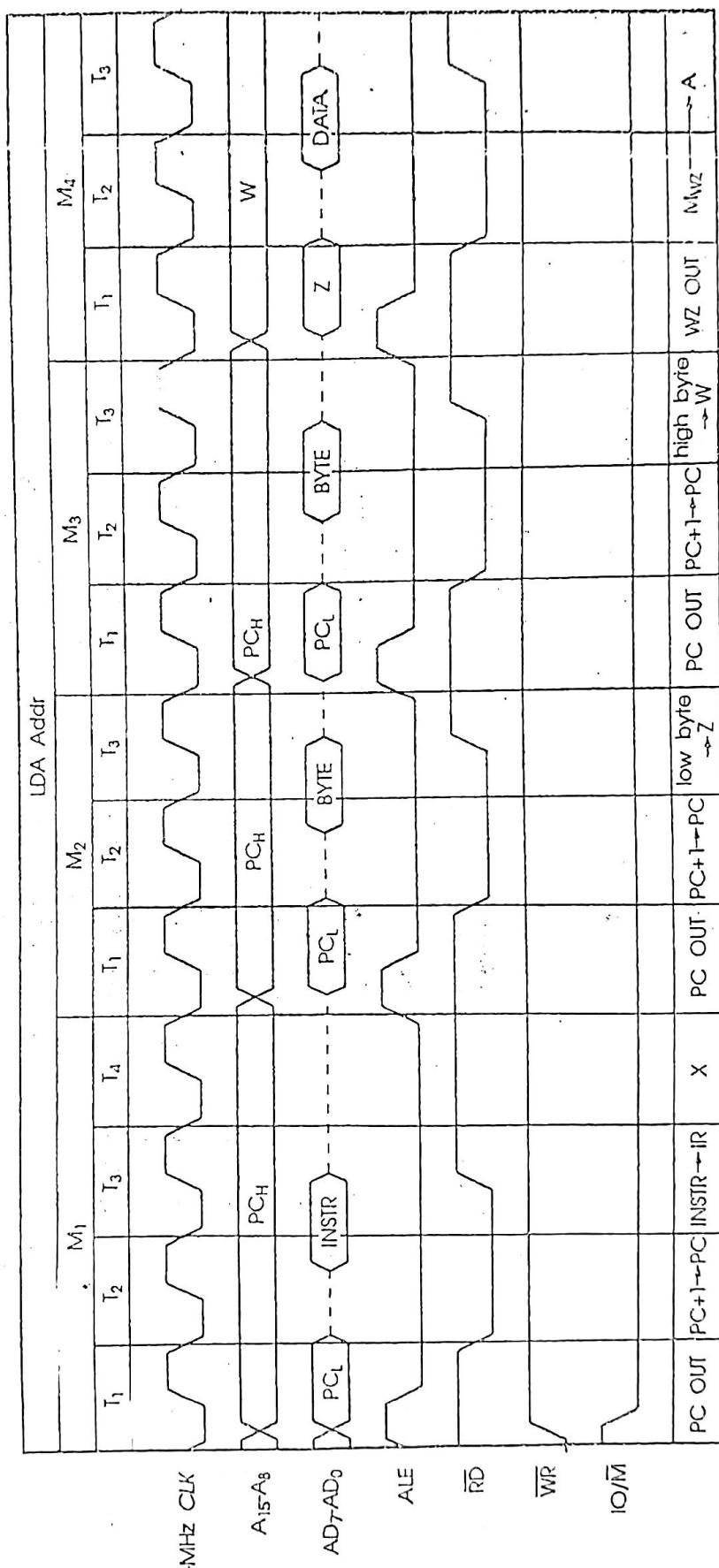


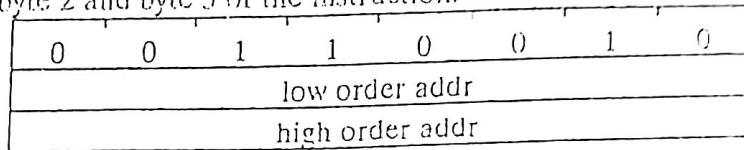
Fig. 2.7. Timing diagram for LDA addr.

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✓ STA addr (Store Accumulator direct)

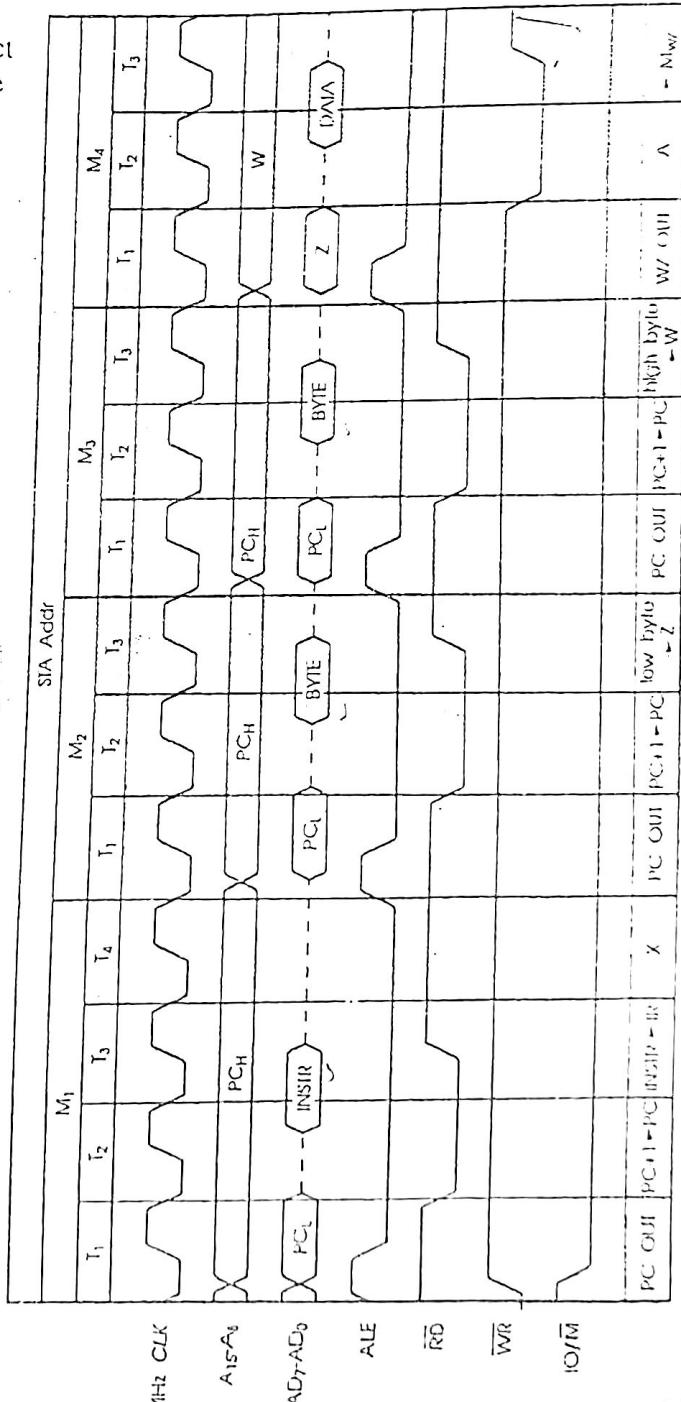
((byte 3) (byte 2)) \leftarrow (A)

The content of the accumulator is moved to the memory location whose address is specified in byte 2 and byte 3 of the instruction.



Cycles : 4
 States : 13
 Addressing : direct
 Flags : none

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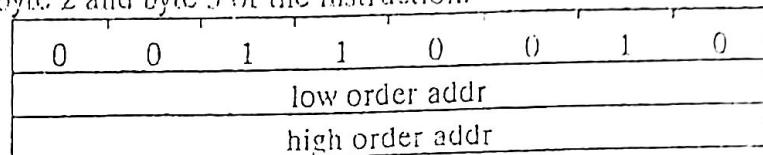


INSTRUCTION SET OF 8085

STA addr (Store Accumulator direct)

((byte 3) (byte 2)) \leftarrow (A)

The content of the accumulator is moved to the memory location whose address is specified in byte 2 and byte 3 of the instruction.



Cycles

: 4

States

: 13

Addressing

: direct

Flags

: none

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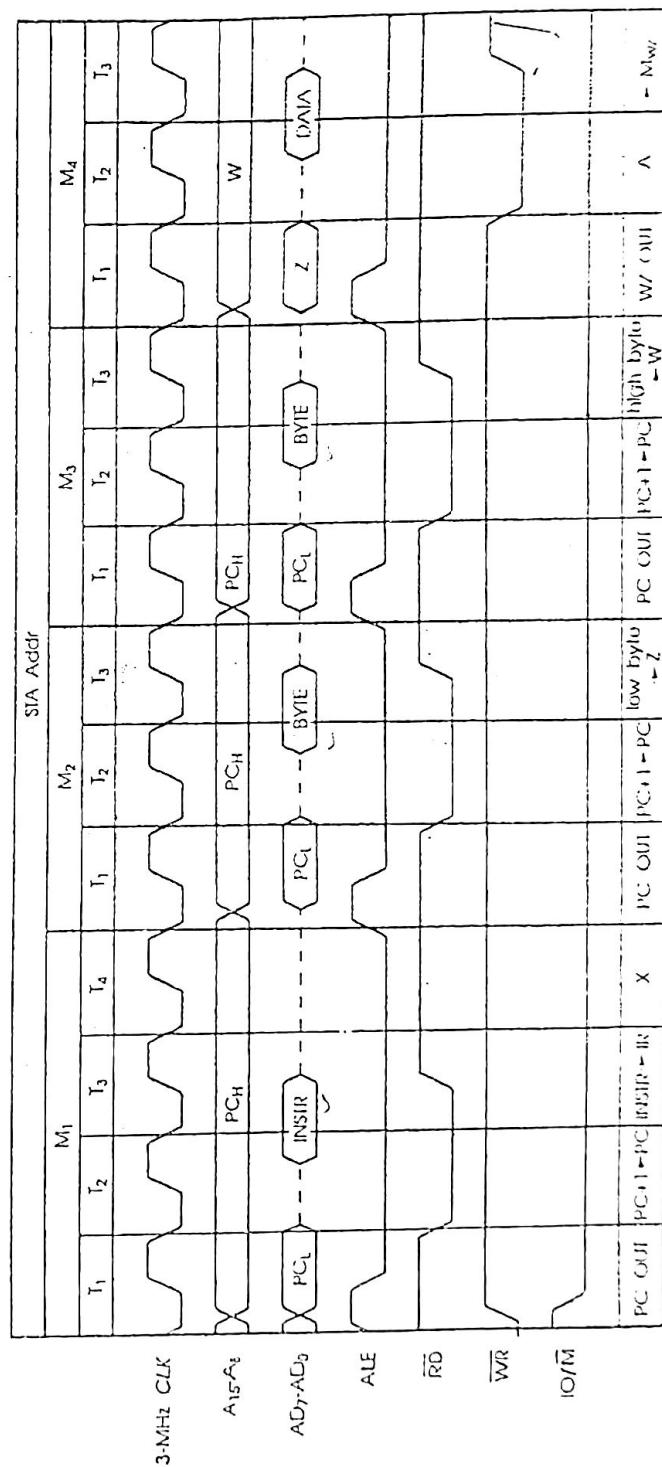


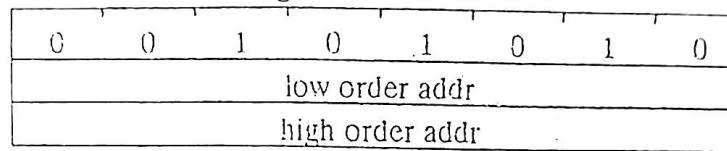
Fig. 2.8. Timing diagram for STA addr.

LHLD addr (Load H and L direct)

$$(L) \leftarrow ((\text{byte } 3)(\text{byte } 2))$$

$$(H) \leftarrow ((\text{byte } 3)(\text{byte } 2) + 1)$$

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register L. The content of the memory location at the succeeding address is moved to register H.



Cycles

: 5

States

: 16

Addressing

: direct

Flags

: none

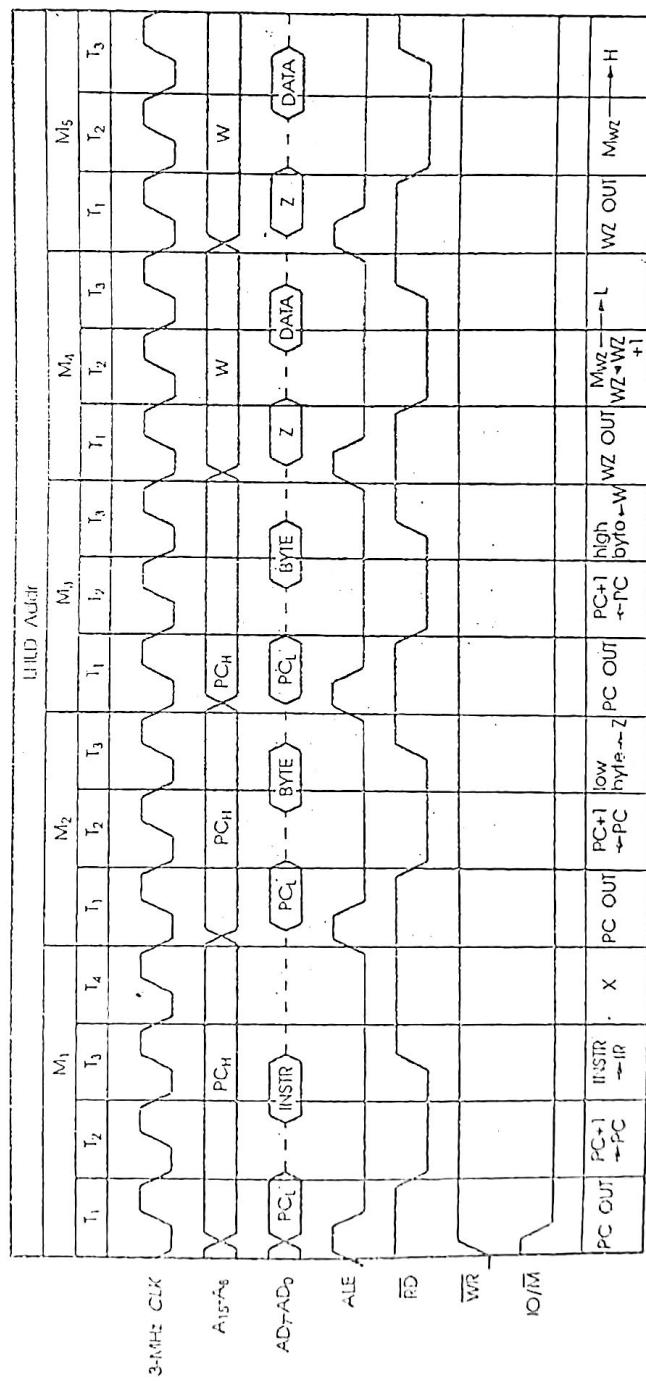


Fig. 2.9. Timing diagram for LHLD addr.

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SHLD addr (Store H and L direct)

((byte 3) (byte 2)) \leftarrow (L)

((byte 3) (byte 2) + 1) \leftarrow (H)

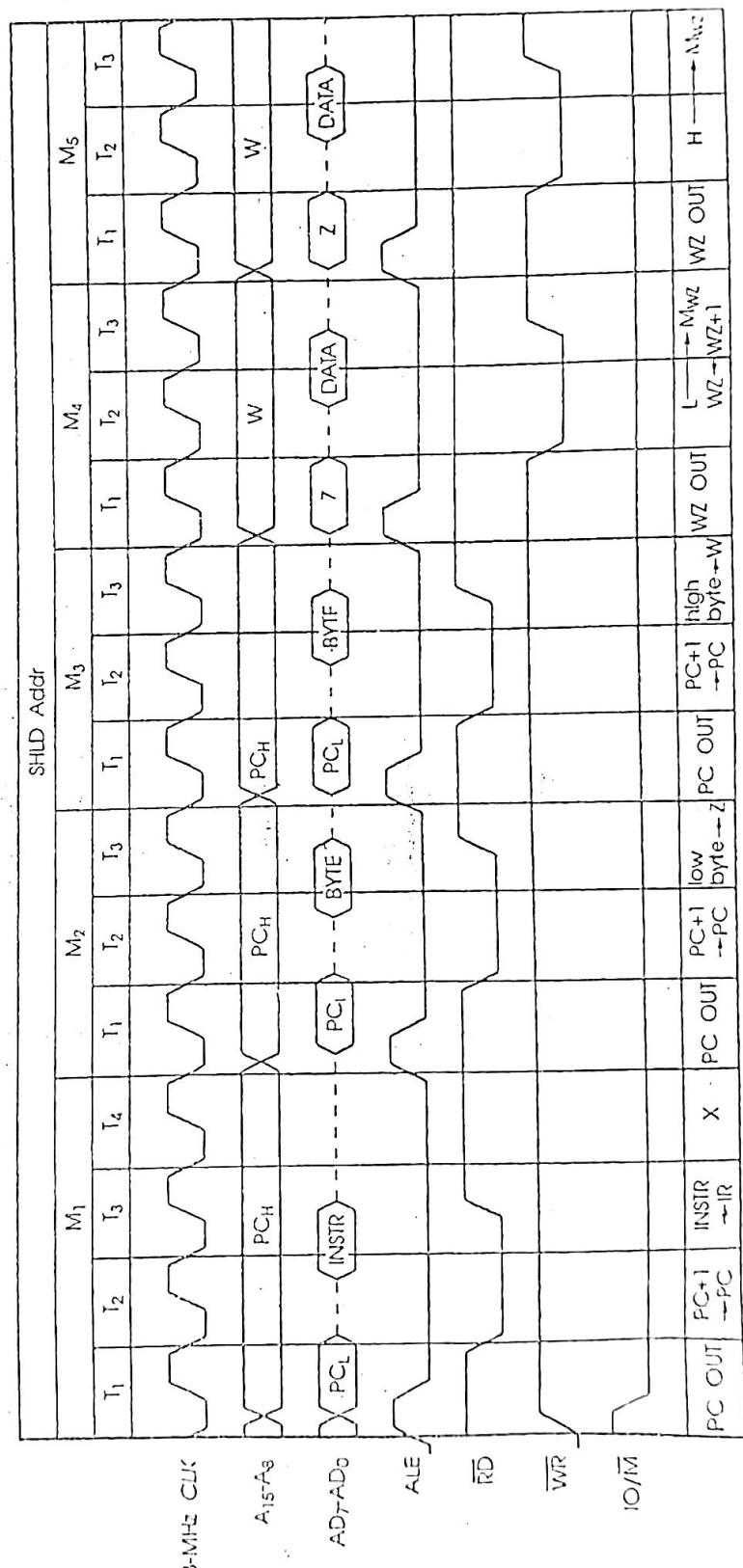


Fig. 2.10. Timing diagram for SHLD addr.

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The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.

0	0	i	0	0	0	1	0
low order addr							
high order addr							

Cycles : 5

States : 16

Addressing : direct

Flags : none

LDAX rp (Load accumulator indirect)

$(A) \leftarrow (rp))$

The content of the memory location, whose address is in the register pair rp, is moved to register A. Note : only register pairs rp = B (registers B and C) or rp = D (registers D and I) may be specified.

0	0	R	P	1	0	1	0
---	---	---	---	---	---	---	---

Cycles : 2

States : 7

Addressing : reg. indirect

Flags : none

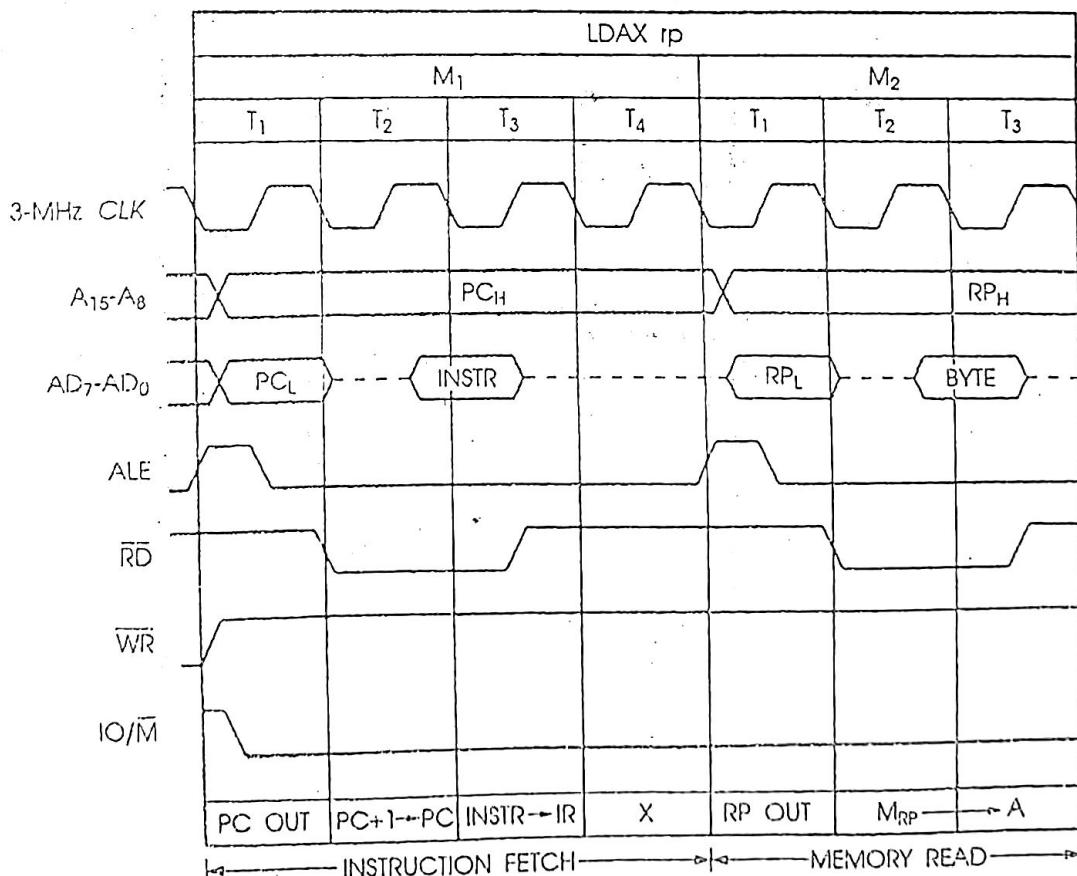


Fig. 2.11. Timing diagram for LDAX rp.

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STAX rp (Store accumulator indirect)
 $((rp)) \leftarrow (A)$

The content of register A is moved to the memory location, whose address is in the register pair rp. Note : only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

0	0	R	P	0	0	1	0
---	---	---	---	---	---	---	---

Cycles : 2
 States : 7
 Addressing : reg. indirect
 Flags : none

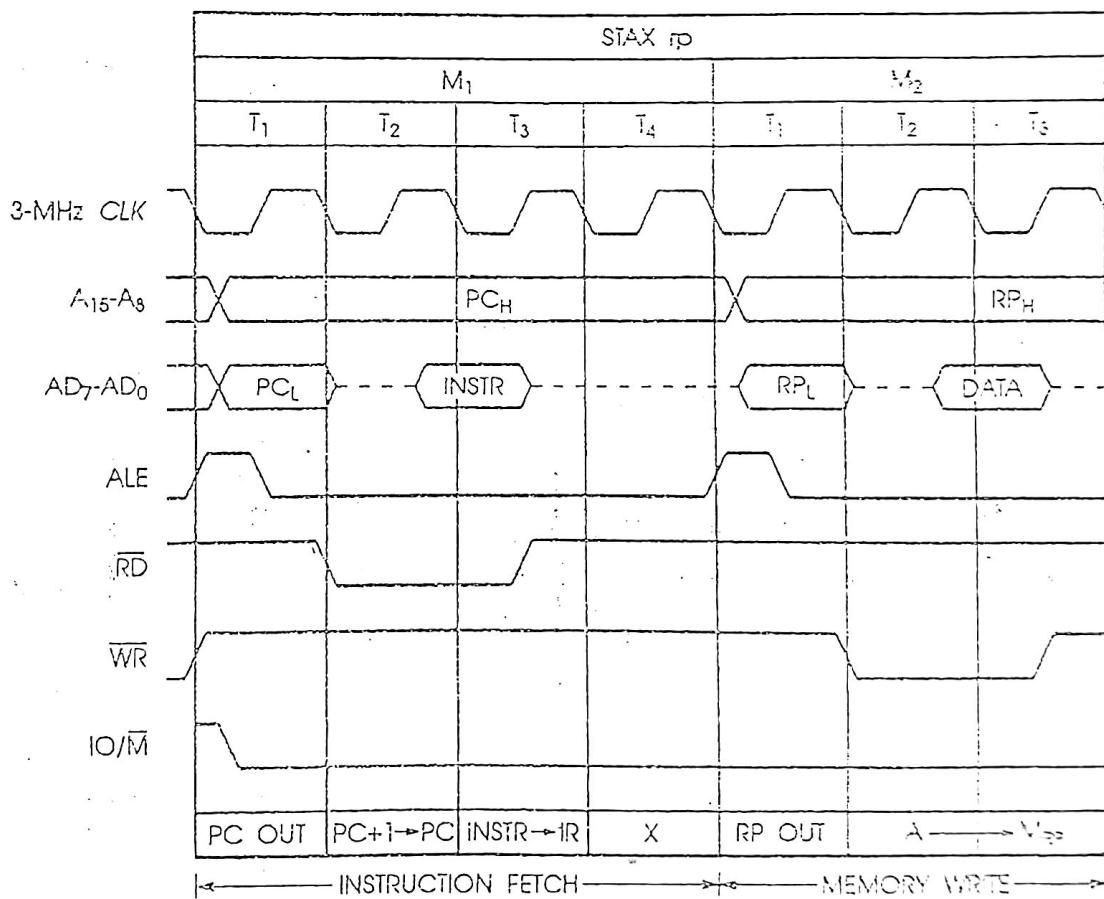


Fig. 2.12. Timing diagram for STAX rp.

XCHG (Exchange H and L with D and E)

(H) \leftrightarrow (D)

(L) \leftrightarrow (E)

The content of register H and L are exchanged with the contents of register D and E.

1	1	1	0	1	0	1	1
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Addressing : register
 Flags : none

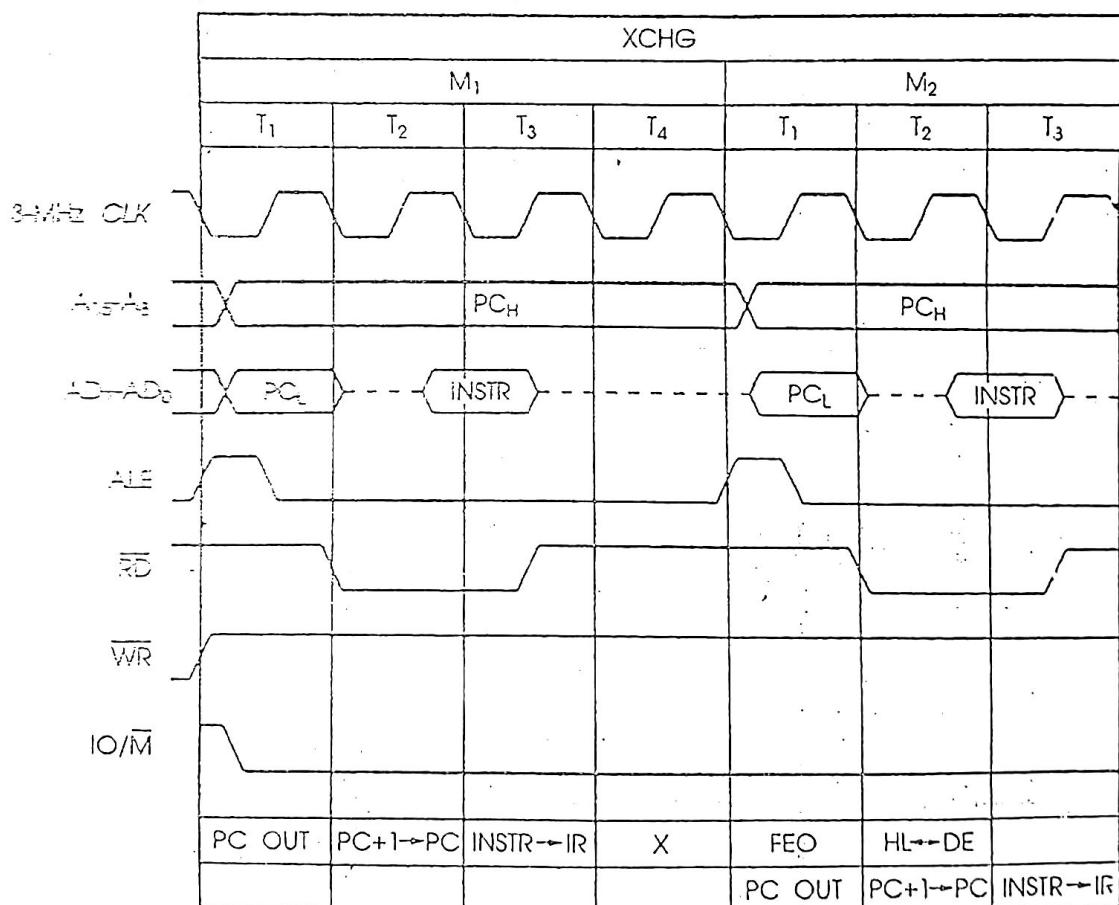


Fig. 2.13. Timing diagram for XCHG.

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2.6.2. ARITHMETIC GROUP

This group of instructions performs arithmetic operations on data in registers and memory.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Carry and Auxillary Carry flags according to the standard rules.

All subtraction operations are performed via two's complement arithmetic and set the carry flag to one to indicate a borrow and clear it to indicate no borrow.

ADD r (Add Register)

$$(A) \leftarrow (A) + (r)$$

The content of register r is added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	0	S	S	S
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Addressing : register
 Flags : Z, S, P, CY, AC

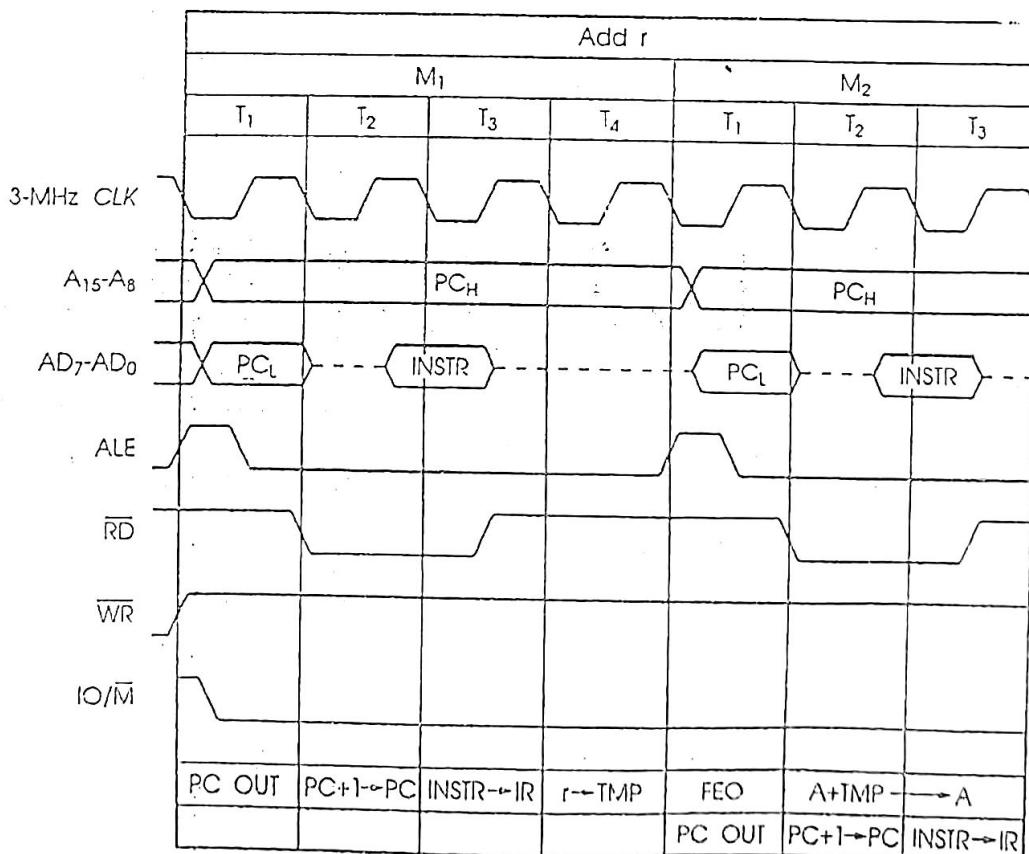


Fig. 2.14. Timing diagram for ADD r.

ADD M (Add memory)
 $(A) \leftarrow (A) + ((H)(L))$

The content of the memory location whose address is contained in the H and L register added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	0	1	1	0
Cycles	: 2						
States	: 7						
Addressing	: reg. indirect						
Flags	: Z, S, P, CY, AC						

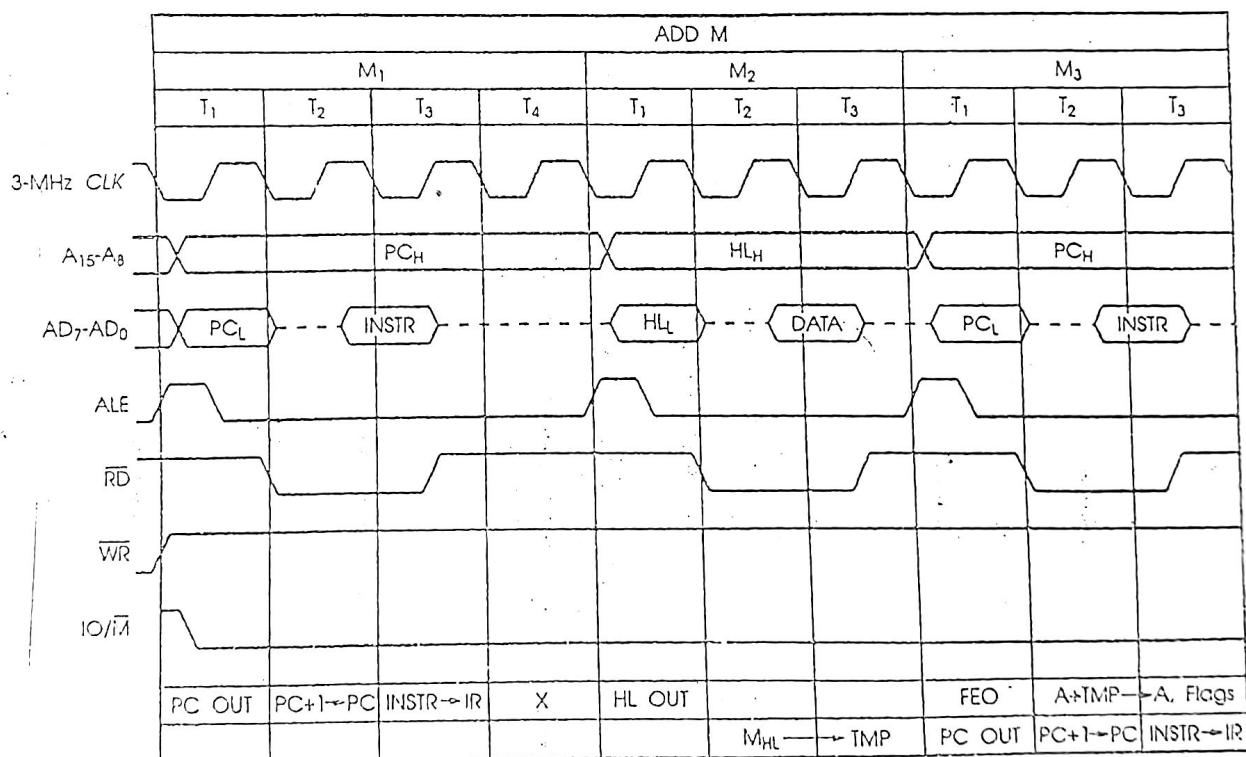


Fig. 2.15. Timing diagram for ADD M.

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ADI data (Add immediate)

$(A) \leftarrow (A) + (\text{byte } 2)$

The content of the second byte of the instruction is added to the content of the accumulator. The result is placed in the accumulator.

1	1	0	0	0	1	1	0
DATA							

Cycles : 2

States : 7

Addressing : immediate

Flags : Z, S, P, CY, AC

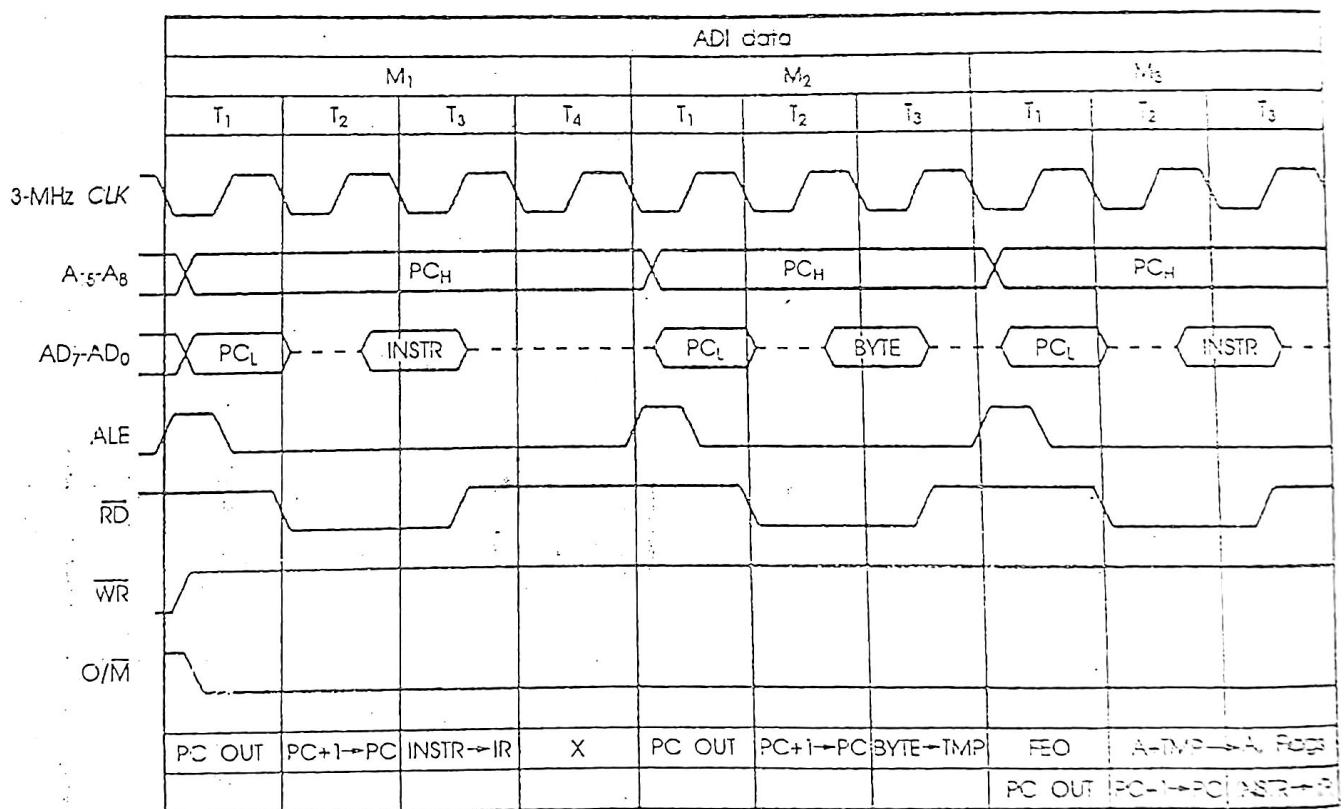


Fig. 2.16. Timing diagram for ADI data.

ADC r (Add Register with carry)

$$(A) \leftarrow (A) + (r) + (CY)$$

The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	1	S	S	S
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Addressing : register
 Flags : Z, S, P, CY, AC

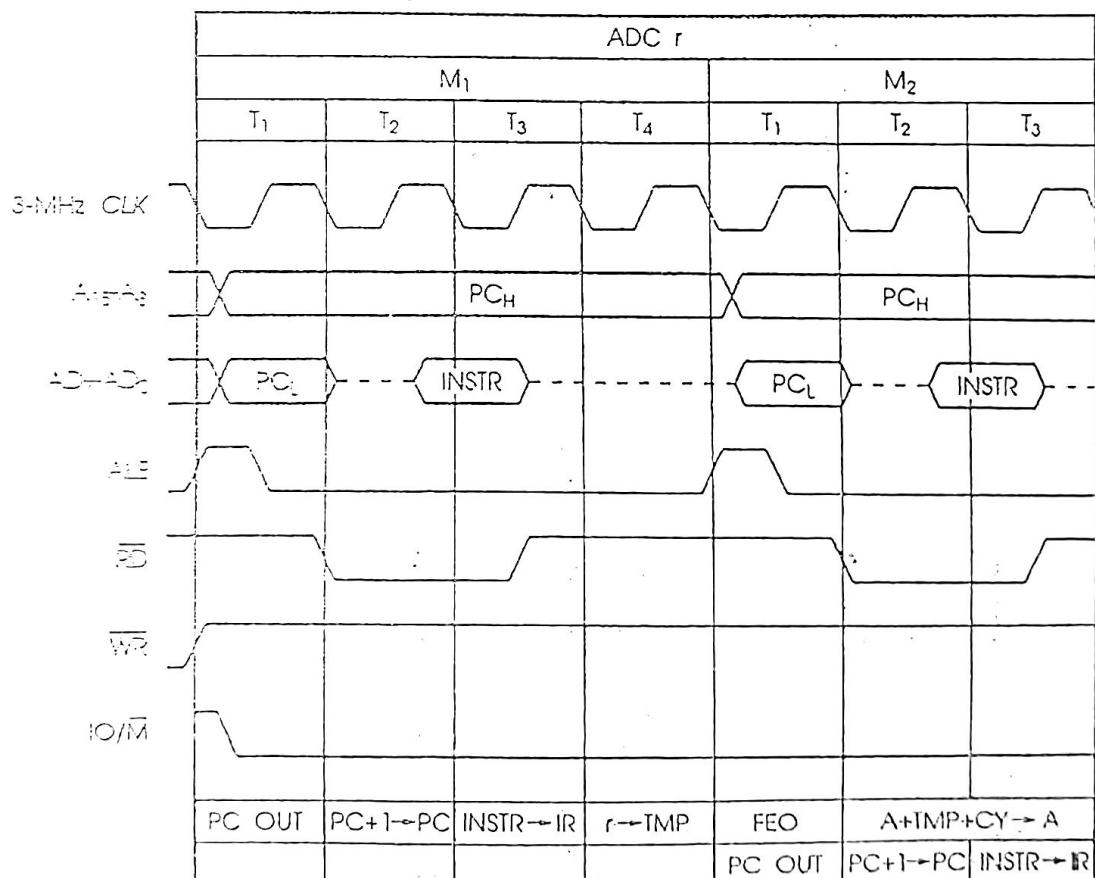


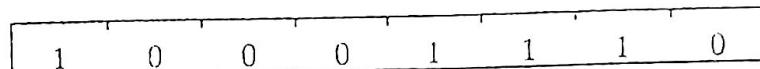
Fig. 2.17. Timing diagram for ADC r.

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ADC M (Add memory with carry)

$$(A) \leftarrow (A) + ((H)(L)) + (CY)$$

The content of the memory location whose address is contained in the H and L register and the the content of the CY flag are added to the accumulator. The result is placed in the accumulator.



Cycles : 2
 States : 7
 Addressing : reg. indirect
 Flags : Z, S, P, CY, AC

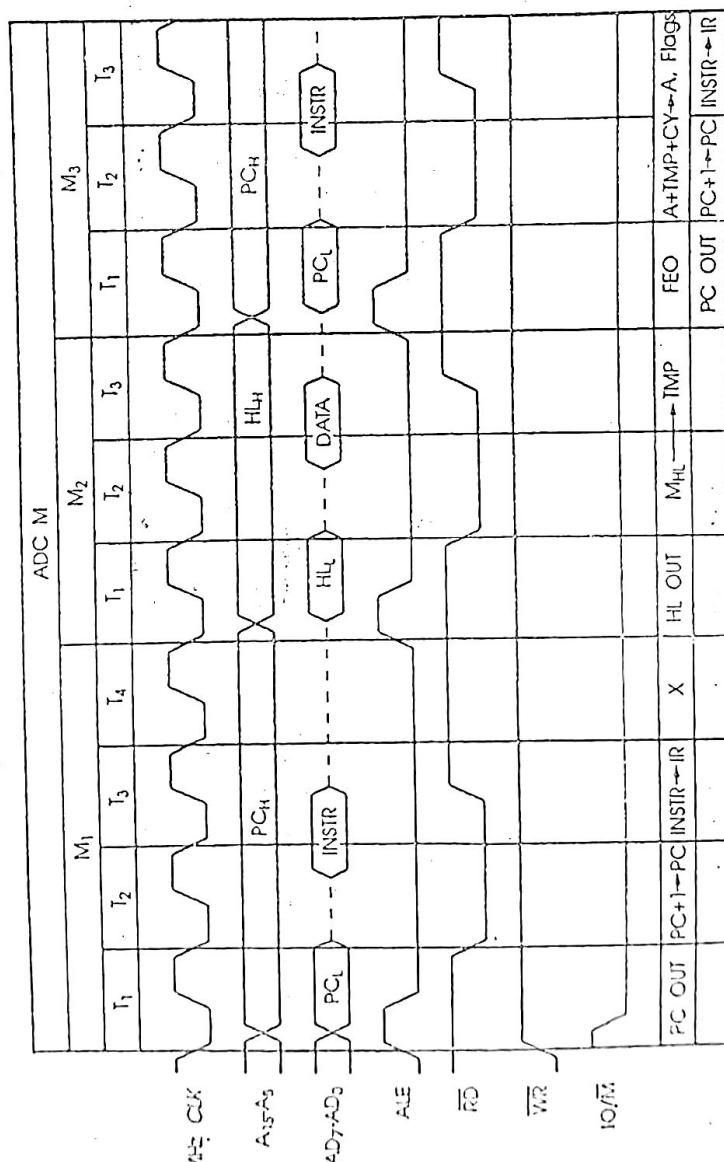


Fig. 2.18. Timing diagram for ADC M.

ACI data (Add immediate with carry)

$$(A) \leftarrow (A) + (\text{byte } 2) + (\text{CY})$$

The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.

1	1	0	0	1	1	1	0
DATA							

Cycles : 2

States : 7

Addressing : immediate

Flags : Z, S, P, CY, AC

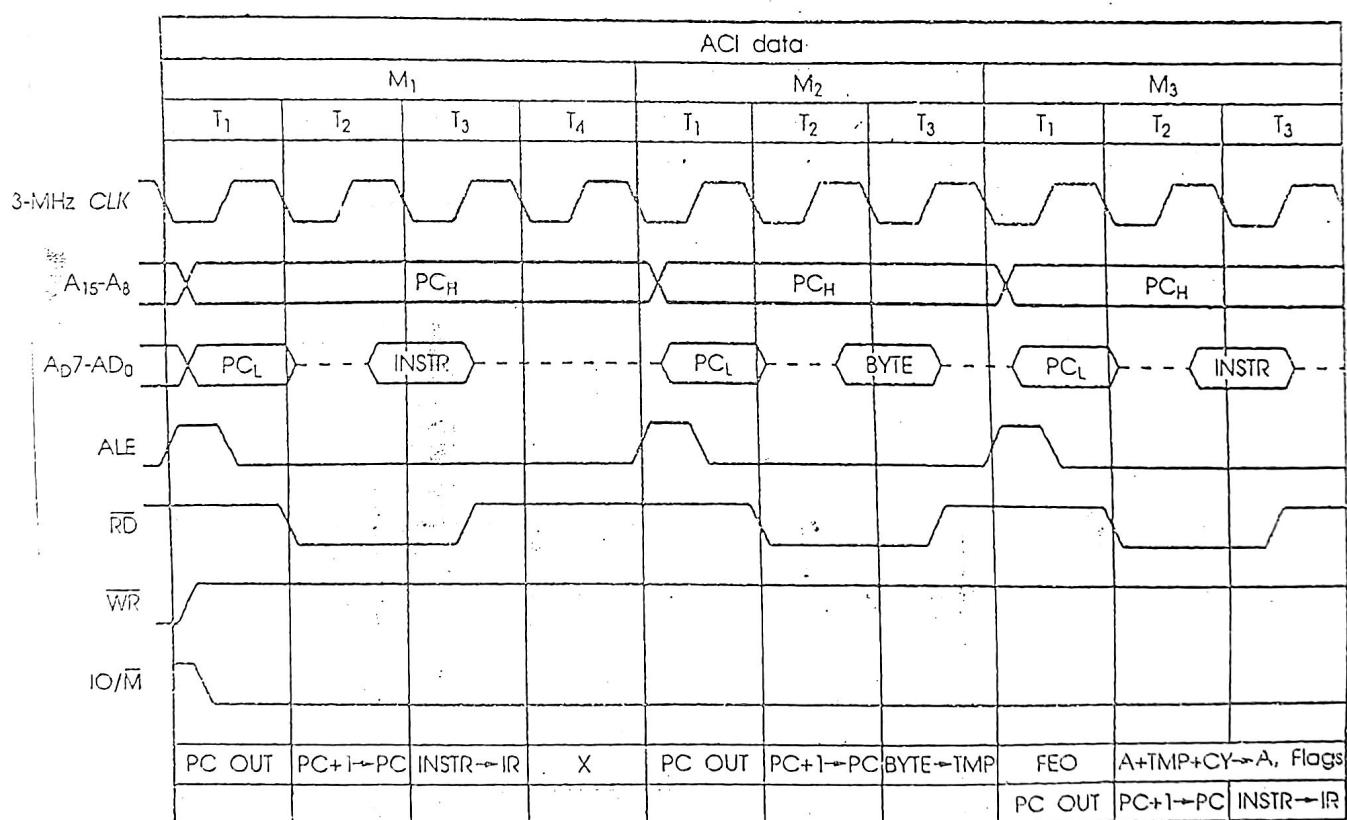


Fig. 2.19. Timing diagram for ACI data.

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.SUB r (Subtract Register)

$$(\hat{A}) \leftarrow (\hat{A}) - (r)$$

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.

1 0 0 1 0 S S S

Cycles : 1

States : 4

Addressing : register

Flags : Z, S, P, CY, AC

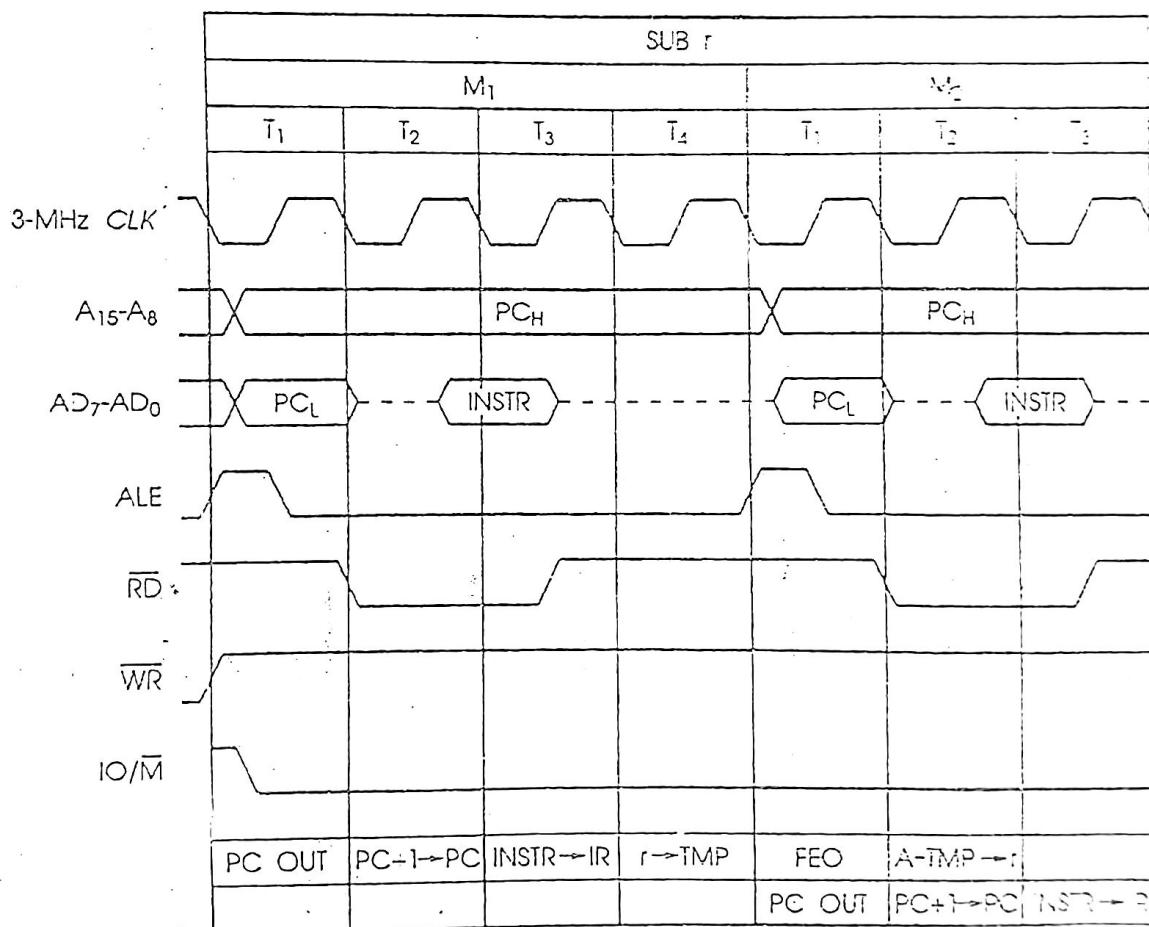


Fig. 2.20. Timing diagram for SUB r.

SUB M (Subtract memory)

$(A) \leftarrow (A) - ((H)(L))$

The content of the memory location whose address is contained in the H and L registers is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	0	0	1	0	1	1	1	0
---	---	---	---	---	---	---	---	---

Cycles : 2

States : 7

Addressing : reg, indirect

Flags : Z, S, P, CY, AC

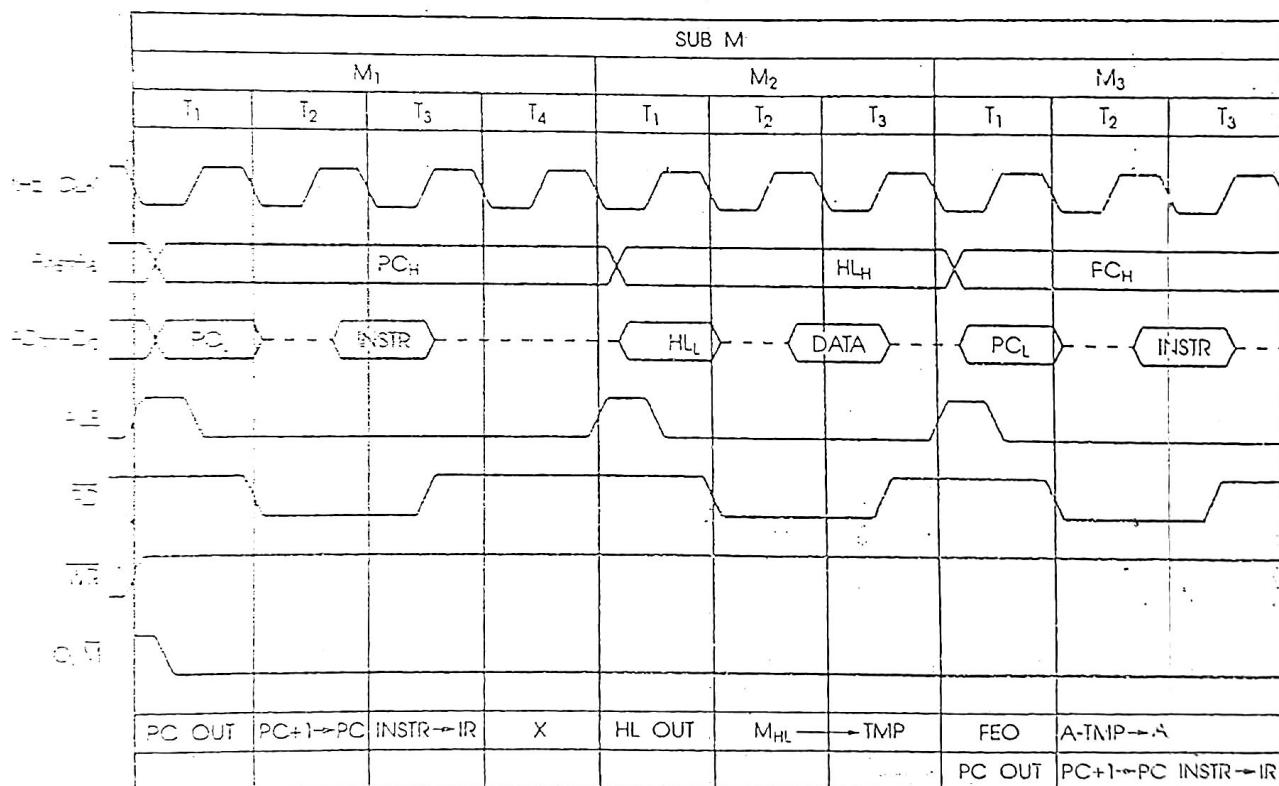


Fig. 2.21 Timing diagram for S-UBM

SUI data (Subtract Immediate)

$$(A) \leftarrow (A) - (\text{byte } 2)$$

The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	1	0	1	0	1	1	0
data							

Cycles : 2
 States : 7
 Addressing : immediate
 Flags : Z, S, P, CY, AC

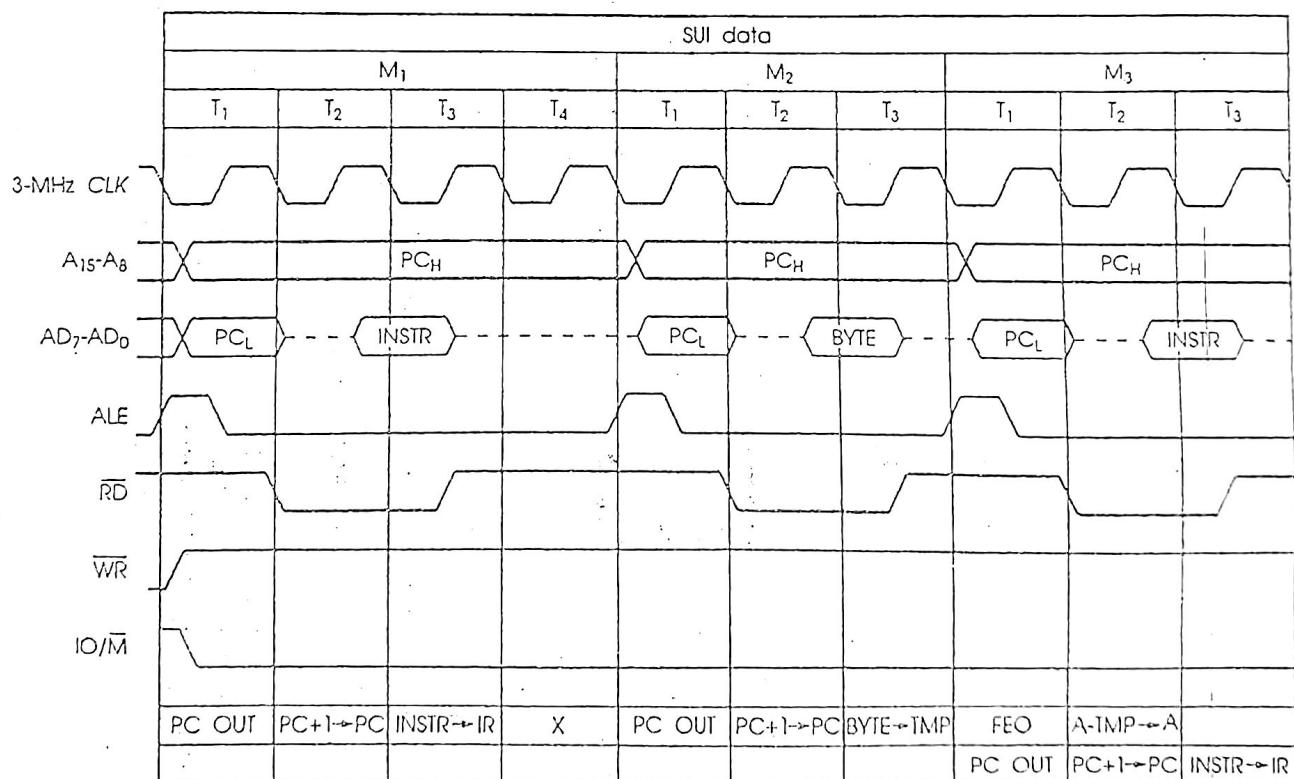


Fig. 2.22. Timing diagram for SUI data.

SBB r (Subtract Register with borrow)

$$(A) \leftarrow (A) - (r) - (\text{CY})$$

The content of register r and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	0	0	1	1	S	S	S
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Addressing : register
 Flags : Z, S, P, CY, AC

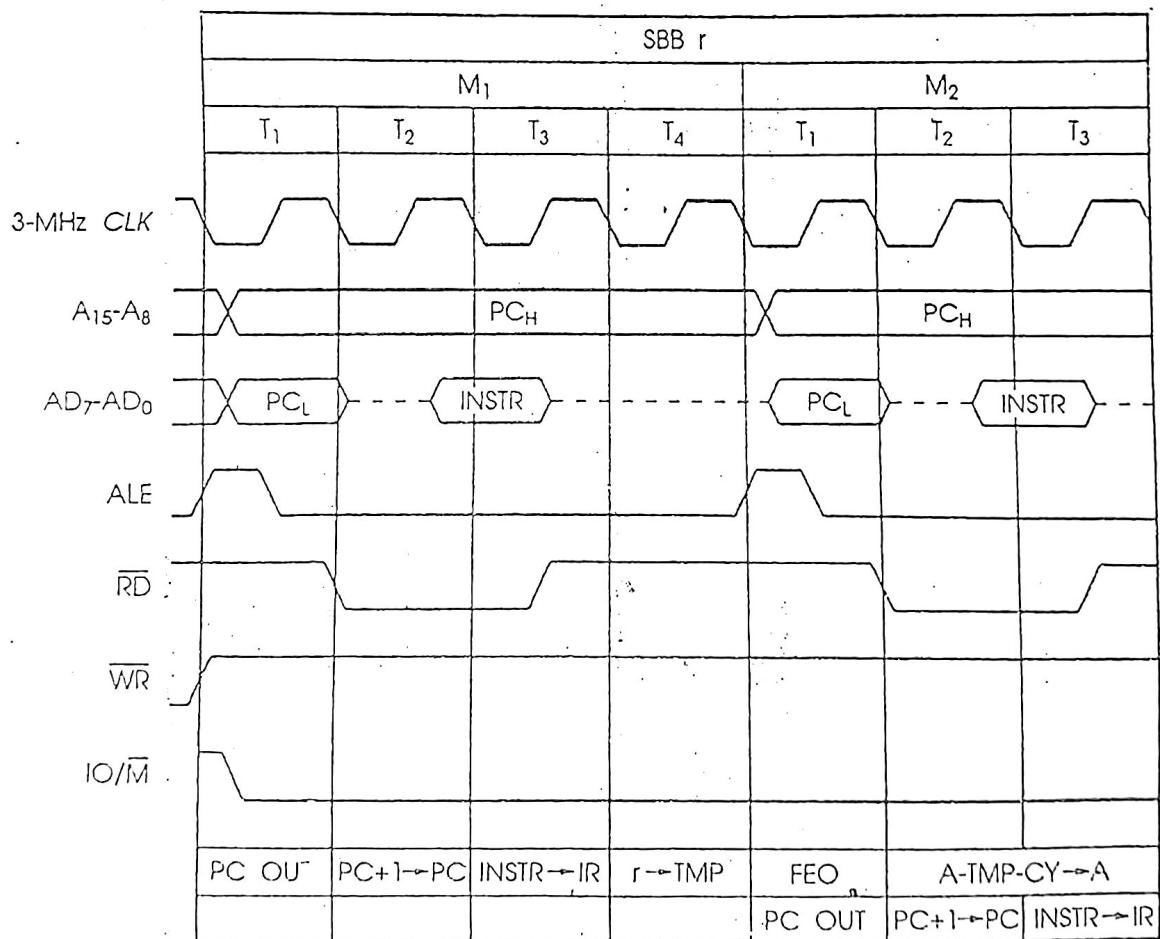


Fig. 2.23. Timing diagram for SBB r instruction.

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SBB M (Subtract memory with borrow)

$$(A) \leftarrow (A) - ((H)(L)) - (CY)$$

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	0	0	1	1	1	1	0	
---	---	---	---	---	---	---	---	--

Cycles : 2
 States : 7
 Addressing : reg. indirect
 Flags : Z, S, P, CY, AC

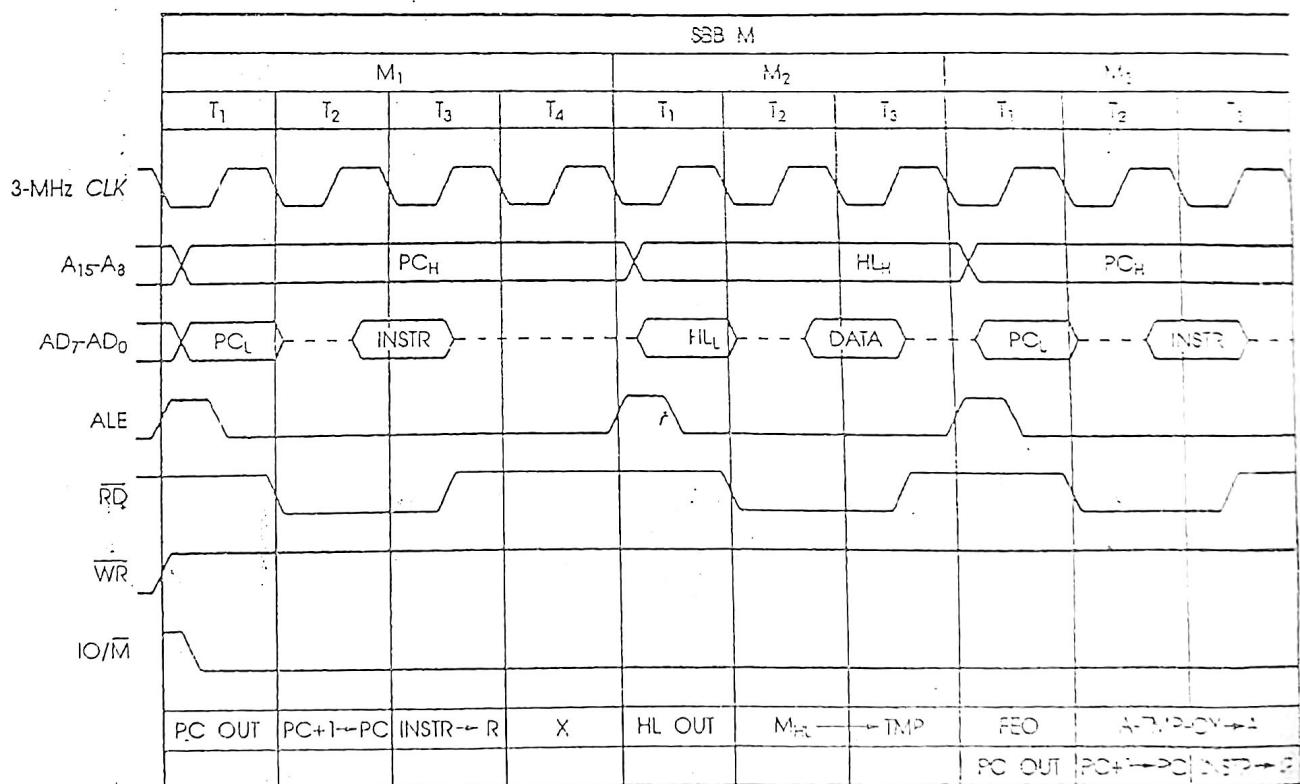


Fig. 2.24. Timing diagram for SBB M.

SBI data (Subtract immediate with borrow)

$$(A) \leftarrow (A) - (\text{byte } 2) - (\text{CY})$$

The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	1	0	1	0	1	1	0
data							

Cycles : 2
 States : 7
 Addressing : immediate
 Flags : Z, S, P, CY, AC

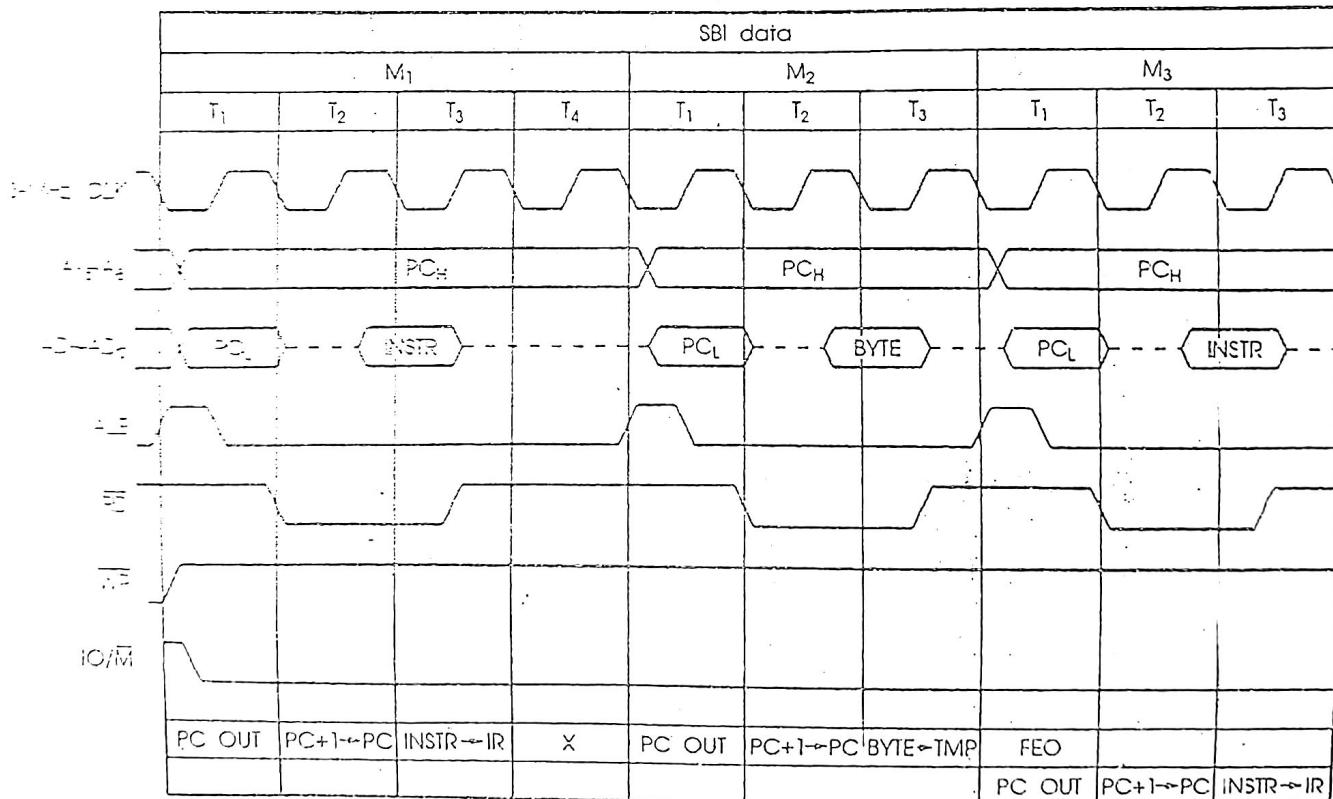


Fig. 2.25. Timing diagram for SBI data.

INR r (Increment Register)

$$(r) \leftarrow (r) + 1$$

The content of register r is incremented by one. Note : All condition flags except CY are affected.

0	0	D	D	D	1	0	0
---	---	---	---	---	---	---	---

Cycles : 1

States : 4

Addressing : register

Flags : Z, S, P, AC

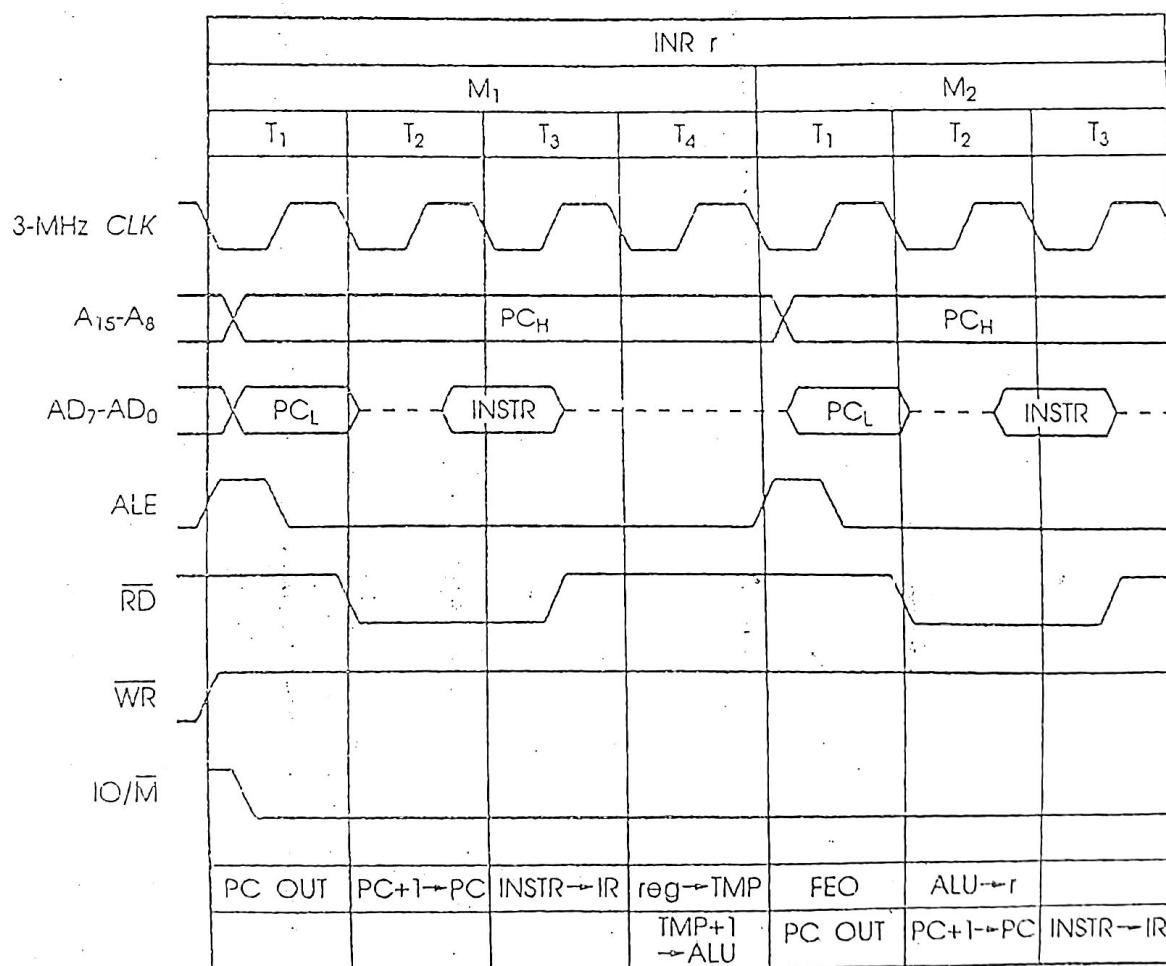
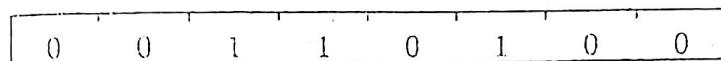


Fig. 2.26. Timing for INR r.

INR M (Increment memory)

$$((H)(L)) \leftarrow ((H)(L)) + 1$$

The content of the memory location whose address is contained in the H and L registers is incremented by one. Note : All condition flags except CY are affected.



Cycles : 3
 States : 10
 Addressing : reg. indirect
 Flags : Z, S, P, AC

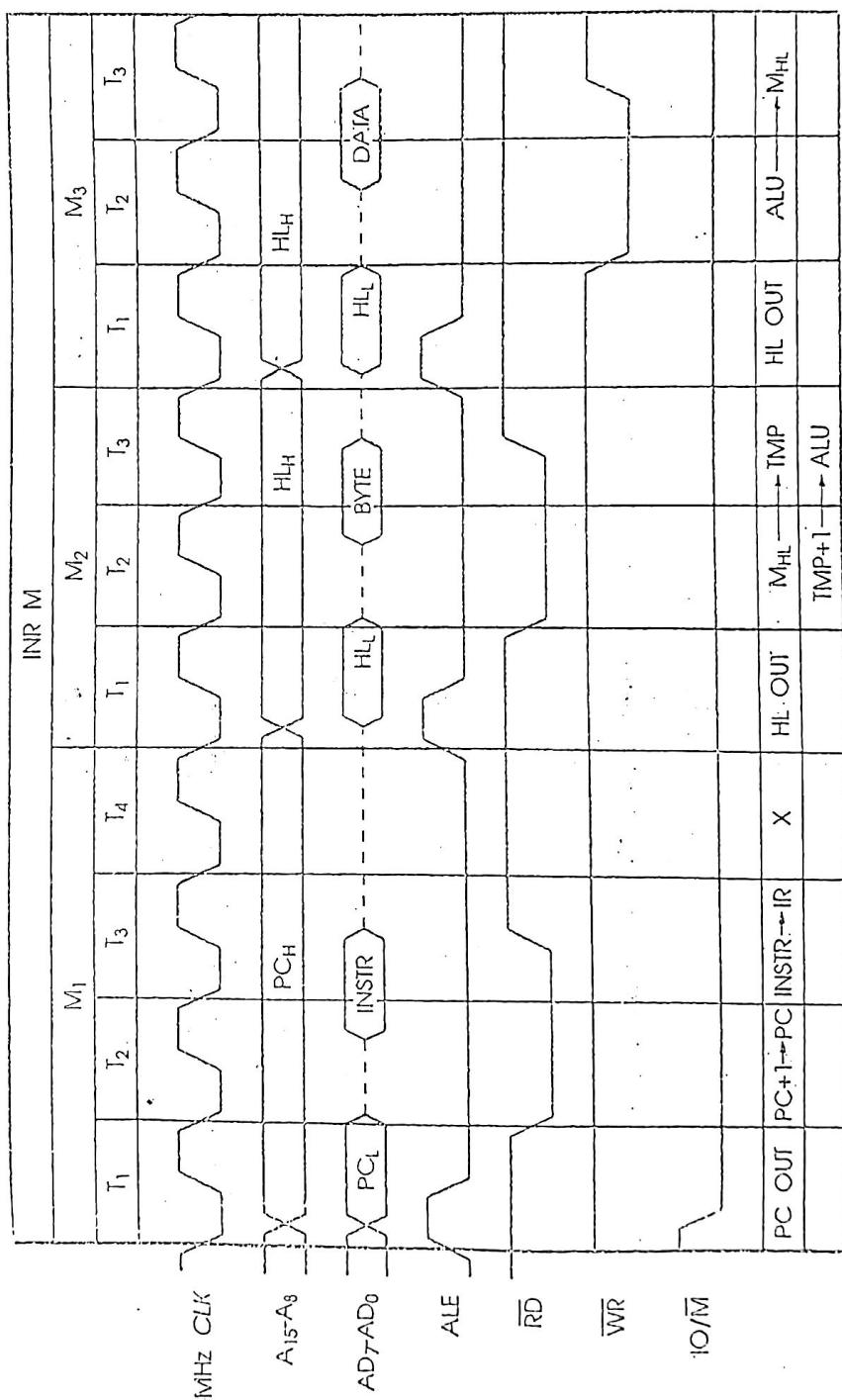


Fig. 2.27. Timing diagram for INR M.

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• DCR r (Decrement Register)

$$(r) \leftarrow (r) - 1$$

The content of register r is decremented by one. Note : All condition flags except CY are affected.

0	0	D	D	D	1	0	1
---	---	---	---	---	---	---	---

Cycles : 1

States : 4

Addressing : register

Flags : Z, S, P, AC

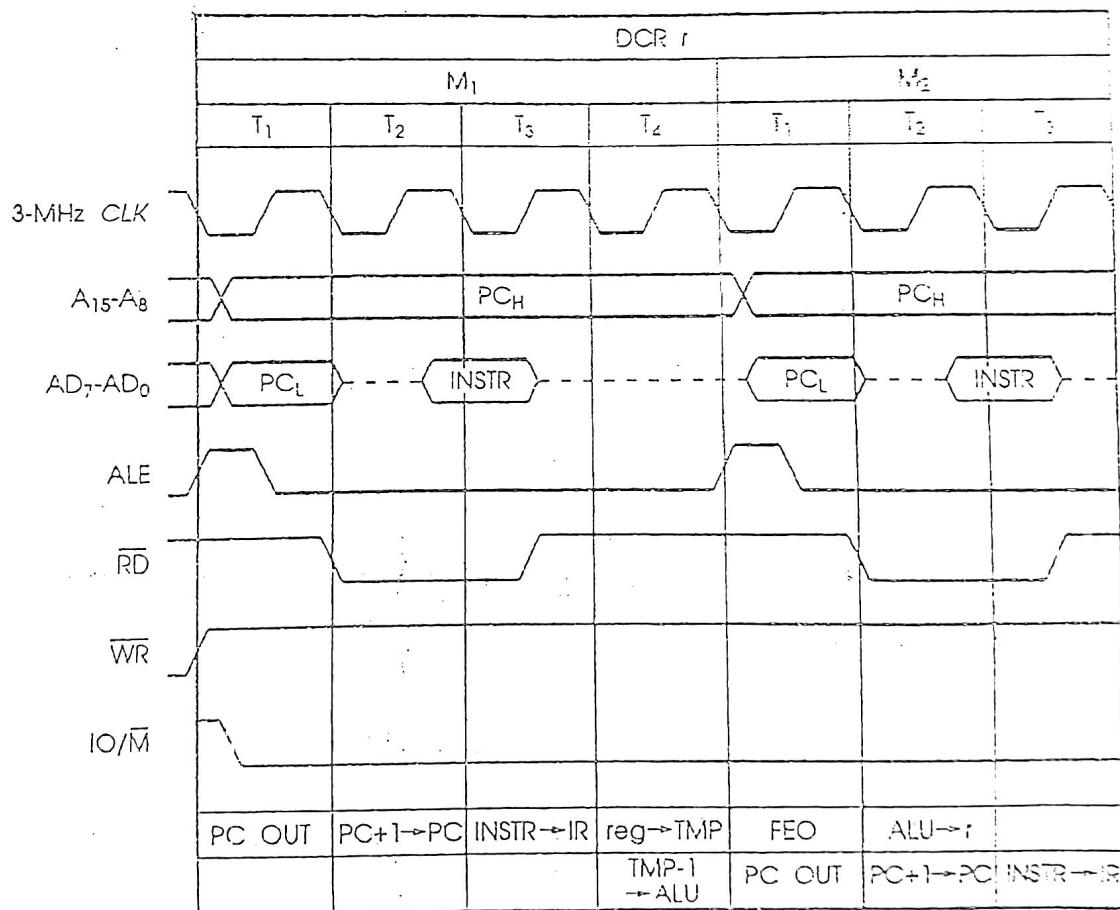


Fig. 2.28. Timing diagram for DCR r.

DCR M (Decrement memory)

$$((H)(L)) \leftarrow ((H)(L)) - 1$$

The content of the memory location whose address is contained in the H and L registers is decremented by one. Note : All condition flags except CY are affected.

0	0	1	1	0	1	0	1
Cycles	: 3						
States	: 10						
Addressing	: reg. indirect						
Flags	: Z, S, P, AC						

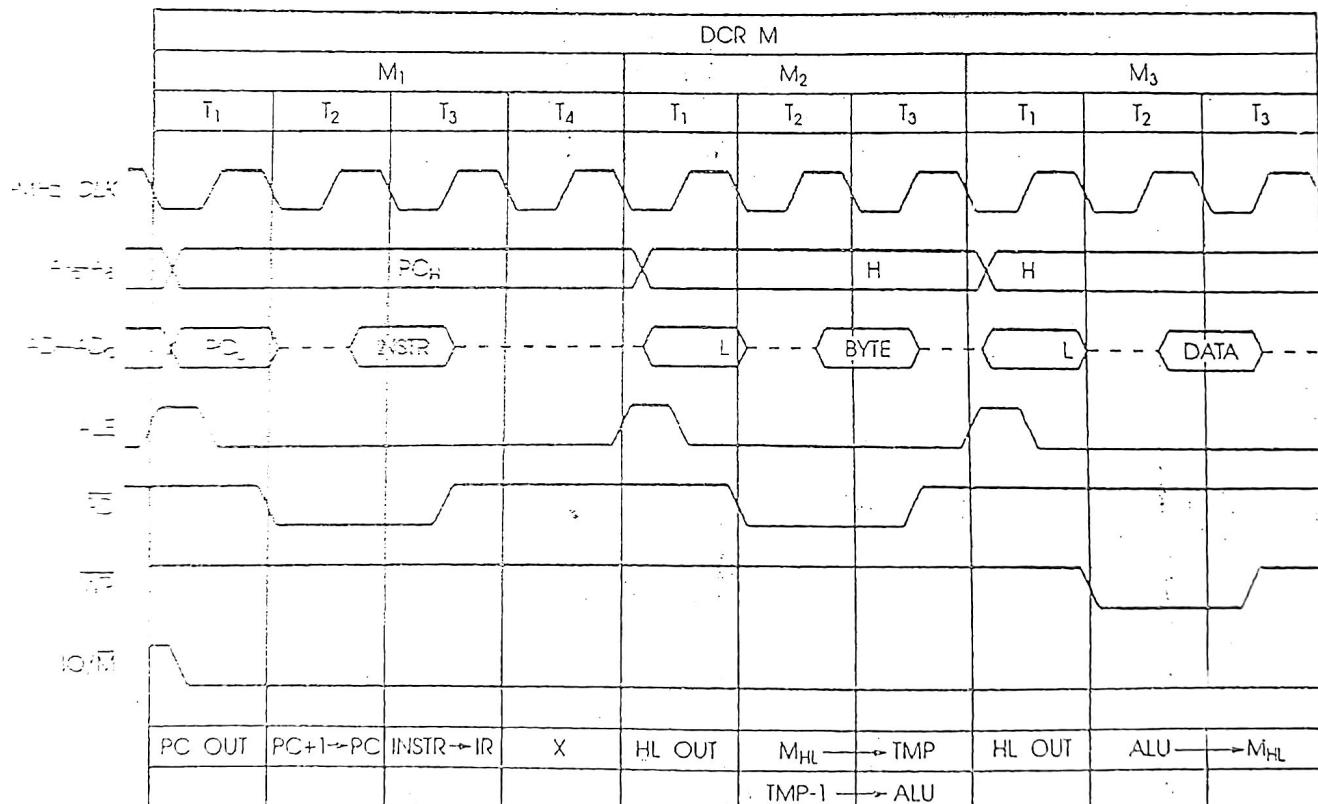


Fig. 2.29. Timing diagram for DCR M.

INX rp (Increment register pair)

$$(rh) (rl) \leftarrow (rh) (rl) + 1$$

The content of the register pair rp is incremented by one. Note : No condition flags are affected.

0	0	R	P	1	0	1	1
---	---	---	---	---	---	---	---

Cycles : 1
 States : 6
 Addressing : register
 Flags : none

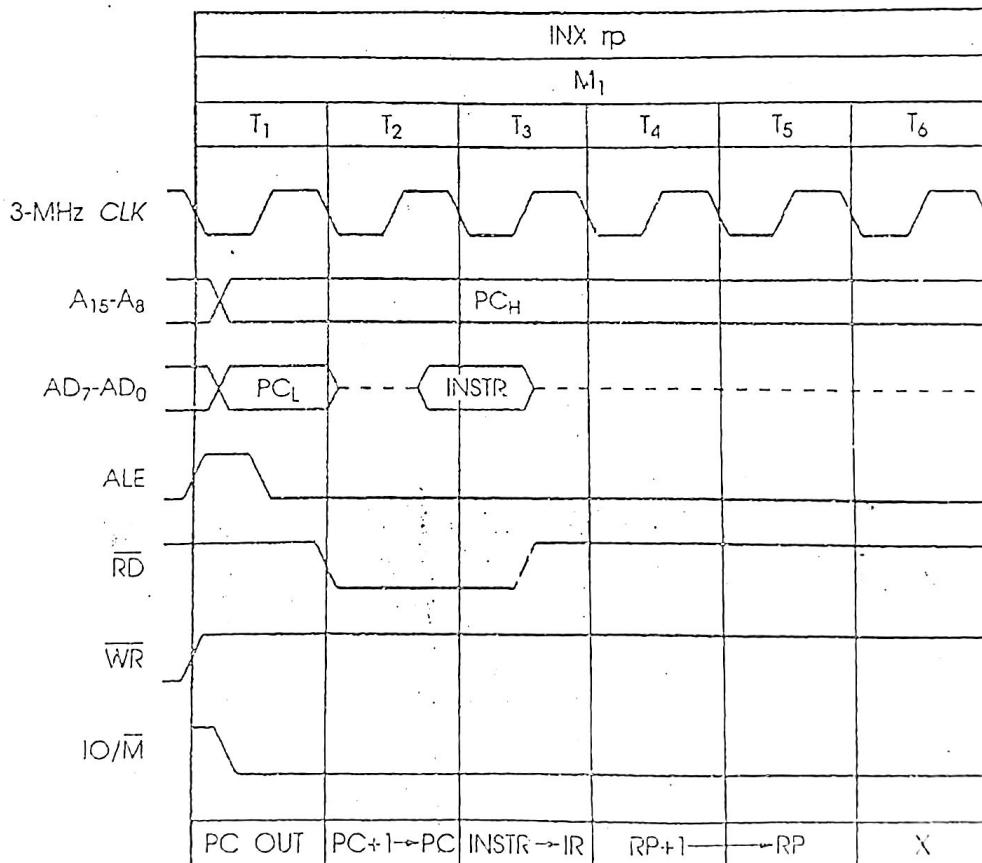


Fig. 2.30. Timing diagram for INX rp.

DCX rp (Decrement register pair)

$$(rh) (rl) \leftarrow (rh) (rl) - 1$$

The content of the register pair rp is decremented by one. Note : No condition flags are affected.

0	0	R	P	1	0	1	1
---	---	---	---	---	---	---	---

Cycles : 1

States : 6

Addressing : register

Flags : none

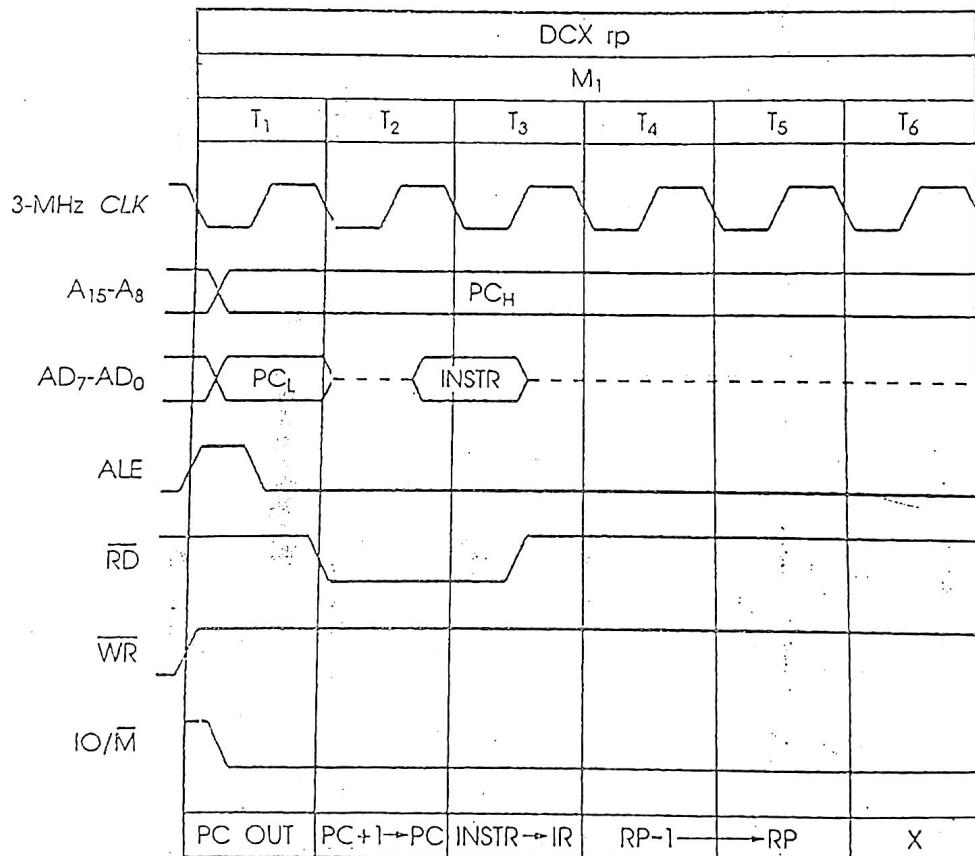


Fig. 2.31. Timing diagram for DCX rp.

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DAD rp (Add register pair to H and L)

$$(H)(L) \leftarrow (H)(L) + (rh)(rl)$$

The content of the register pair rp is added to the content of the register pair H and L. The result is placed in the register pair H and L. Note : Only the CY flag is affected. It is set if there is a carry out of the double precision add; otherwise it is reset.

0	0	R	P	1	0	0	1
---	---	---	---	---	---	---	---

Cycles : 3

States : 10

Addressing : register

Flags : CY

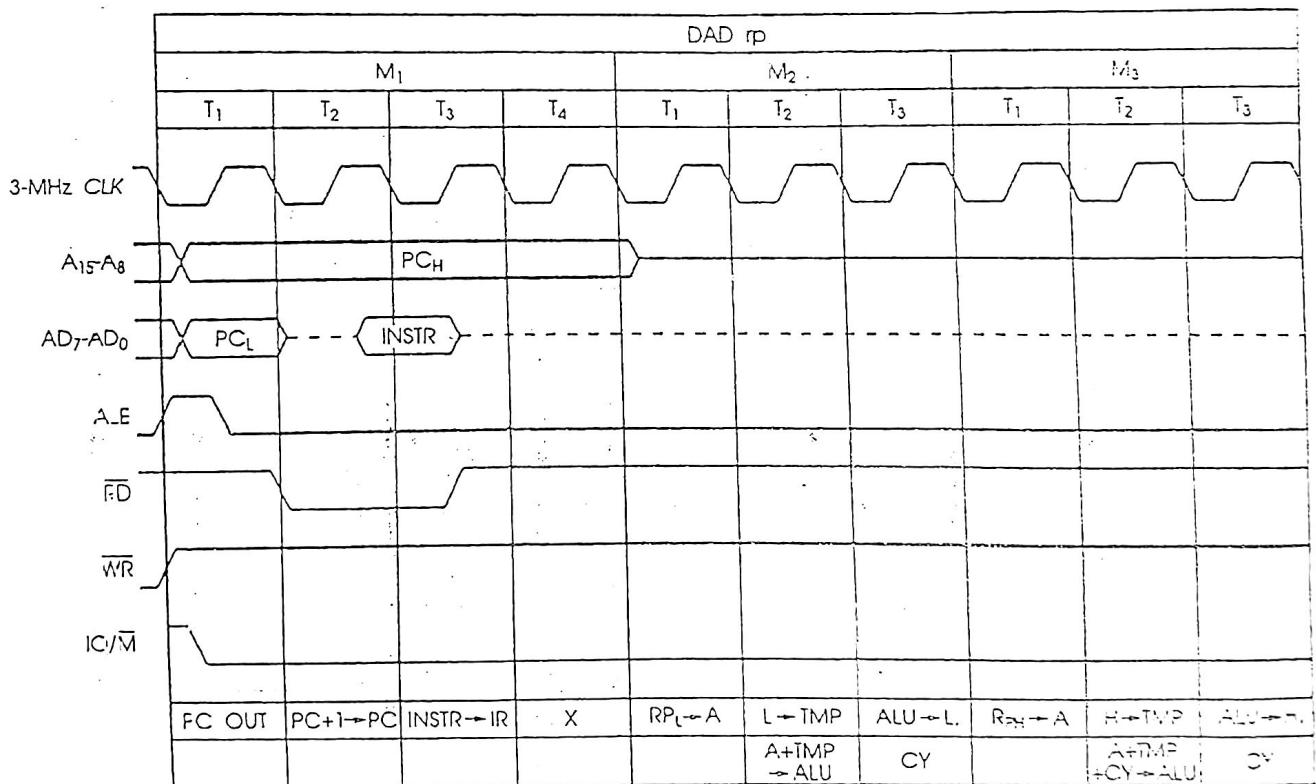


Fig.2.32. Timing diagram for DAD rp

DAA (Decimal Adjust Accumulator)

The eight bit number in the accumulator is adjusted to form two four-bit Binary-Coded-Decimal digits by the following process :

1. If the value of the least significant 4 bits of the accumulator is greater than 9 or if the AC flag is set, 6 is added to the accumulator.
 2. If the value of the most significant 4 bits of the accumulator is now greater than 9, or if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.
- Note : All flags are affected.

0	0	1	0	0	1	1	1
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Flags : Z, S, P, CY, AC

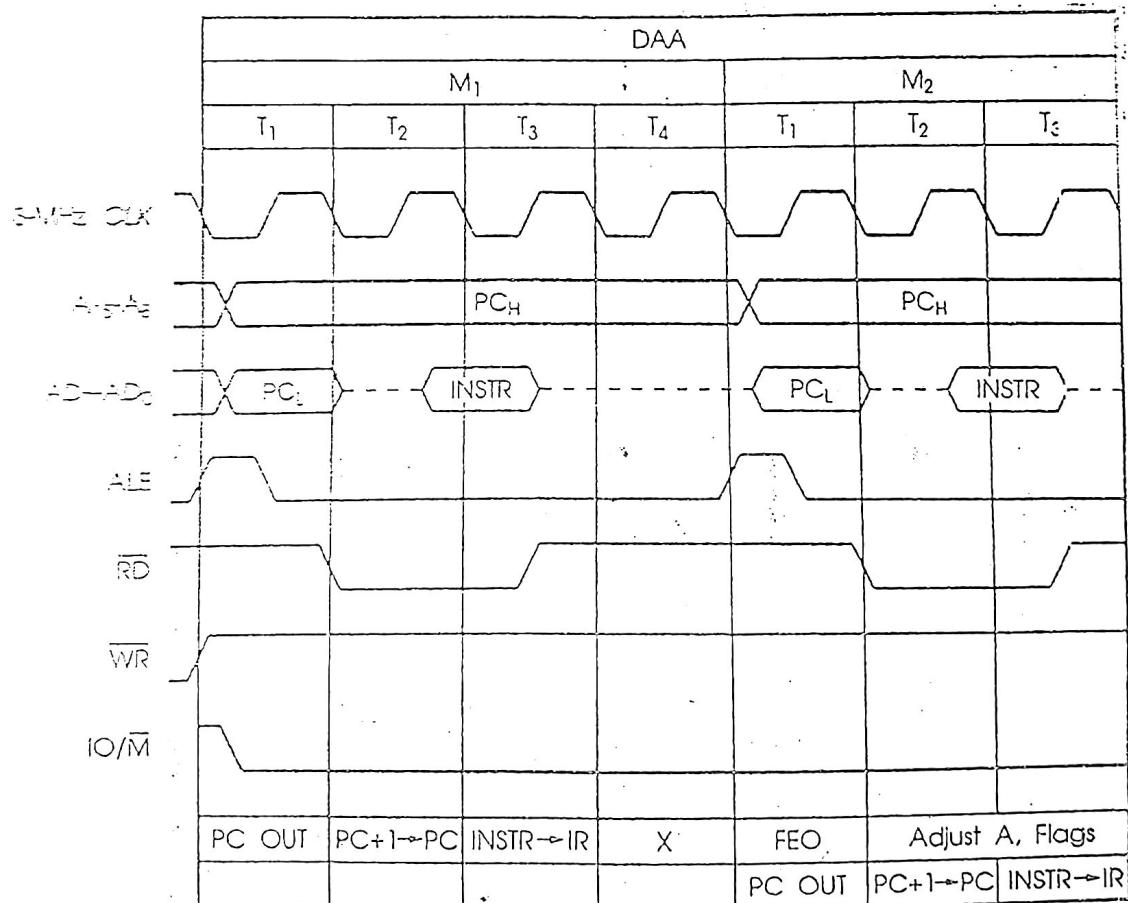


Fig. 2.33. Timing diagram for DAA.

2.6.3 LOGIC GROUP

This group of instruction performs logical (Boolean) operations on data in registers and memory and on condition flags.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Auxiliary Carry and Carry flags according to the standard rules.

ANA r (AND Register)

$(A) \leftarrow (A) \wedge (r)$

The content of register r is logically ANDed with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared and AC is set.

1	0	1	0	0	S	S	S
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Addressing : register
 Flags : Z, S, P, CY, AC

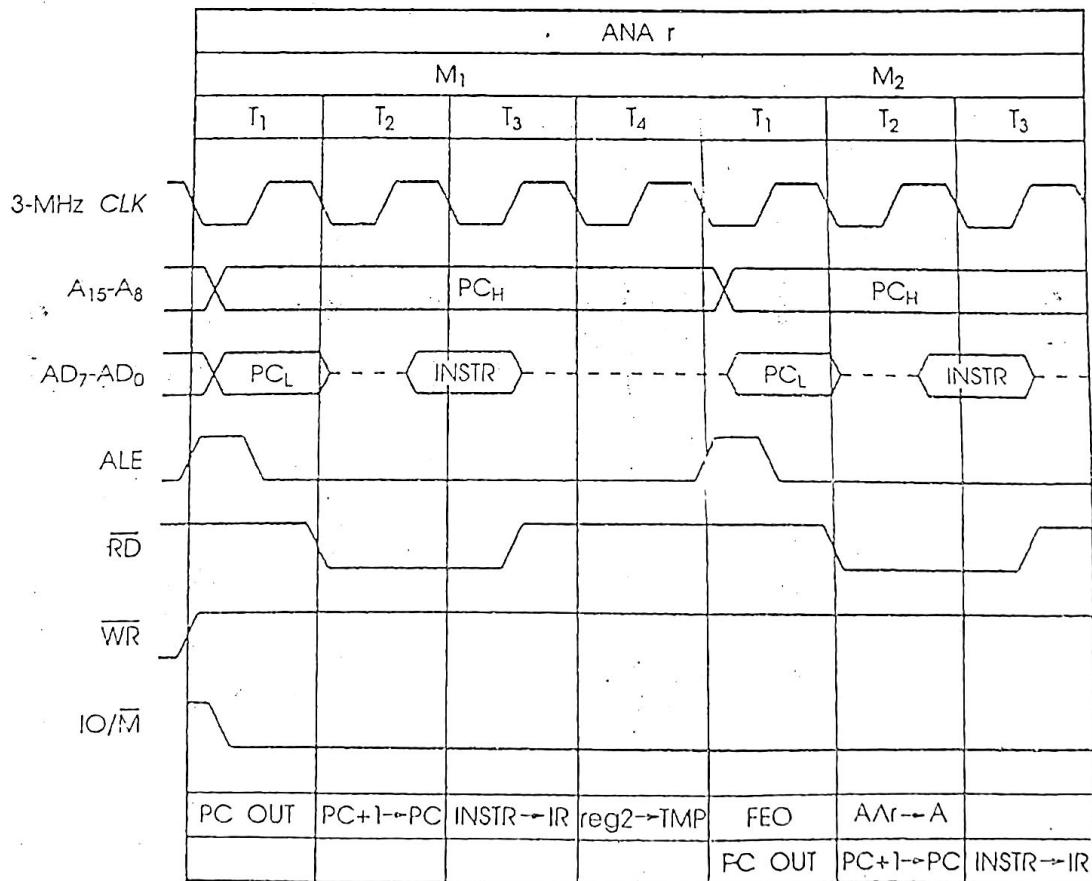


Fig. 2.34. Timing diagram for ANA r.

ANA M (AND memory)

$$(A) \leftarrow (A) \wedge ((H)(L))$$

The contents of the memory location whose address is contained in the H and L registers is logically ANDed with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared and AC is set.

1	0	1	0	0	1	1	0
---	---	---	---	---	---	---	---

Cycles : 2
 States : 7
 Addressing : reg. indirect
 Flags : Z, S, P, CY, AC

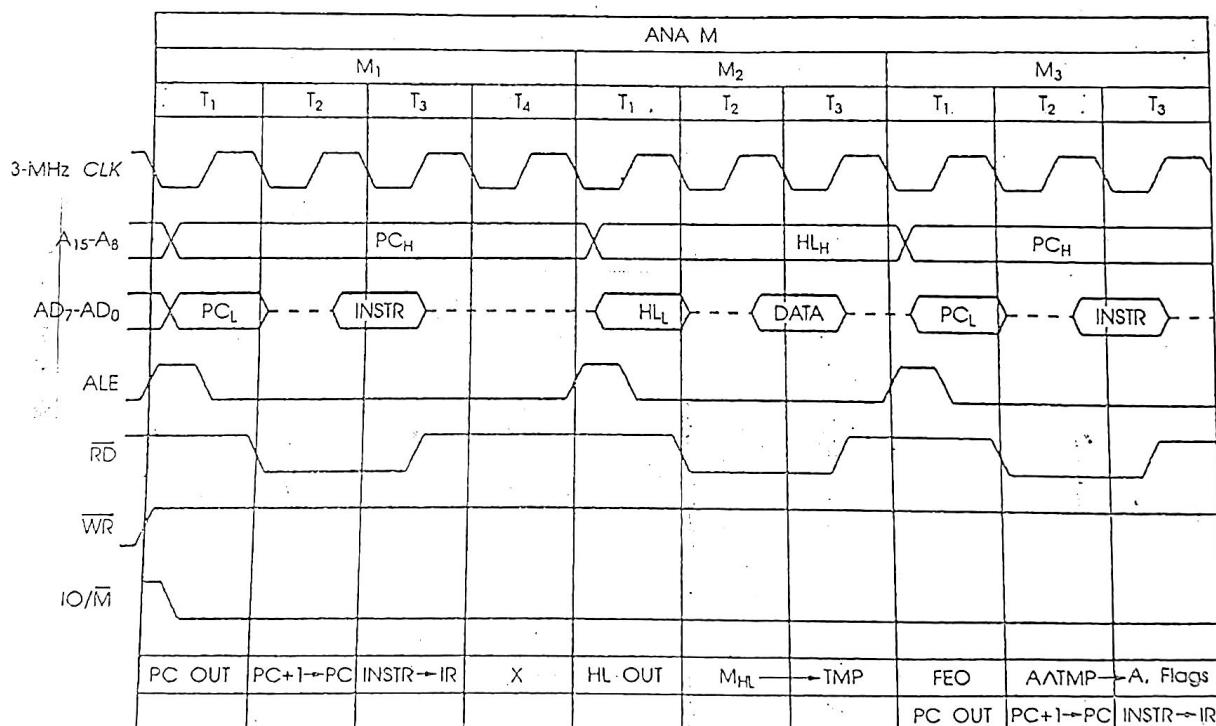


Fig. 2.35. Timing diagram for ANA M instruction.

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ANI data - (AND immediate)

$$(A) \leftarrow (A) \wedge (\text{byte } 2)$$

The content of the second byte of the instruction is logically ANDed with the contents of the accumulator. The result is placed in the accumulator. The CY flag is cleared and AC is set.

1	1	1	0	0	1	1	0
data							

Cycles	: 2
States	: 7
Addressing	: immediate
Flags	: Z, S, P, CY, AC

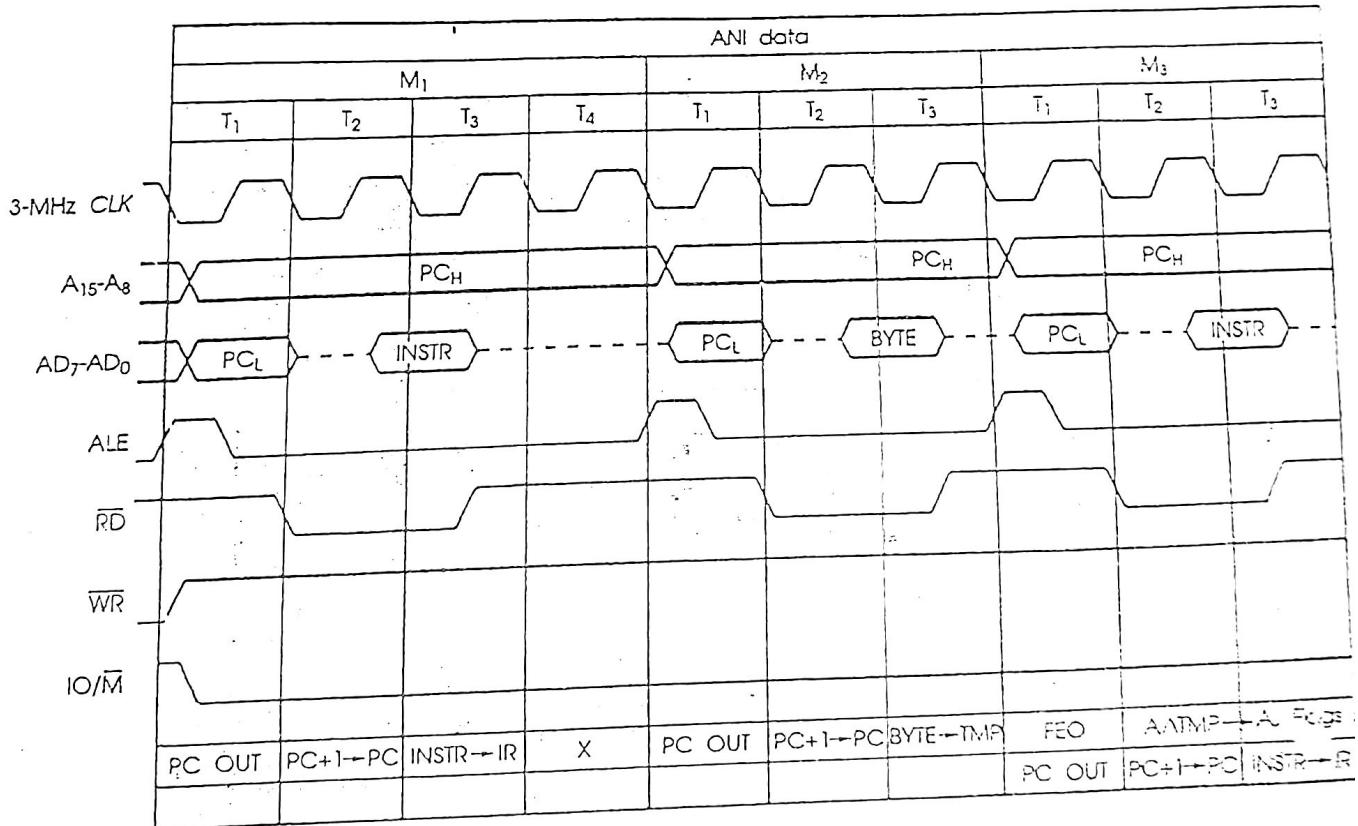


Fig. 2.36. Timing diagram for ANI data.

XRA r (Exclusive OR Register)

$$A \leftarrow A \vee r$$

The content of register r is exclusive OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	0	1	S	S	S
Cycles	: 1						
States	: 4						
Addressing	: register						
Flags	: Z, S, P, CY, AC						

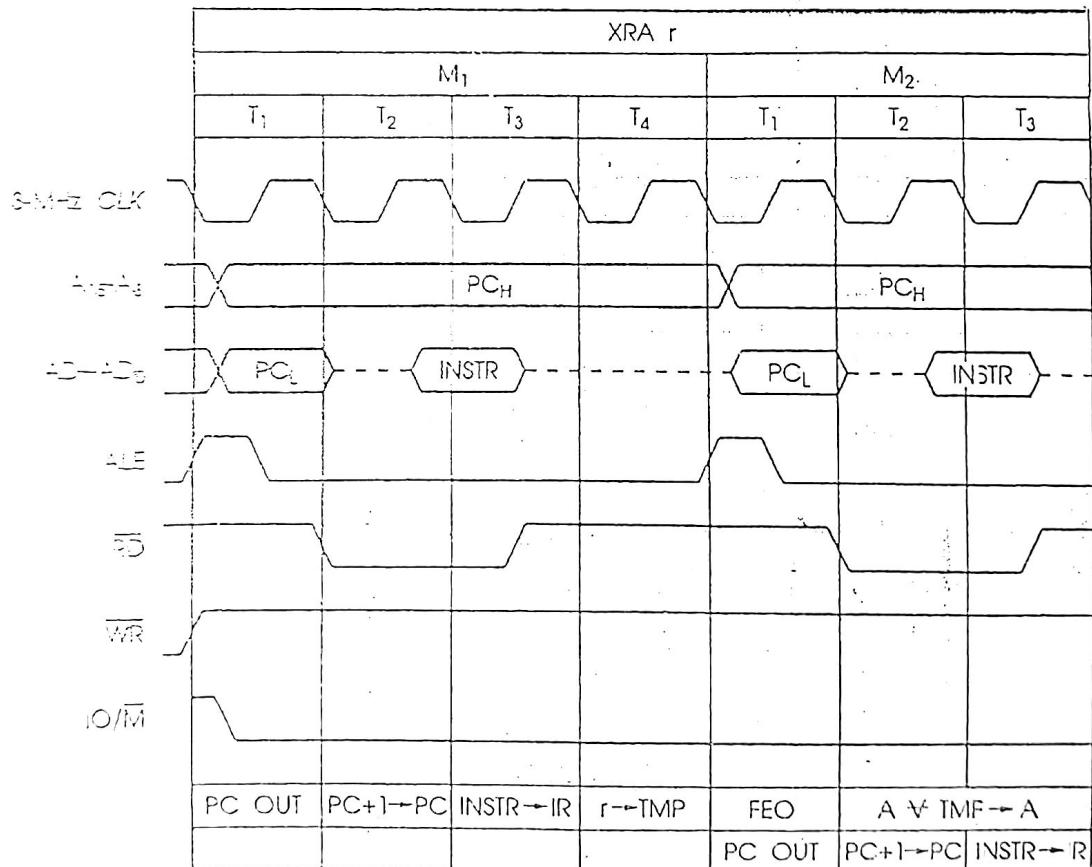


Fig. 2.37. Timing diagram for XRA r instruction.

XRA M (Exclusive OR Memory) $(A) \leftarrow (A) \vee ((H) (L))$

The content of the memory location whose address is contained in the H and L registers is exclusive OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	0	1	1	1	0
Cycles	: 2						
States	: 7						
Addressing	: reg. indirect						
Flags	: Z, S, P, CY, AC						

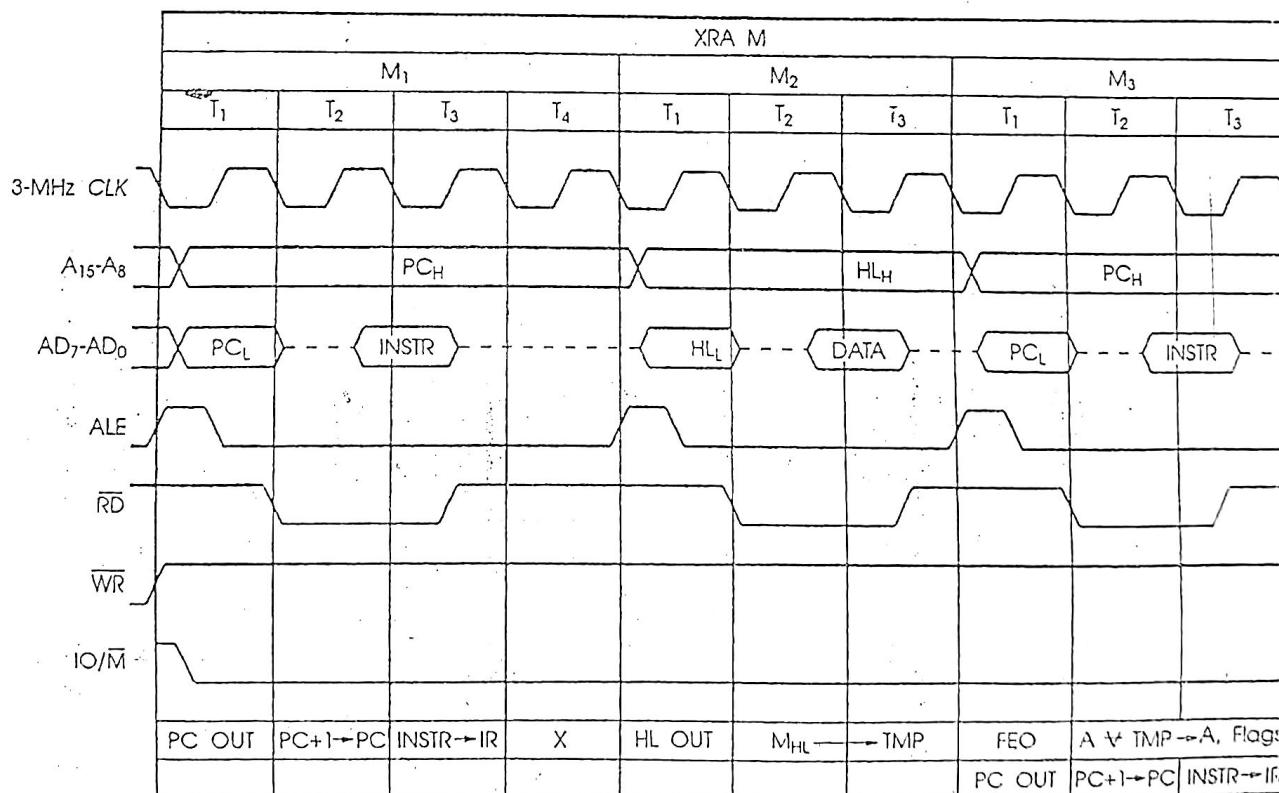


Fig. 2.38. Timing diagram for XRA M instruction.

XRI data (Exclusive OR immediate)

$$(A) \leftarrow (A) \vee (\text{byte } 2)$$

The content of the second byte of the instruction is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	1	1	0	1	1	1	0
data							

Cycles : 2
 States : 7
 Addressing : immediate
 Flags : Z, S, P, CY, AC

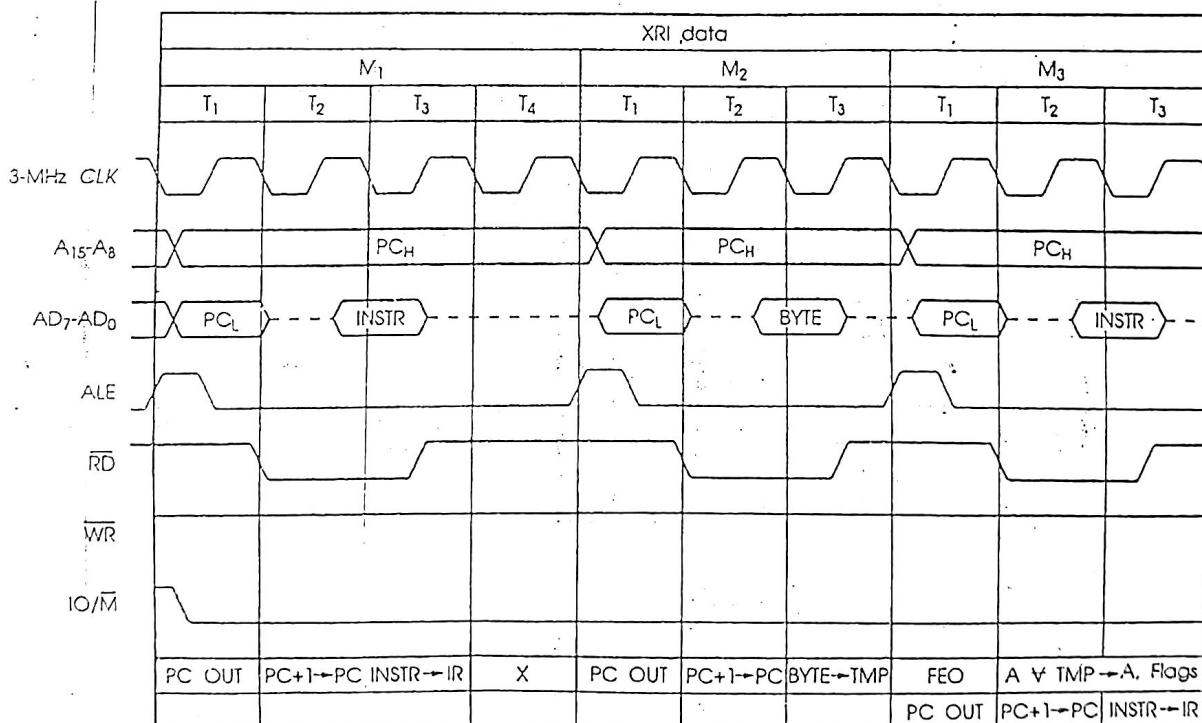


Fig. 2.39. Timing diagram for XRI data.

INSTRUCTION SET OF 8085

ORA r (OR Register)

$$(A) \leftarrow (A) \vee (r)$$

The content of register r is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	1	0	S	S	S
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Addressing : register
 Flags : Z, S, P, CY, AC

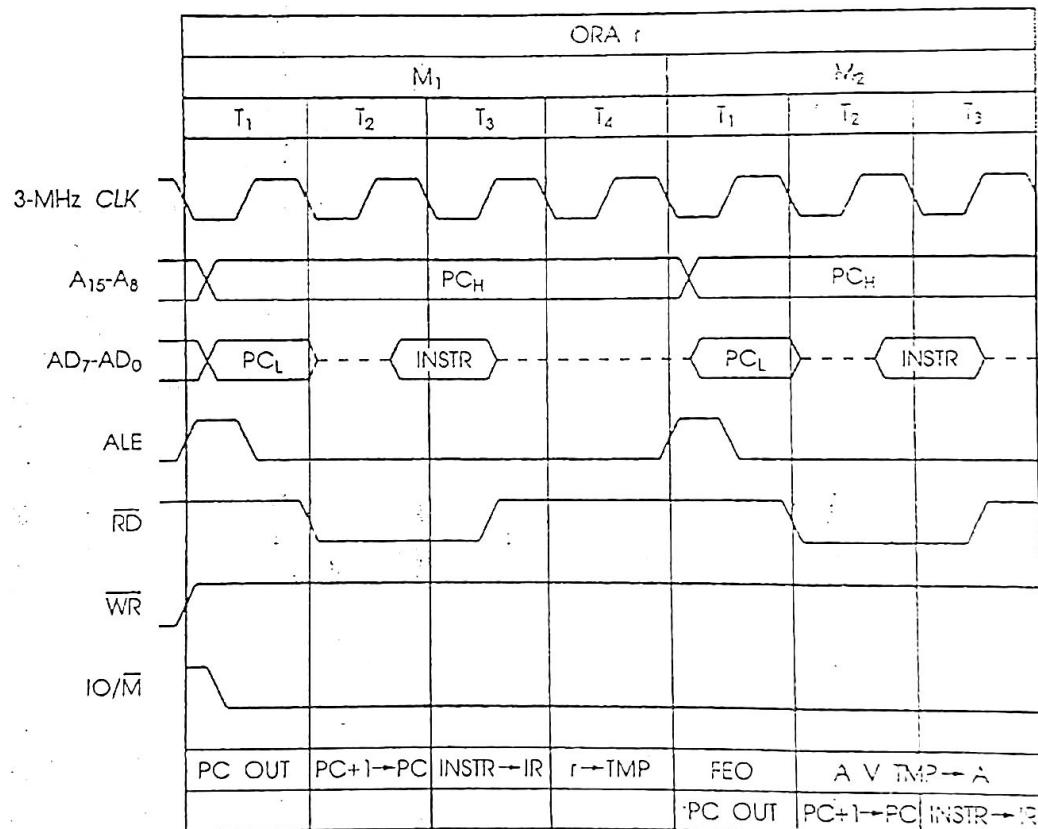


Fig. 2.40. Timing diagram for ORA r instruction.

ORA M (OR memory)

 $(A) \leftarrow (A) V ((H) (L))$

The content of the memory location whose address is contained in the H and L registers is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	.	1	1	0	1	1	0
---	---	---	---	---	---	---	---	---

Cycles : 2

States : 7

Addressing : reg. indirect

Flags : Z, S, P, CY, AC

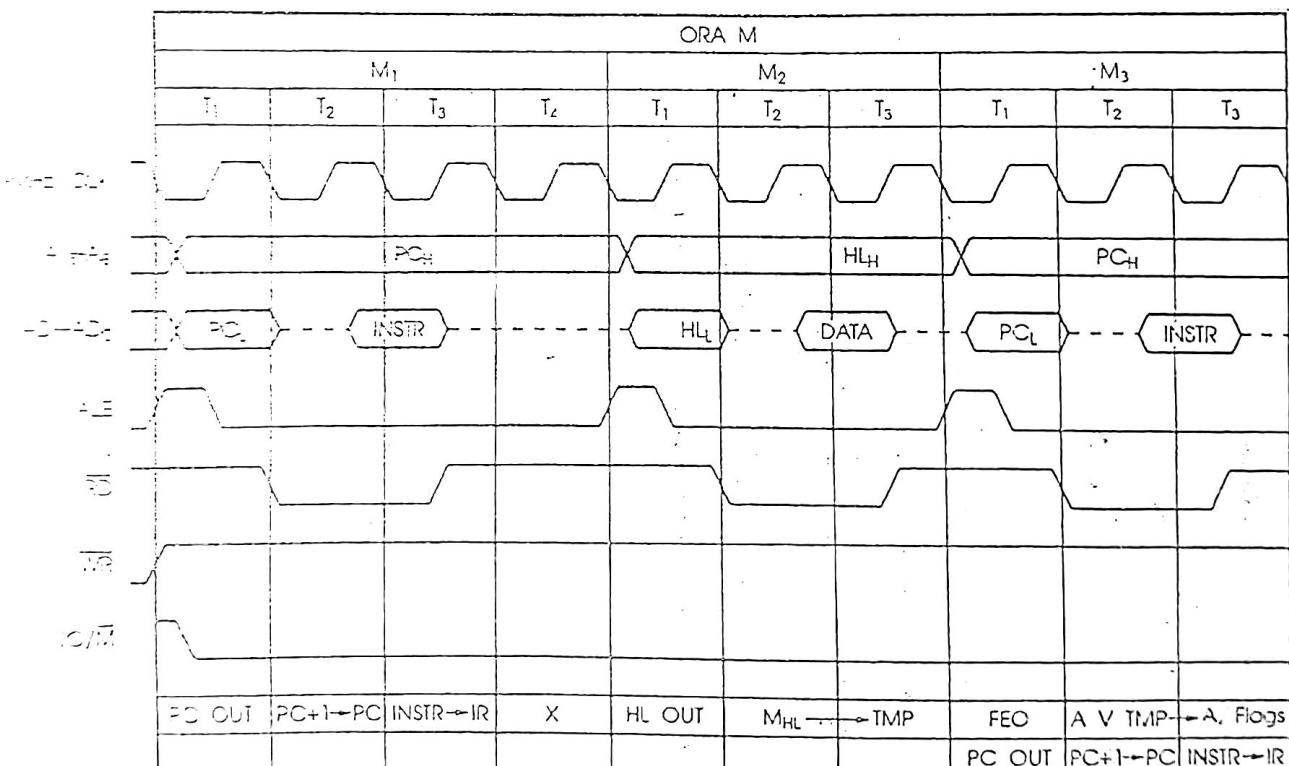


Fig. 2.41. Timing diagram for ORA M instruction.

INSTRUCTION SET OF 8085

ORI data (OR immediate)

$(A) \leftarrow (A) V$ (byte 2)

The content of the second byte of the instruction is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	1	1	1	0	1	1	0
data							

Cycles : 2
 States : 7
 Addressing : immediate
 Flags : Z, S, P, CY, AC

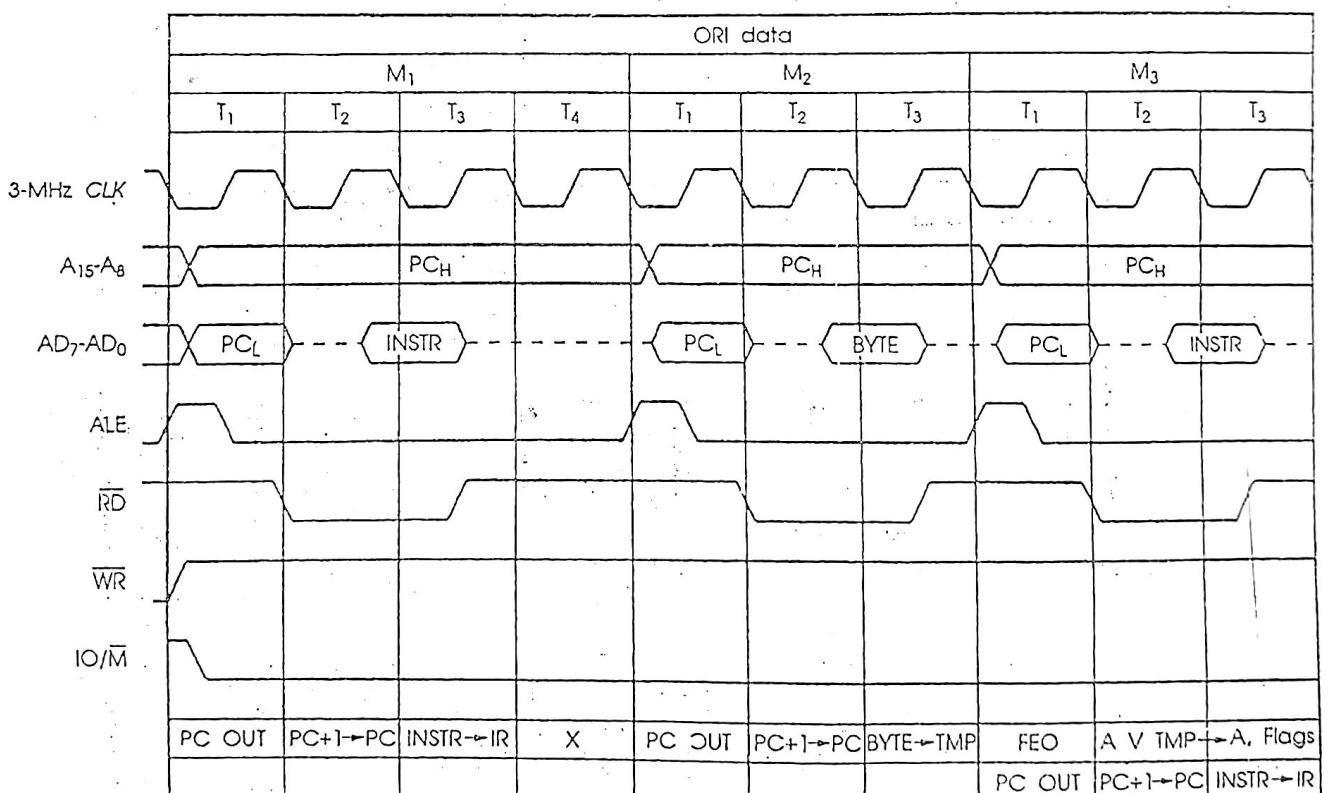


Fig. 2.42. Timing diagram for ORI data instruction.

CMP r (Compare Register)

(A) - (r)

The content of register r is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).

1	0	1	1	1	S	S	S
---	---	---	---	---	---	---	---

Cycles : 1

States : 4

Addressing : register

Flags : Z, S, P, CY, AC

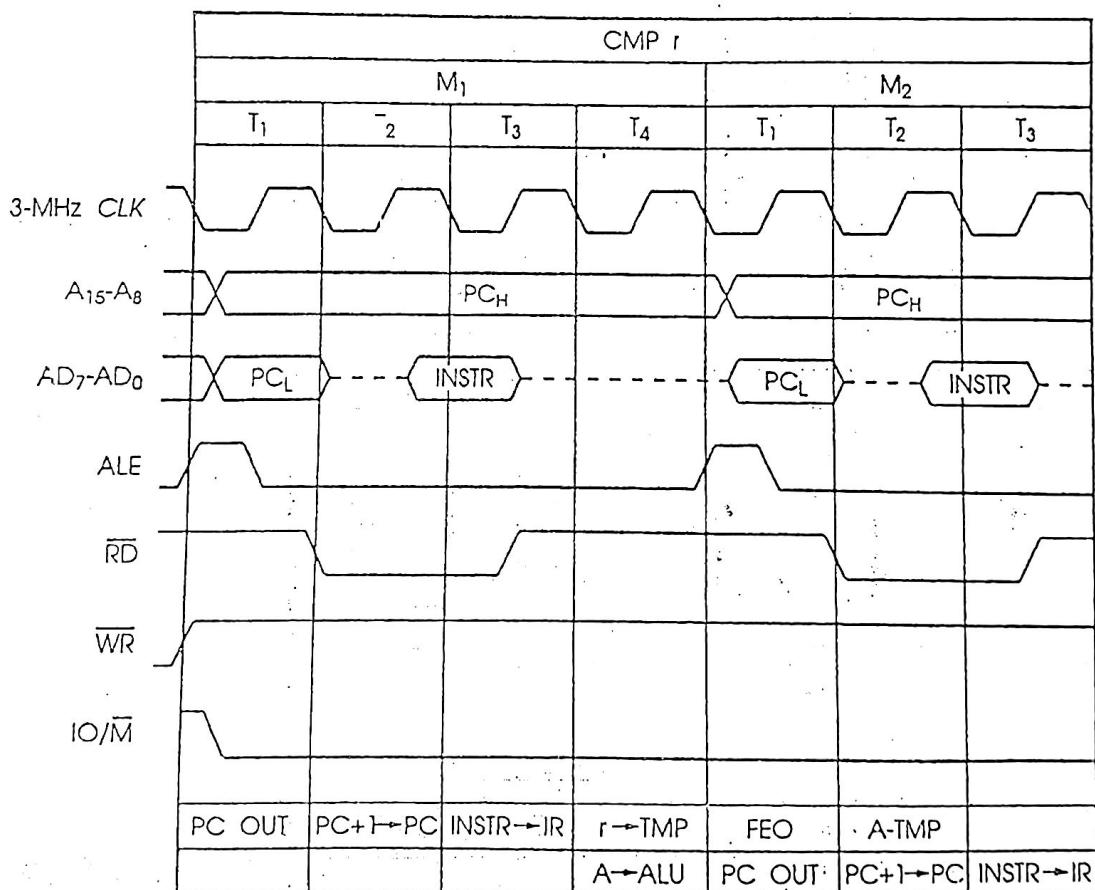


Fig. 2.43. Timing diagram for CMP r instruction.

INSTRUCTION SET OF 8085

CMP M (Compare memory)

(A - ((H) (L)))

The content of the memory location whose address is contained in the H and L registers is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = ((H) (L)). The CY flag is set to 1 if (A) < ((H) (L)).

1	0	1	1	1	1	1	0
---	---	---	---	---	---	---	---

Cycles : 2
 States : 7
 Addressing : reg. indirect
 Flags : Z, S, P, CY, AC

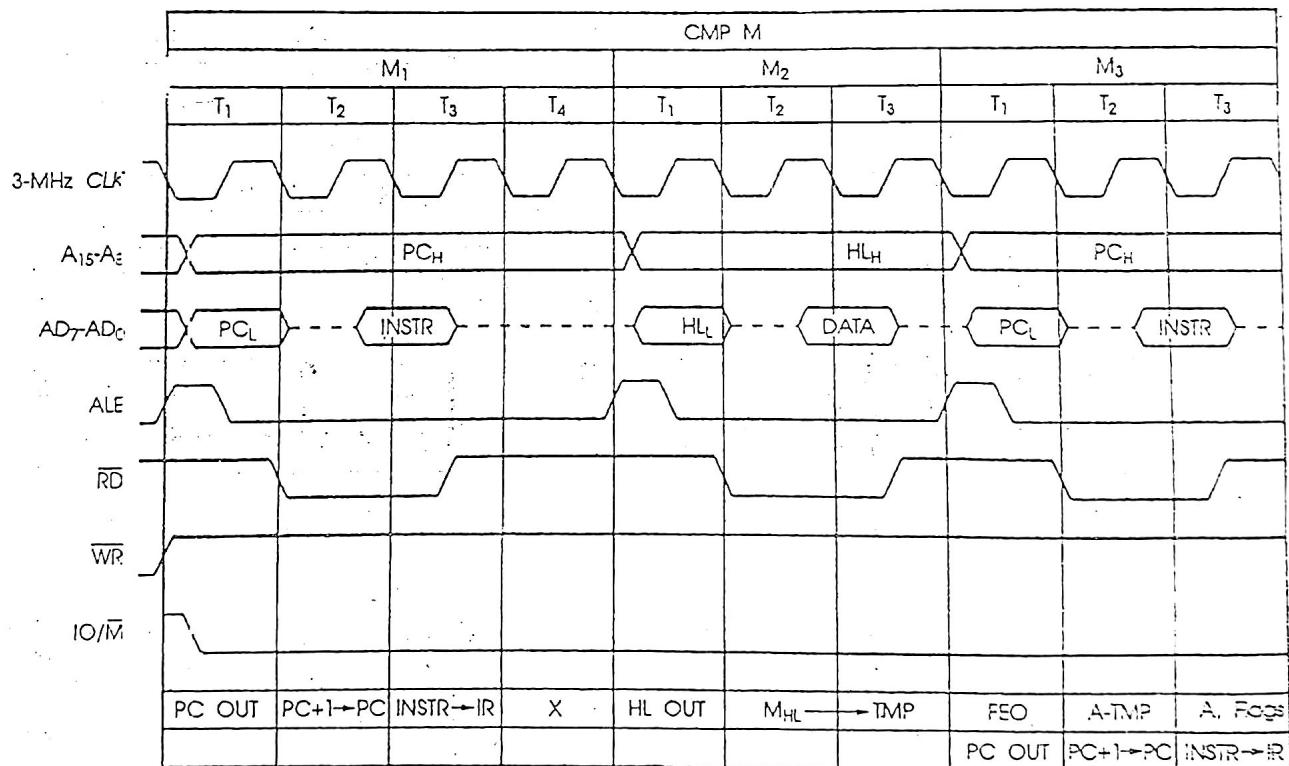


Fig. 2.44. Timing diagram for CMP M instruction.

CPI data (Compare immediate)

(A) - (byte 2)

The content of the second byte of the instruction is subtracted from the accumulator. The condition flags are set by the result of the subtraction. The Z flag is set to 1 if (A) = (byte 2). The CY flag is set to 1 if (A) < (byte 2).

1	1	1	1	1	1	1	0
---	---	---	---	---	---	---	---

Cycles : 2
 States : 7
 Addressing : immediate
 Flags : Z, S, P, CY, AC

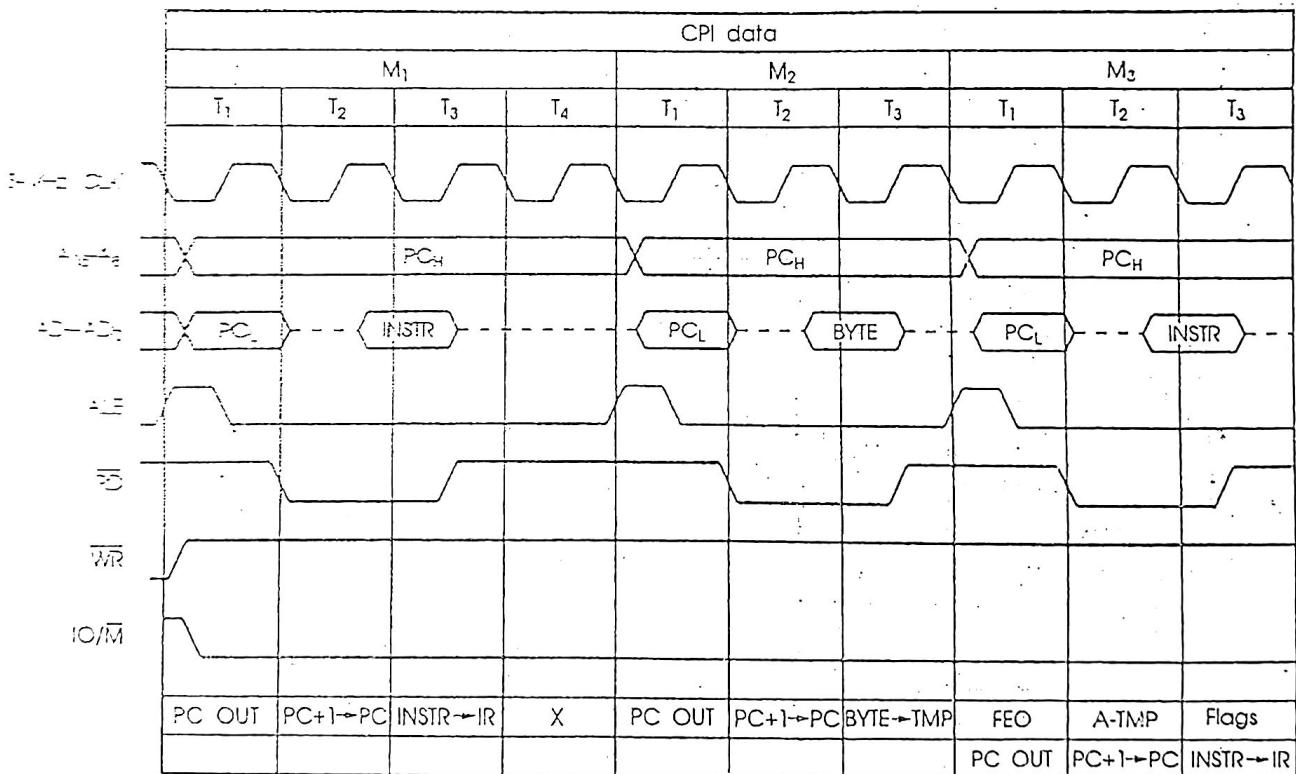


Fig. 2.45. Timing diagram for CPI data.

RLC (Rotate left)
 $(A_{n+1}) \leftarrow (A_n); (A_0) \leftarrow (A_7)$
 $(CY) \leftarrow (A_7)$

The content of the accumulator is rotated left one position. The low order bit and the CY flag are both set to the value shifted out of the high order bit position. Only the CY flag is affected.

0	0	0	0	0	1	1	1
Cycles	:	1					
States	:	4					
Flags	:	CY					

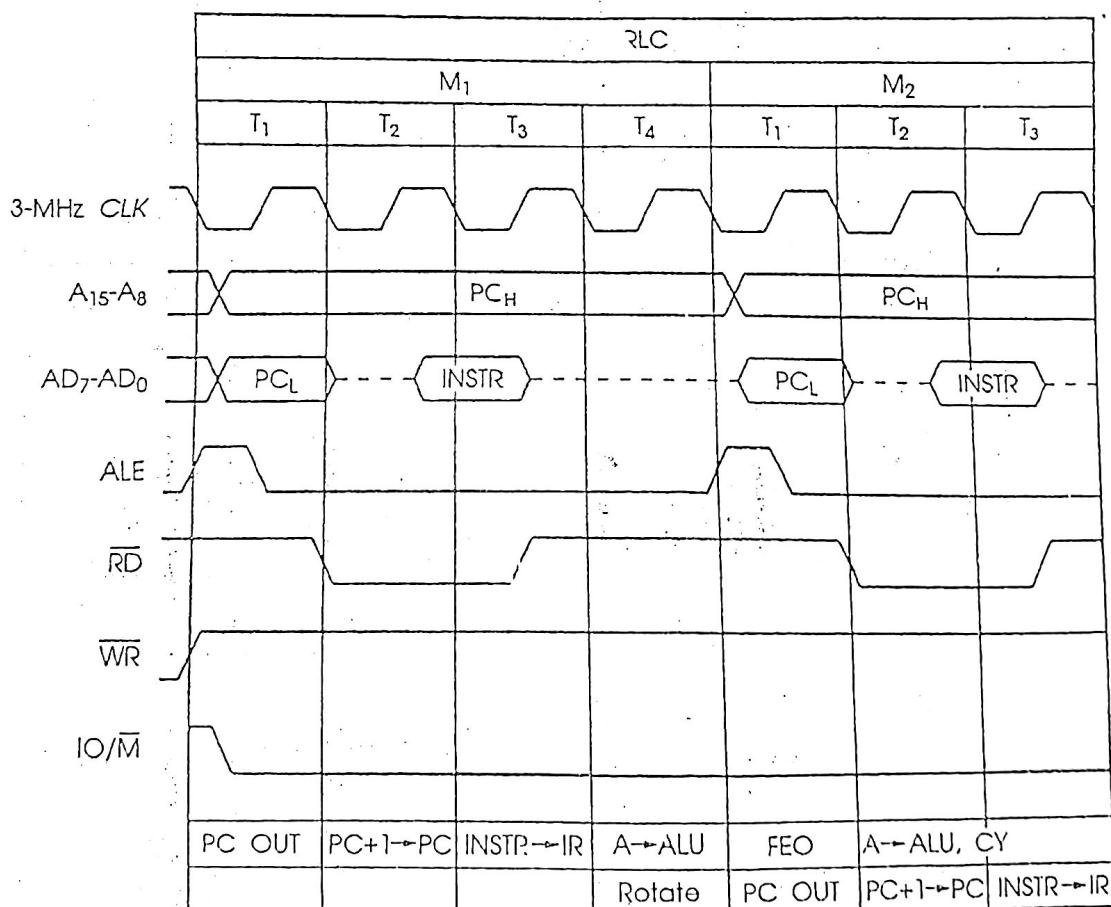


Fig. 2.46. Timing diagram for RLC instruction.

RRC (Rotate right)

$(A_n) \leftarrow (A_{n+1}) ; (A_7) \leftarrow (A_0)$
 $(CY) \leftarrow (A_0)$

The content of the accumulator is rotated right one position. The high order bit and the CY flag are both set to the value shifted out of the low order bit position. Only the CY flag is affected.

0	0	0	0	1	1	1	1
---	---	---	---	---	---	---	---

Cycles : 1
States : 4
Flags : CY

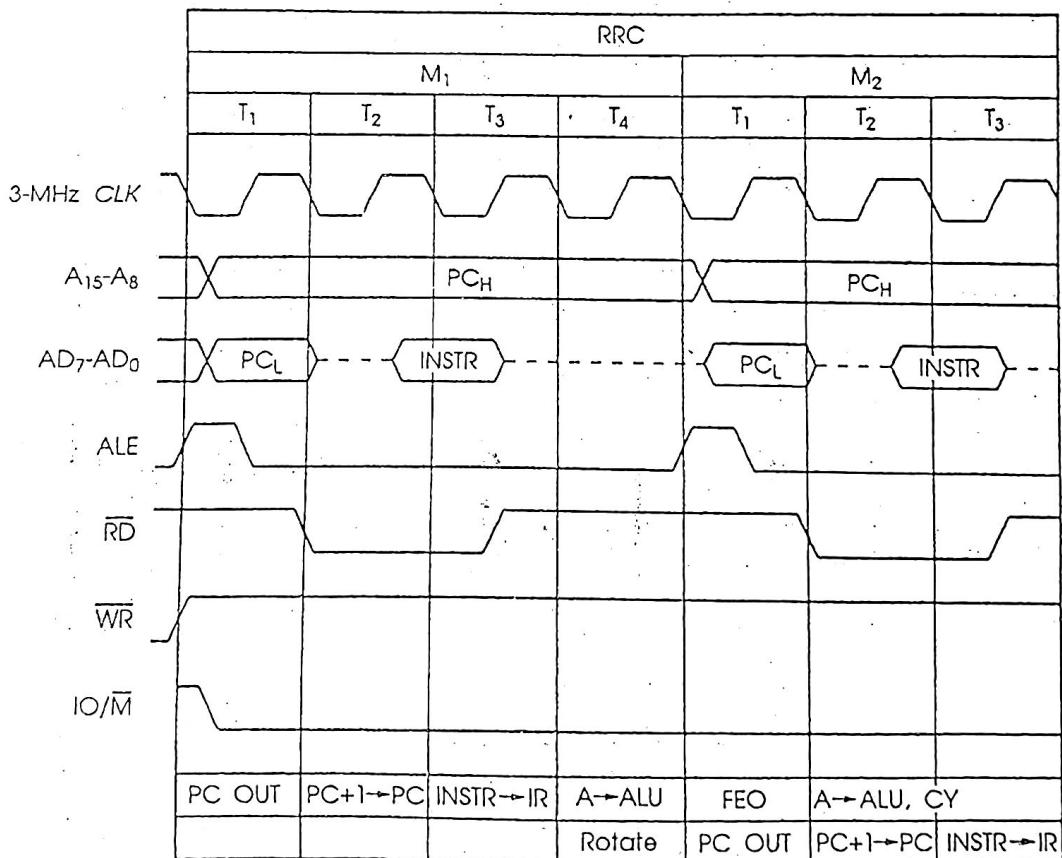


Fig. 2.47. Timing diagram for RRC instruction.

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RAL (Rotate left through carry)

$$\begin{aligned}(A_{n+1}) &\leftarrow (A_n); (CY) \leftarrow (A_7) \\ (A_0) &\leftarrow (CY)\end{aligned}$$

The content of the accumulator is rotated left one position through the CY flag. The low order bit is set equal to the CY flag and CY flag is set to the value shifted out of the high order bit. Only the CY flag is affected.

0	0	0	1	0	1	1	1
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Flags : CY

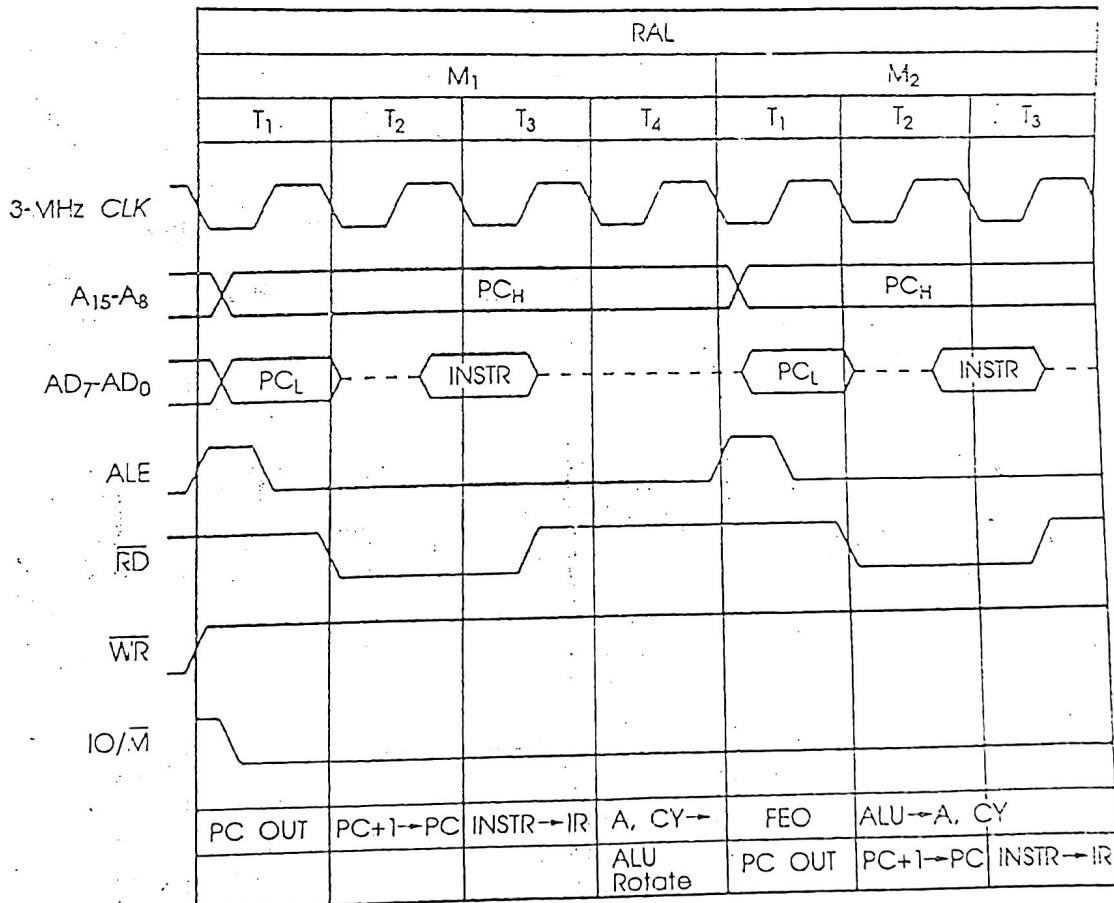


Fig. 2.48. Timing diagram for RAL instruction

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RAR (Rotate right through carry)

$$(A_n) \leftarrow (A_{n+1}); (CY) \leftarrow (A_0)$$

$$(A_7) \leftarrow (CY)$$

The content of the accumulator is rotated right one position through the CY flag. The high order bit is set to the CY flag and the CY flag is set to the value shifted out of the low order bit. Only the CY flag is affected.

0	0	0	1	1	1	1	1
---	---	---	---	---	---	---	---

Cycles : 1

States : 4

Flags : CY

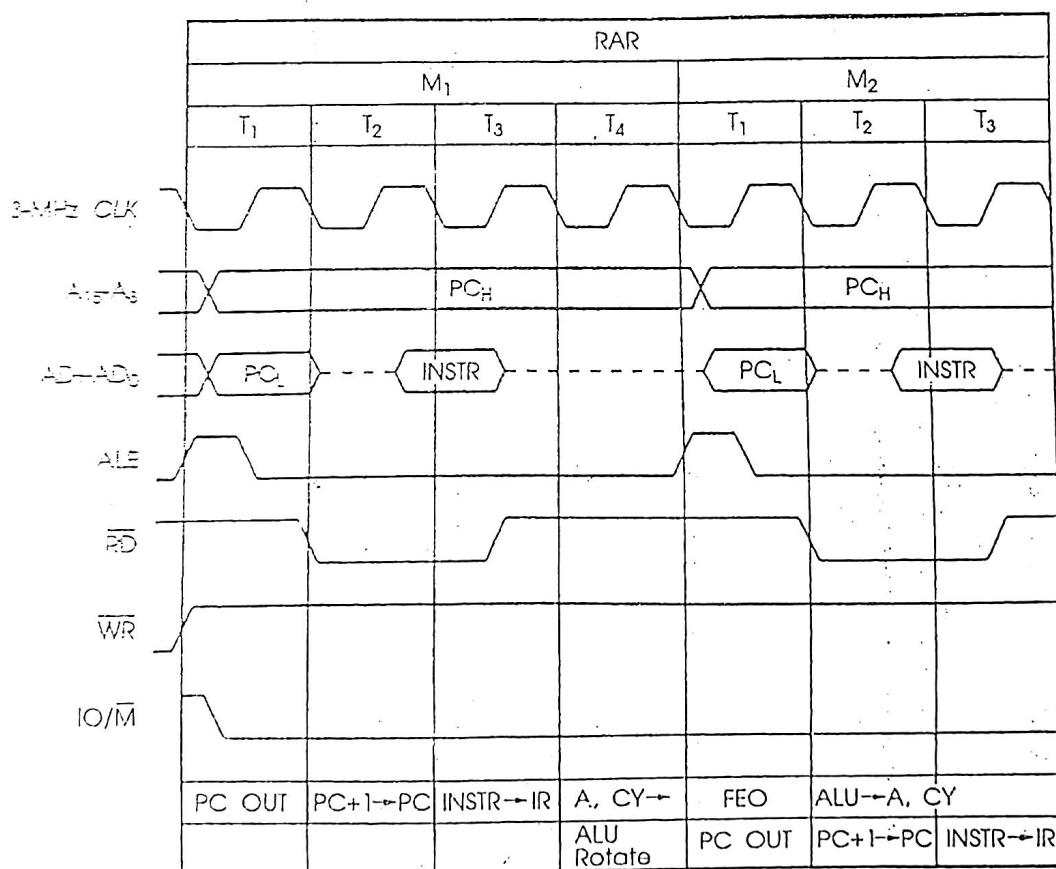


Fig. 2.49. Timing diagram for RAR instruction

INSTRUCTION SET OF 8085

CMA (Complement accumulator)

$(A) \leftarrow (\bar{A})$

The contents of the accumulator are complemented (zero bits become 1, one bits become 0). No flags are affected.

0	0	1	0	1	1	1	1
---	---	---	---	---	---	---	---

Cycles : 1

States : 4

Flags : CY

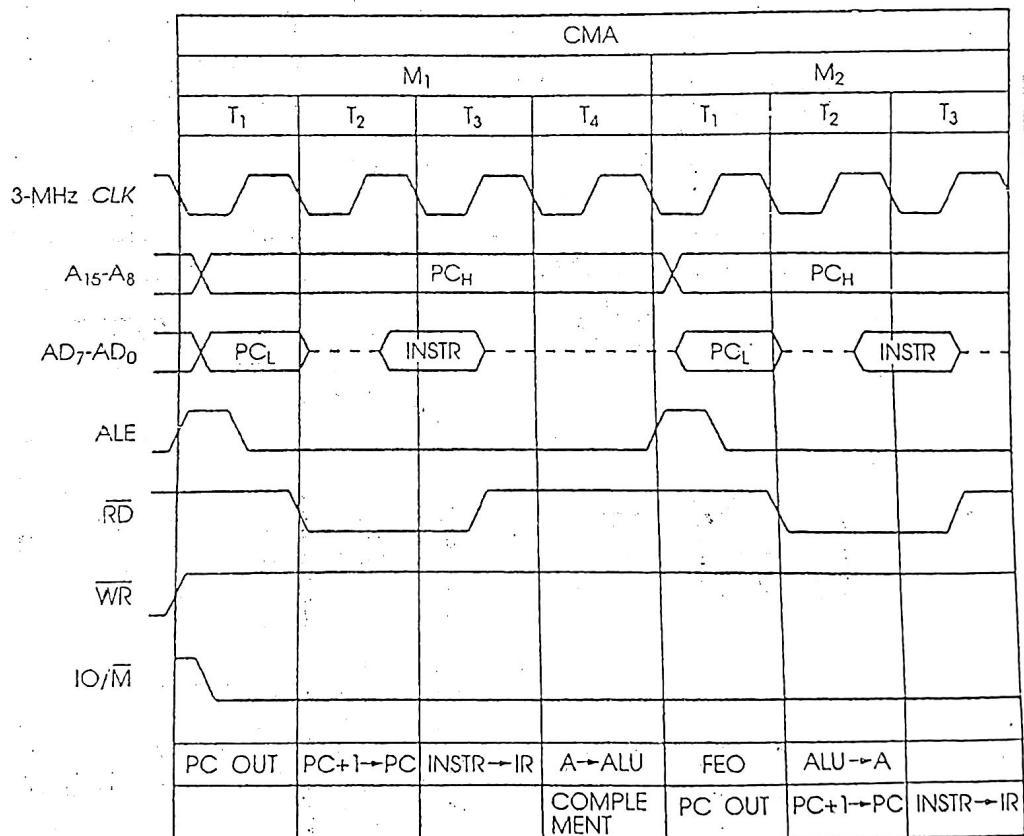


Fig. 2.50. Timing diagram for CMA instruction

CMC (Complement carry)
 $(CY) \leftarrow \overline{(CY)}$

The CY flag is complemented. No other flags are affected.

0	0	1	1	0	1	1	1
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Flags : CY

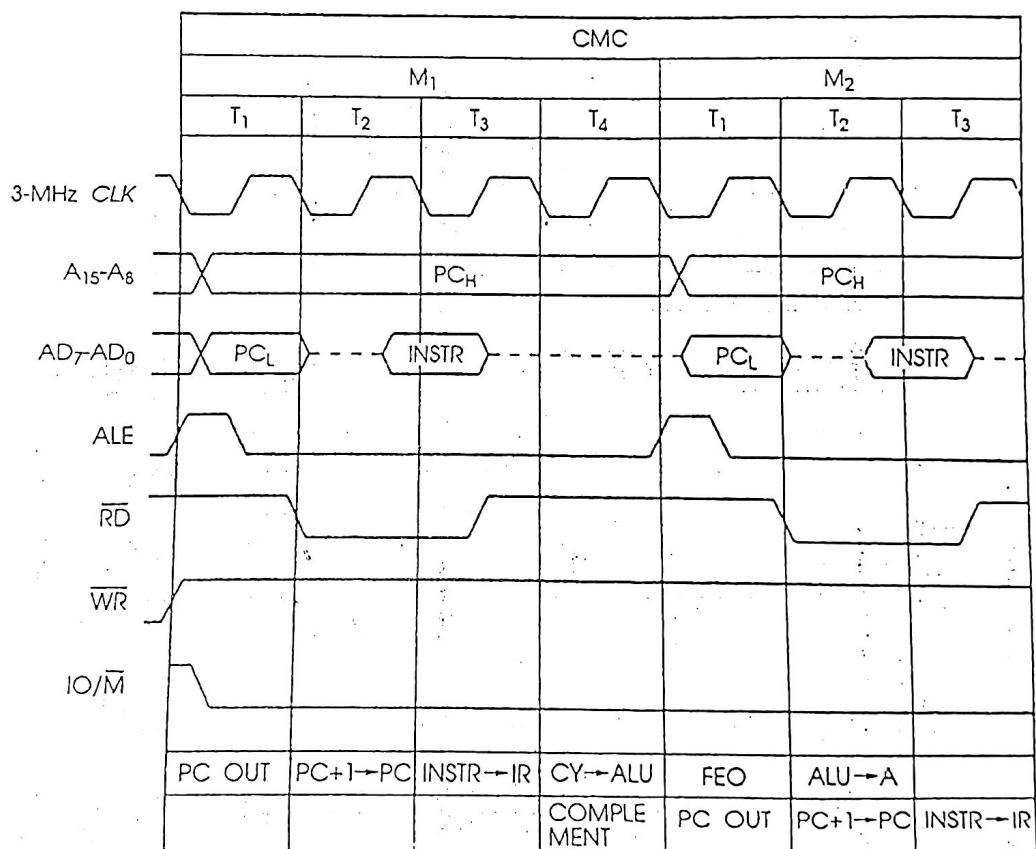


Fig. 2.51. Timing diagram for CMC Instruction

INSTRUCTION SET OF 8085

STC (Set carry)

$(CY) \leftarrow (1)$

The CY flag is set to 1. No other flags are affected.

0	0	1	1	0	1	1	1
---	---	---	---	---	---	---	---

Cycles : 1

States : 4

Flags : CY

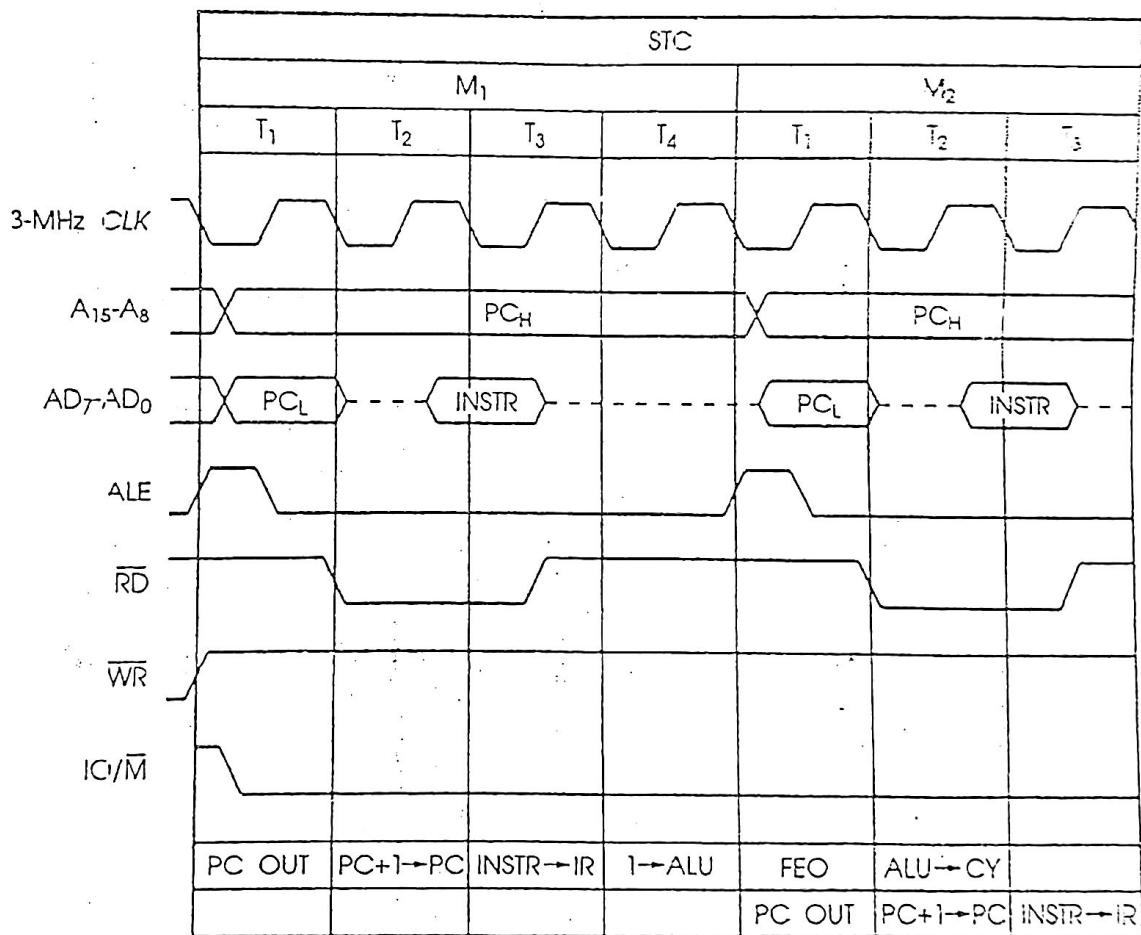


Fig. 2.52. Timing diagram for STC instruction

2.3.4 BRANCH GROUP

This group of instruction alter normal sequential program flow.

Condition flags are not affected by any instruction in this group.

The two types of branch instructions are unconditional and conditional. Unconditional transfers simply perform the specified operation on register PC (the program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed. The conditions that may be specified are as follows :

CONDITION	CCC
NZ — not zero ($Z = 0$)	000
Z — zero ($Z = 1$)	001
NC — not carry ($CY = 0$)	010
C — carry ($CY = 1$)	011
PO — parity odd ($P = 0$)	100
PE — parity even ($P = 1$)	101
P — plus ($S = 0$)	110
M — minus ($S = 1$)	111

JMP addr (Jump)

(PC) \leftarrow (byte 3) (byte 2)

Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

1	1	0	0	0	0	1	1
low-order addr							
high-order addr							

Cycles : 3
 States : 10
 Addressing : immediate
 Flags : none

Jcondition addr (Conditional jump)

If (CCC)

(PC) \leftarrow (byte 3) (byte 2)

If the specified condition is true, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise, control continues sequentially.

1	1	C	C	C	0	1	0
low-order addr							
high-order addr							

Cycles : 2/3
 States : 7/10
 Addressing : immediate
 Flags : none

INSTRUCTION SET OF 8085

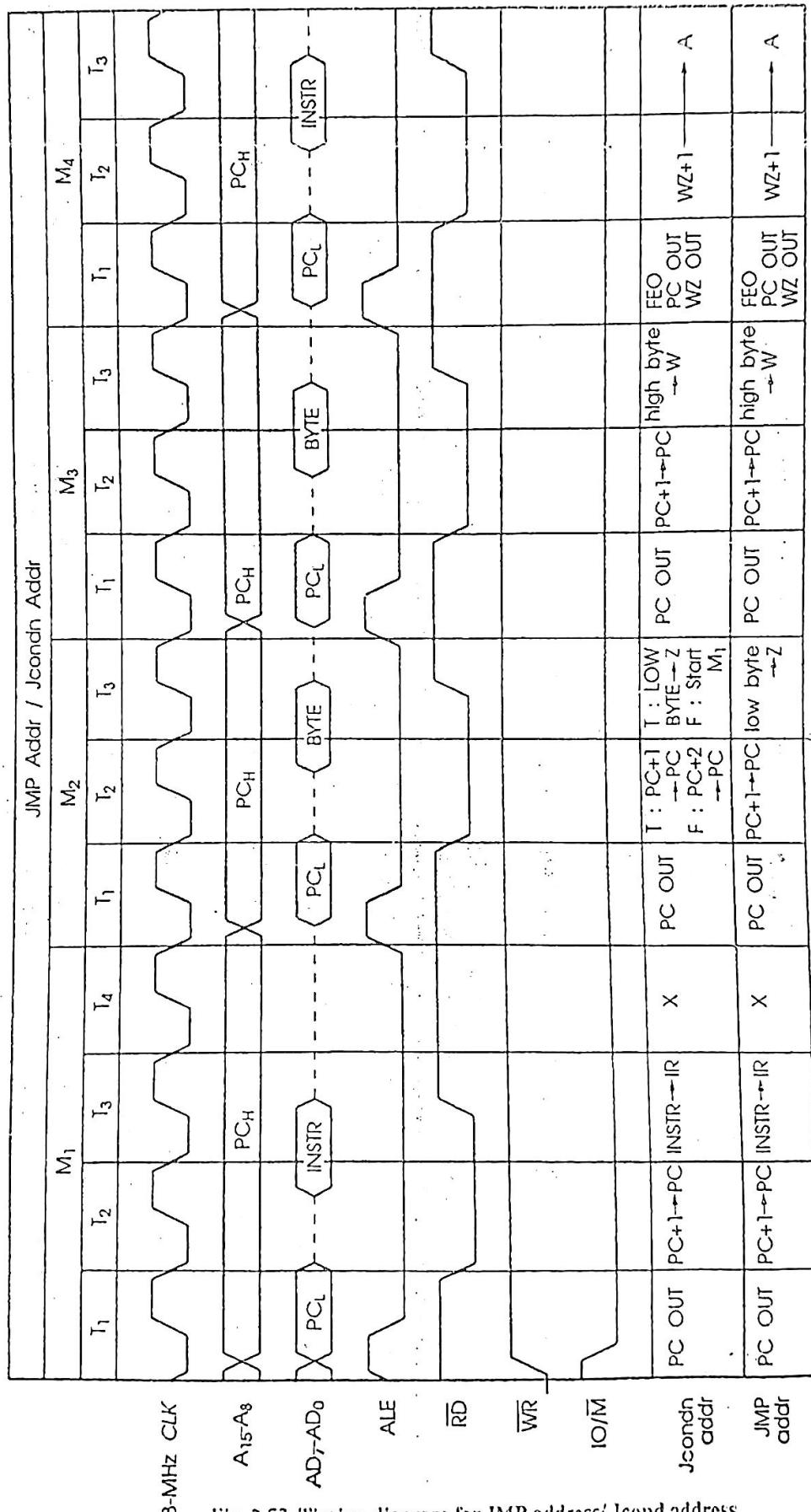


Fig. 2.53. Timing diagram for JMP address/Jcond address.

CALL addr (Call) $((SP) - 1) \leftarrow (PCH)$ $((SP) - 2) \leftarrow (PCL)$ $(SP) \leftarrow (SP) - 2$ $(PC) \leftarrow (\text{byte } 3) (\text{byte } 2)$

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

1	1	0	0	1	1	0	1
low-order addr							
high-order addr							

Cycles : 5

States : 18

Addressing : immediate/reg. indirect

Flags : none

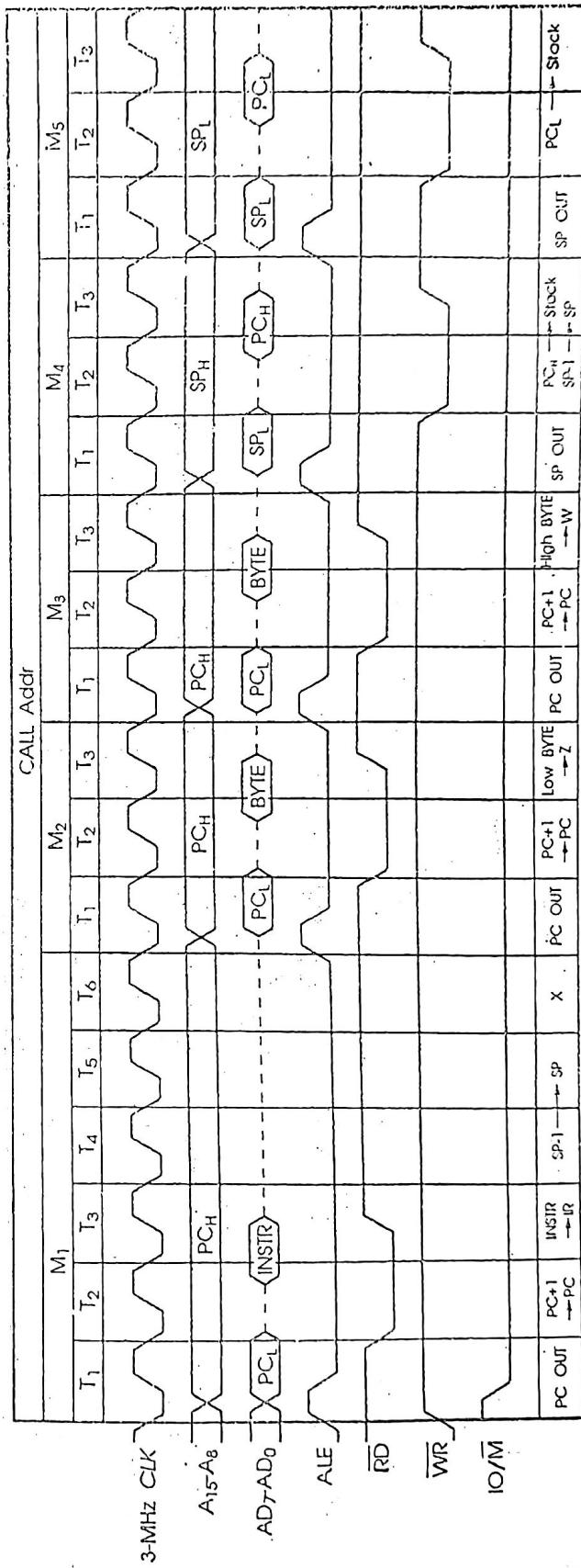


Fig. 2.54. Timing diagram for call instruction

INSTRUCTION SET OF 8085

C Condition addr (Condition call)

If (CCC),

((SP) - 1) \leftarrow (PCH)

((SP) - 2) \leftarrow (PCL)

(SP) \leftarrow (SP) - 2

(PC) \leftarrow (byte 3) (byte 2)

If the specified condition is true, the actions specified in the CALL instruction (see above) are performed; otherwise, control continues sequentially.

1	1	C	C	C	1	0	0
low-order addr							
high-order addr							

Cycles : 2/5

States : 9/18

Addressing : immediate/reg. indirect

Flags : none

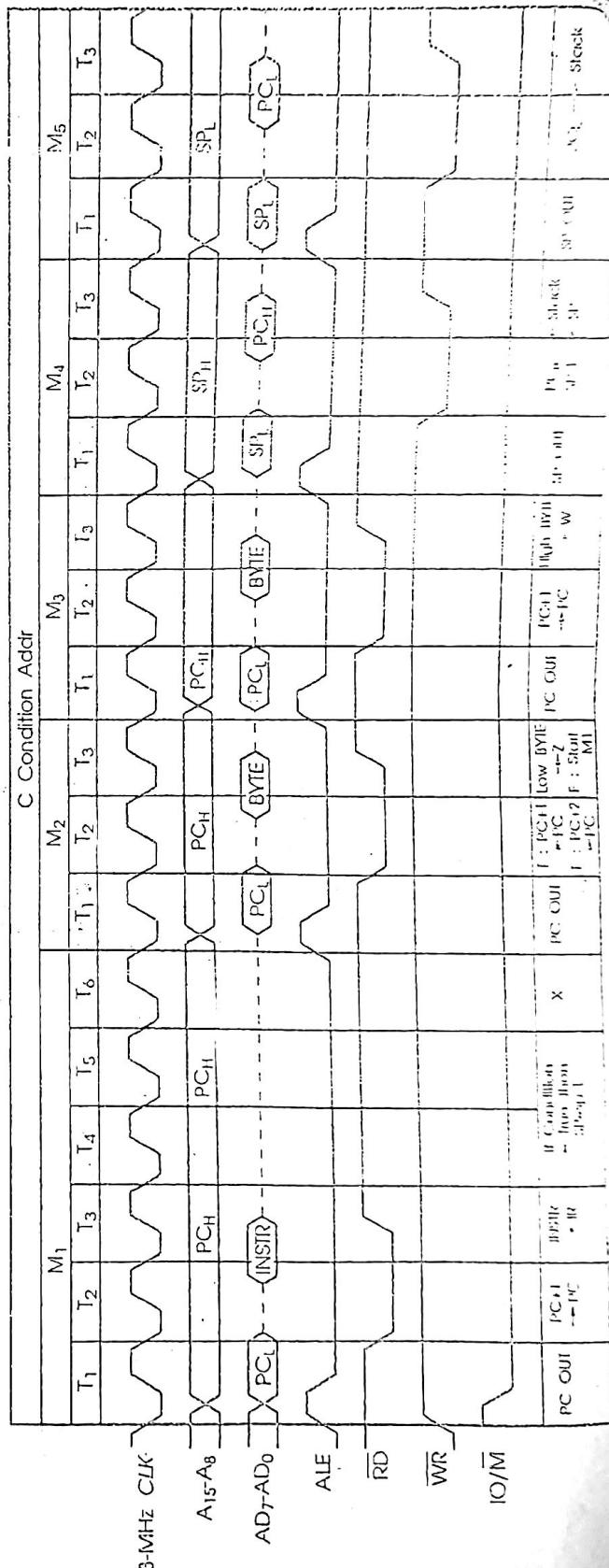


Fig. 2.55. Timing diagram for Condition Addr instruction

RET (Return)

```
(PCL) ← ((SP));
(PCH) ← ((SP) + 1);
(SP) ← (SP) + 2;
```

The content of the memory location whose address is specified in register SP is moved to the low-order eight bits of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order eight bits of register PC. The content of register SP is incremented by 2.

1	1	0	0	1	0	0	1
---	---	---	---	---	---	---	---

Cycles : 3
 States : 10
 Addressing : reg. indirect
 Flags : none

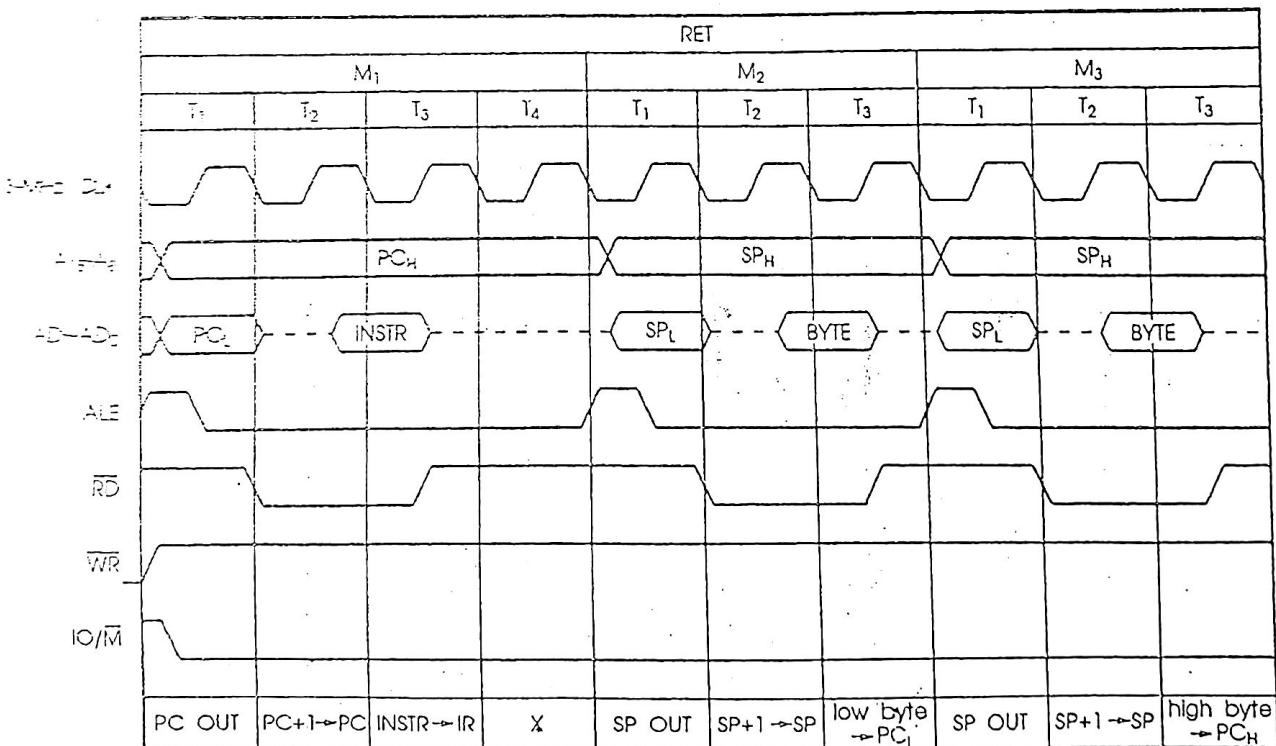


Fig. 2.56. Timing diagram for RET instruction

Recondition (Conditional return)

If (CCC),

 $(PCL) \leftarrow ((SP))$ $(PCH) \leftarrow ((SP) + 1)$ $(SP) \leftarrow (SP) + 2$

If the specified condition is true, the actions specified in the RET instruction (see above) are performed ; otherwise, control continues sequentially.

1	1	C	C	C	0	0	0
---	---	---	---	---	---	---	---

Cycles : 1/3

States : 6/12

Addressing : reg. indirect

Flags : none

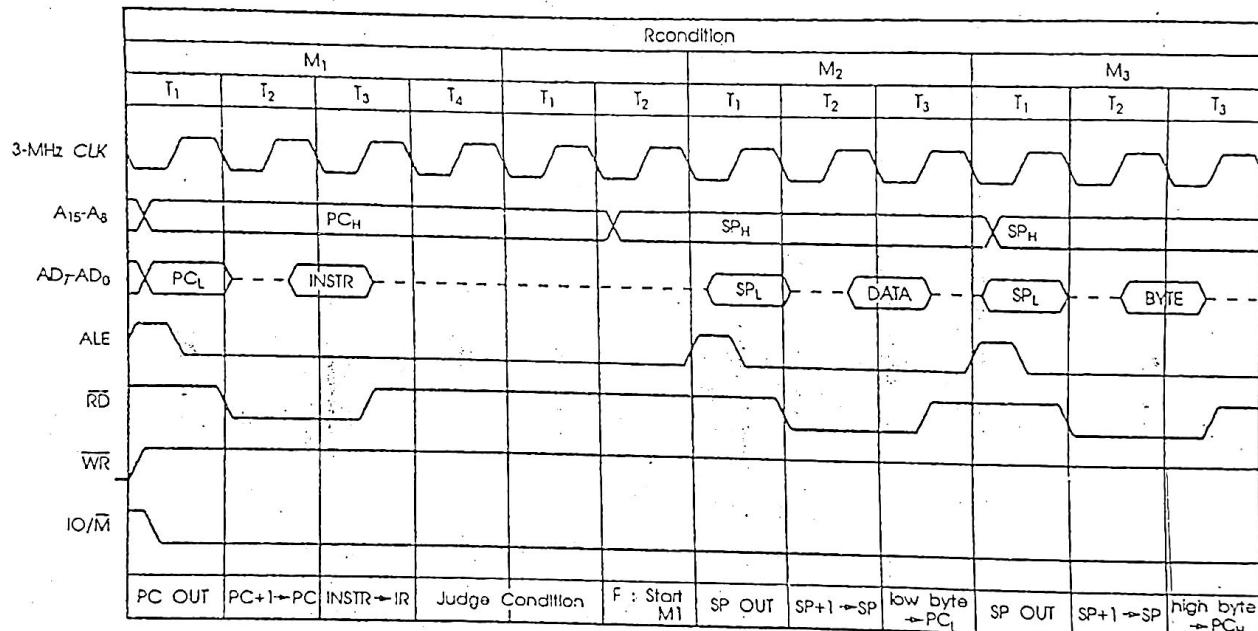
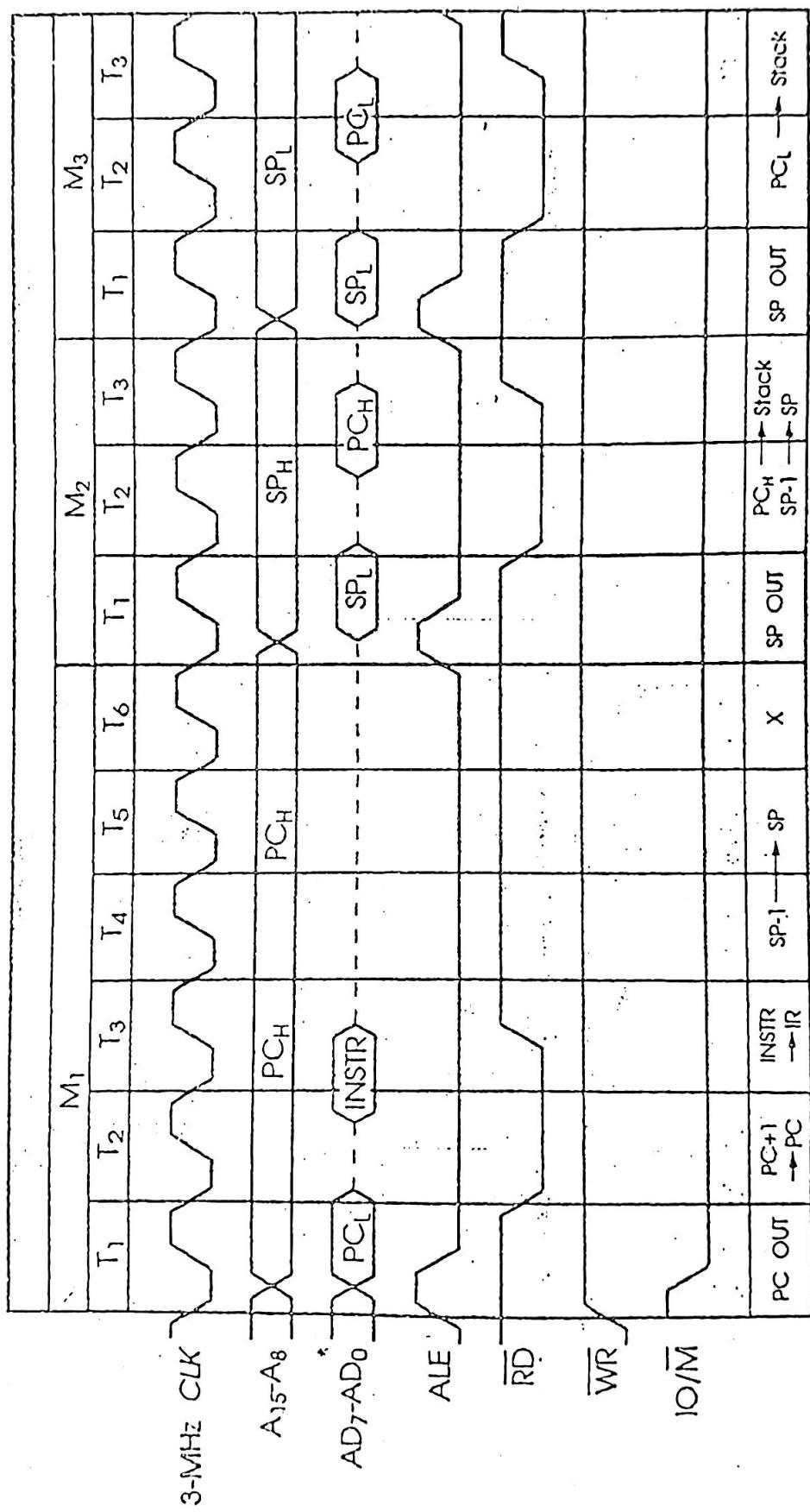


Fig. 2.57. Timing diagram for Recondition instruction

RST n (Restart)

 $((SP) - 1) \leftarrow (PCH)$ $((SP) - 2) \leftarrow (PCL)$ $(SP) \leftarrow (SP) - 2$ $(PC) \leftarrow 8 * (NNN)$

The high-order eight bits of the next instruction address are moved to the memory



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location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two. Control is transferred to the instruction whose address is eight times the content of NNN.

1	1	N	N	N	1	1	1
Cycles : 3							
States : 12							
Addressing : reg. indirect							
Flags : none							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	1
0	0	N	N	N	0	0	1

Program Counter After Restart

PCHL (Jump H and L indirect – move H and L to PC)

(PCH) \leftarrow (H)

(PCL) \leftarrow (L)

The content of register H is moved to the high-order eight bits of register PC. The content of register L is moved to the low-order eight bits of register PC.

1	1	1	0	1	0	0	1
Cycles : 1							
States : 6							
Addressing : register.							
Flags : none							

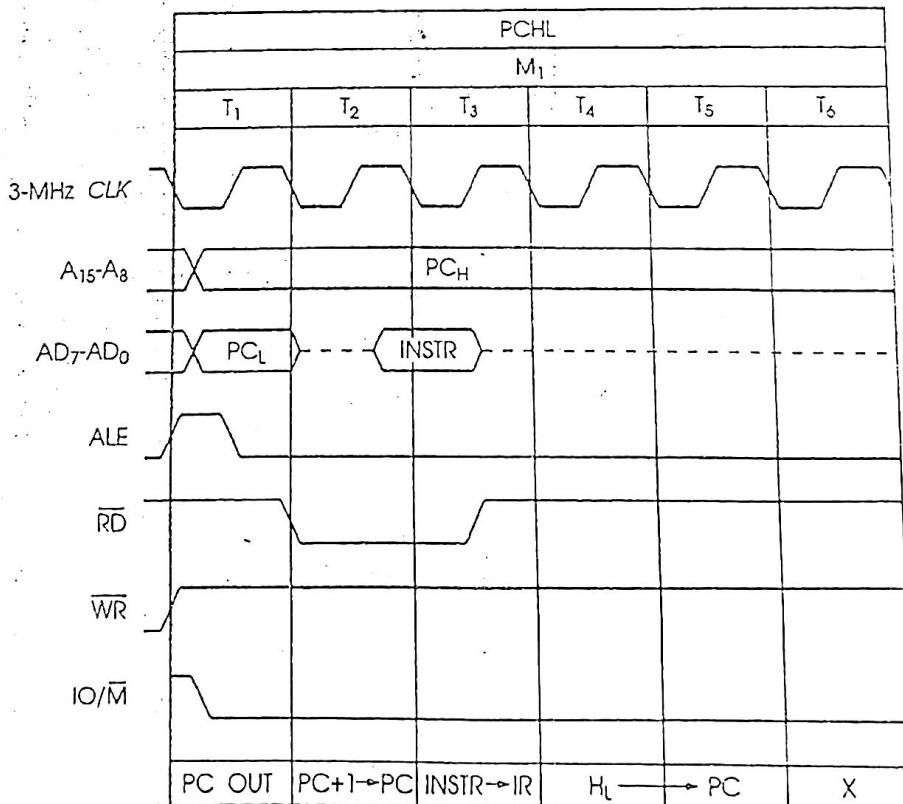


Fig. 2.59. Timing diagram for PCHL instruction

2.6.5 STACK, I/O AND MACHINE CONTROL GROUP

This group of instructions performs I/O, manipulates the Stack and alters internal control flags. Unless otherwise specified, condition flags are not affected by any instructions in this group.

PUSHI rp (Push)

$((SP) - 1) \leftarrow (r_h)$

$((SP) - 2) \leftarrow (r_l)$

$(SP) \leftarrow (SP) - 2$

The content of the high-order register of register pair rp is moved to the memory location whose address is one less than the content of register SP. The content of low-order register of register pair rp is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Note : Register pair rp = SP may not be specified.

1	1	R	P	0	1	0	1
---	---	---	---	---	---	---	---

Cycles	: 3
States	: 12
Addressing	: reg. indirect
Flags	: none

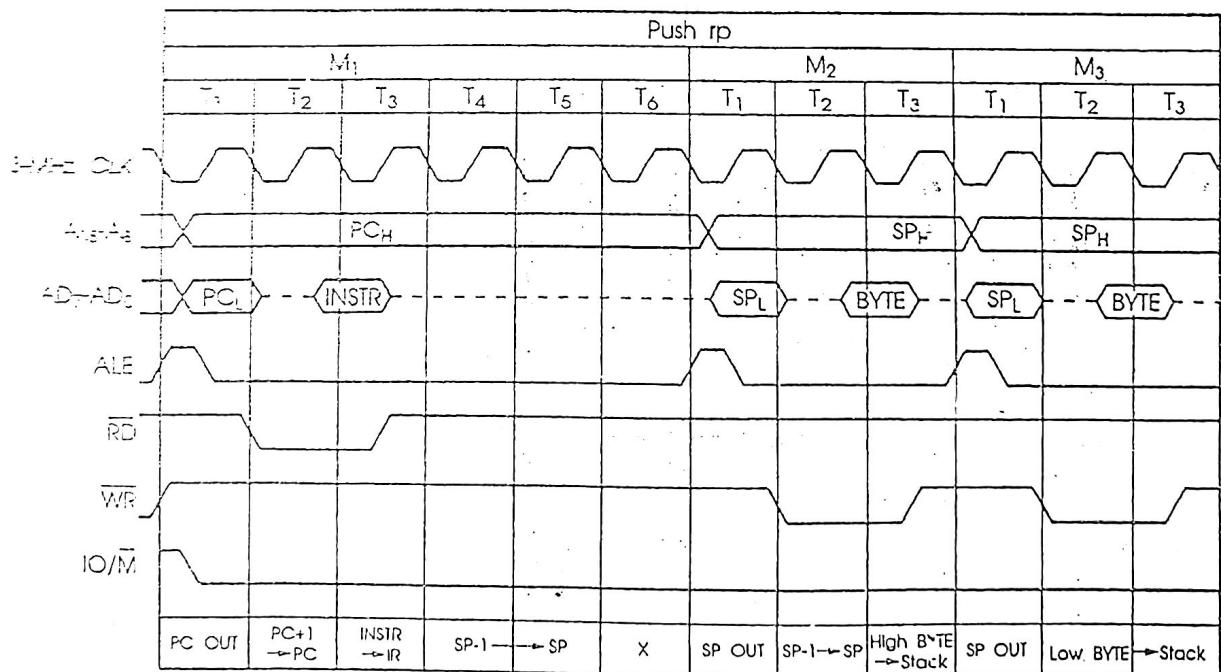


Fig. 2.60. Timing diagram for Push rp instruction

PUSH PSW (Push processor status word)

$((SP) - 1) \leftarrow (A)$
 $((SP) - 2)_0 \leftarrow (CY), ((SP) - 2)_1 \leftarrow X$
 $((SP) - 2)_2 \leftarrow (P), ((SP) - 2)_3 \leftarrow X$
 $((SP) - 2)_4 \leftarrow (AC), ((SP) - 2)_5 \leftarrow X$
 $((SP) - 2)_6 \leftarrow (Z), ((SP) - 2)_7 \leftarrow (S)$
 $(SP) \leftarrow (SP) - 2$

X : Undefined.

The content of register A is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a processor status word and the word is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.

1	1	1	1	0	1	0	1
---	---	---	---	---	---	---	---

Cycles : 3
 States : 12
 Addressing : reg. indirect
 Flags : none

FLAG WORD

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
S	Z	X	AC	X	P	X	CY

X : Undefined

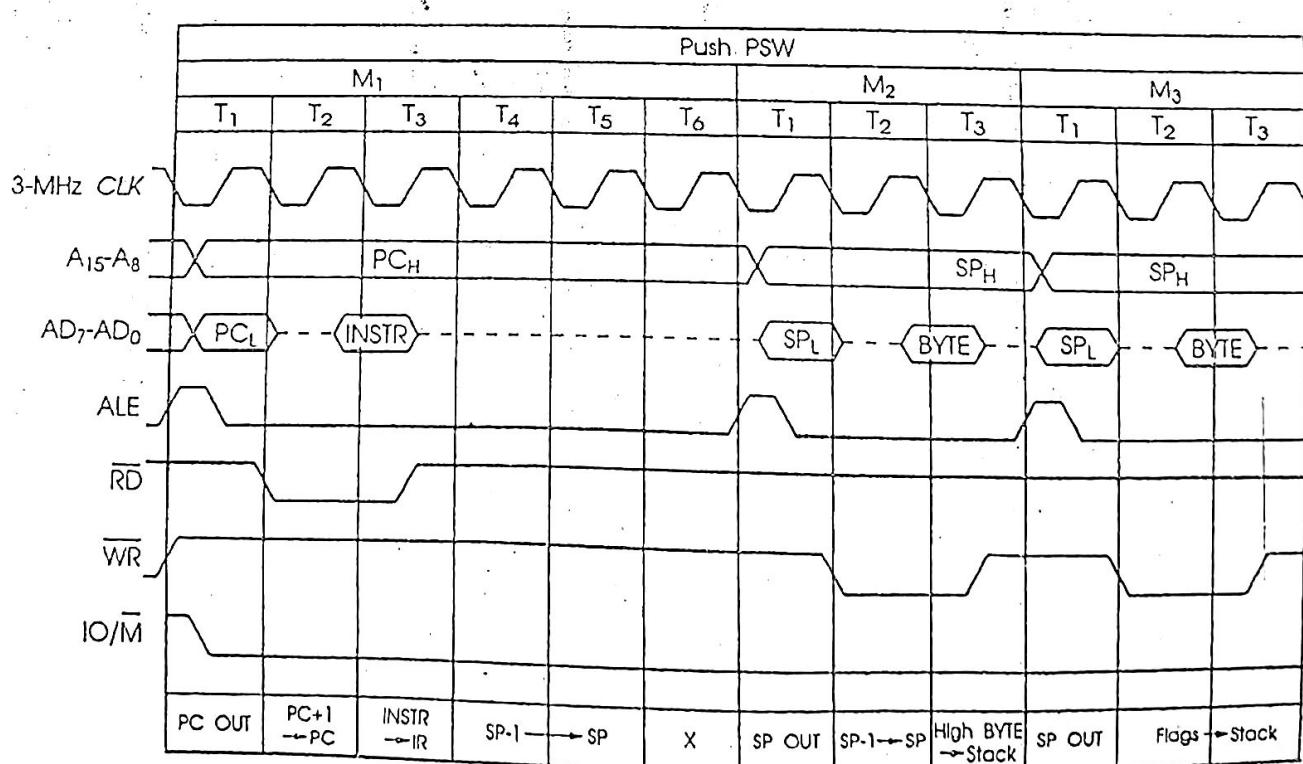


Fig. 2.61. Timing diagram for Push PSW instruction

POP rp (POP)

$$\begin{aligned} (rl) &\leftarrow ((SP))_0 \\ (rh) &\leftarrow ((SP))_1 \\ (SP) &\leftarrow (SP) + 2 \end{aligned}$$

The content of the memory location, whose address is specified by the content of register SP, is moved to the low-order register of register pair rp. The content of the memory location, whose address is one more than the content of register SP, is moved to the high-order register of register rp. The content of register SP is incremented by 2. Note : Register pair rp = SP may not be specified.

1	1	R	P	0	0	0	1
---	---	---	---	---	---	---	---

Cycles : 3
 States : 10
 Addressing : reg. indirect
 Flags : none

Fog timing diagram Refer to figure number 2.56.

Actions during each clock state is given below :

	Machine cycle 1	Machine cycle 2	Machine cycle 3
T ₁	PC out	SP out	SP out
T ₂	PC + 1 → PC	SP + 1 → SP	SP + 1 → SP
T ₃	INSTR → IR	low byte → RP _L	high byte → RP _H
T ₄	×		

POP PSW (Pop processor status word)

$$\begin{aligned} (CY) &\leftarrow ((SP))_0 \\ (P) &\leftarrow ((SP))_2 \\ (AC) &\leftarrow ((SP))_4 \\ (Z) &\leftarrow ((SP))_6 \\ (S) &\leftarrow ((SP))_7 \\ (A) &\leftarrow ((SP) + 1) \\ (SP) &\leftarrow (SP) + 2 \end{aligned}$$

The content of the memory location whose address is specified by the content of register SP is used to restore the condition flags. The content of the memory location whose address is one more than the content of register SP is moved to register A. The content of register SP is incremented by 2.

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1	1	1	1	0	0	0	1
---	---	---	---	---	---	---	---

Cycles : 3
 States : 10
 Addressing : reg. indirect
 Flags : Z, S, P, CY, AC

For timing diagram Refer to figure no 2.56.

Actions during each clock state is given below :

	Machine cycle 1	Machine cycle 2	Machine cycle 3
T ₁	PC out	SP out	SP out
T ₂	PC + 1 → PC	SP + 1 → SP	SP + 1 → SP
T ₃	INSTR → IR	low byte → Flags	high byte → A
T ₄	×		

XTHL (Exchange stack top with H and L)

$$(L) \leftrightarrow ((SP))$$

$$(H) \leftrightarrow ((SP) + 1)$$

The content of the L register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H register is exchanged with the content of the memory location whose address is one more than the content of register SP.

1	1	1	0	0	0	1	1
---	---	---	---	---	---	---	---

Cycles : 5
 States : 16
 Addressing : reg. indirect
 Flags : none

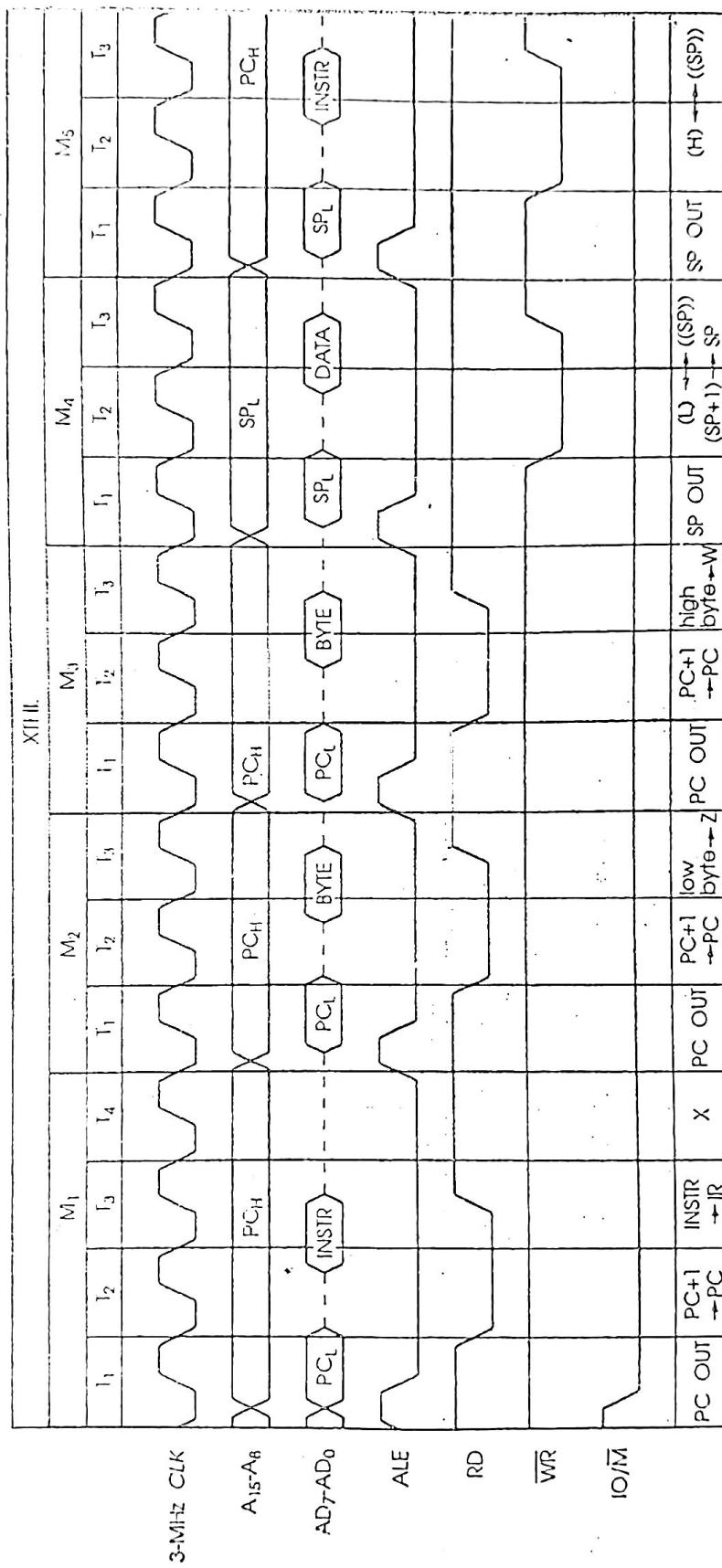


Fig. 2.62. Timing diagram for XTHL instructions

INSTRUCTION SET OF 8085

SPHL (Move HL to SP)

$(SP) \leftarrow (H) (L)$

The contents of registers H and L (16 bits) are moved to register SP.

1	1	1	1	1	0	0	1
---	---	---	---	---	---	---	---

Cycles : 1
 States : 6
 Addressing : register.
 Flags : none

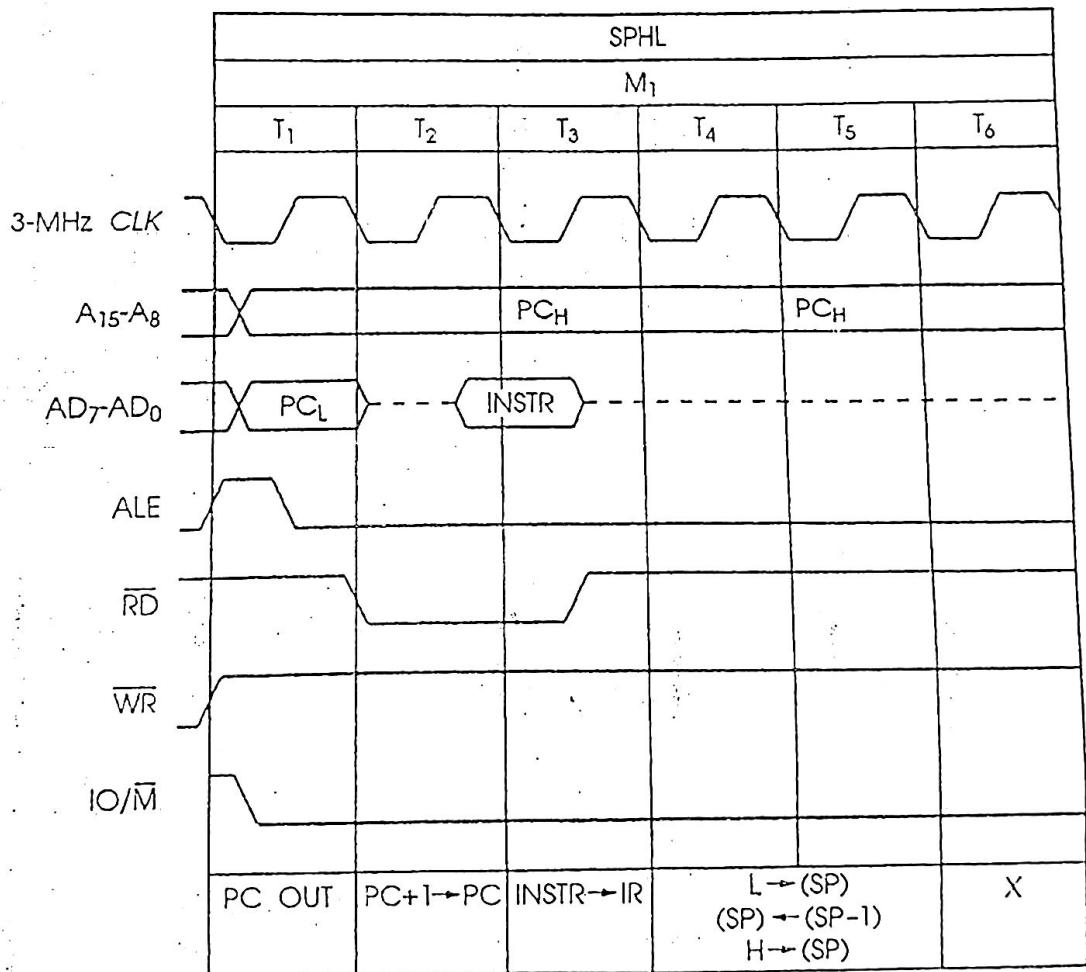


Fig. 2.63. Timing diagram SPHL instruction

IN port (input)
 $(A) \leftarrow (\text{data})$

The data placed on the eight bit bidirectional data bus by the specified port is moved to register A.

1	1	0	1	1	0	1	1
port							

Cycles : 3
States : 10
Addressing : direct
Flags : none

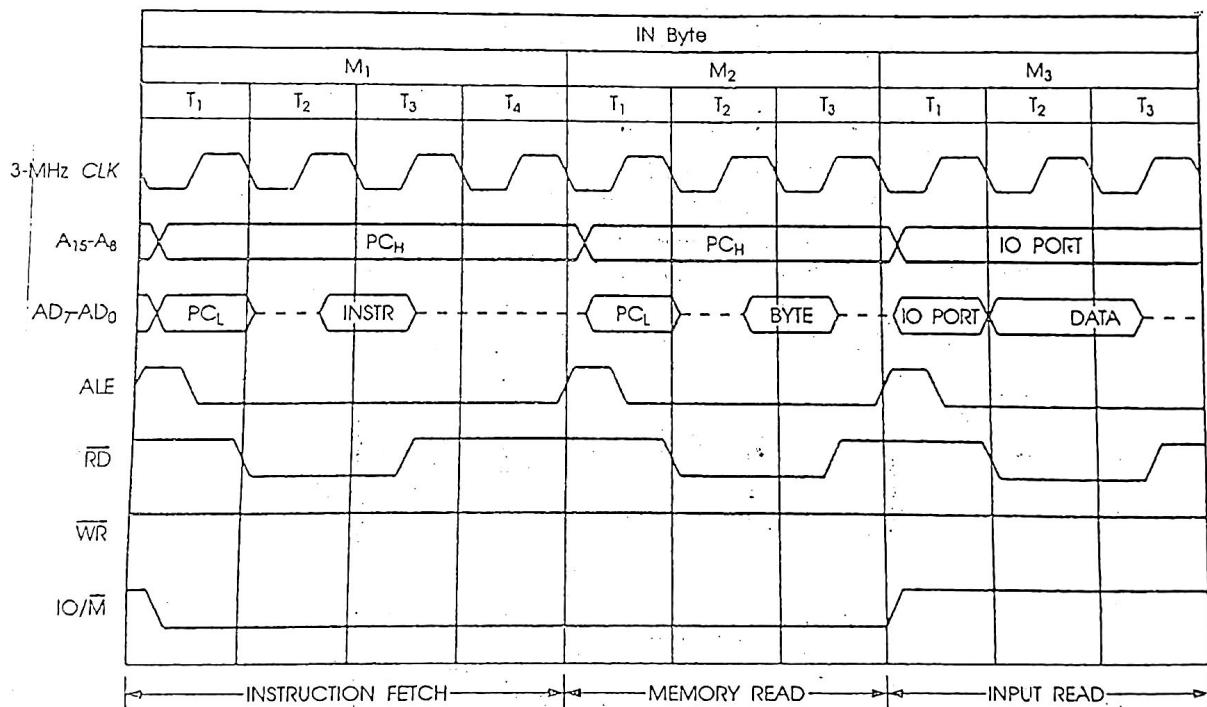


Fig. 2.64. Timing diagram for IN port instruction

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OUT port (Output)
 $(\text{data}) \leftarrow (\text{A})$

The content of register A is placed on the eight bit bi-directional data bus for transmission to the specified port.

1	1	0	1	0	0	1	1
port							

Cycles : 3
 States : 10
 Addressing : direct
 Flags : none

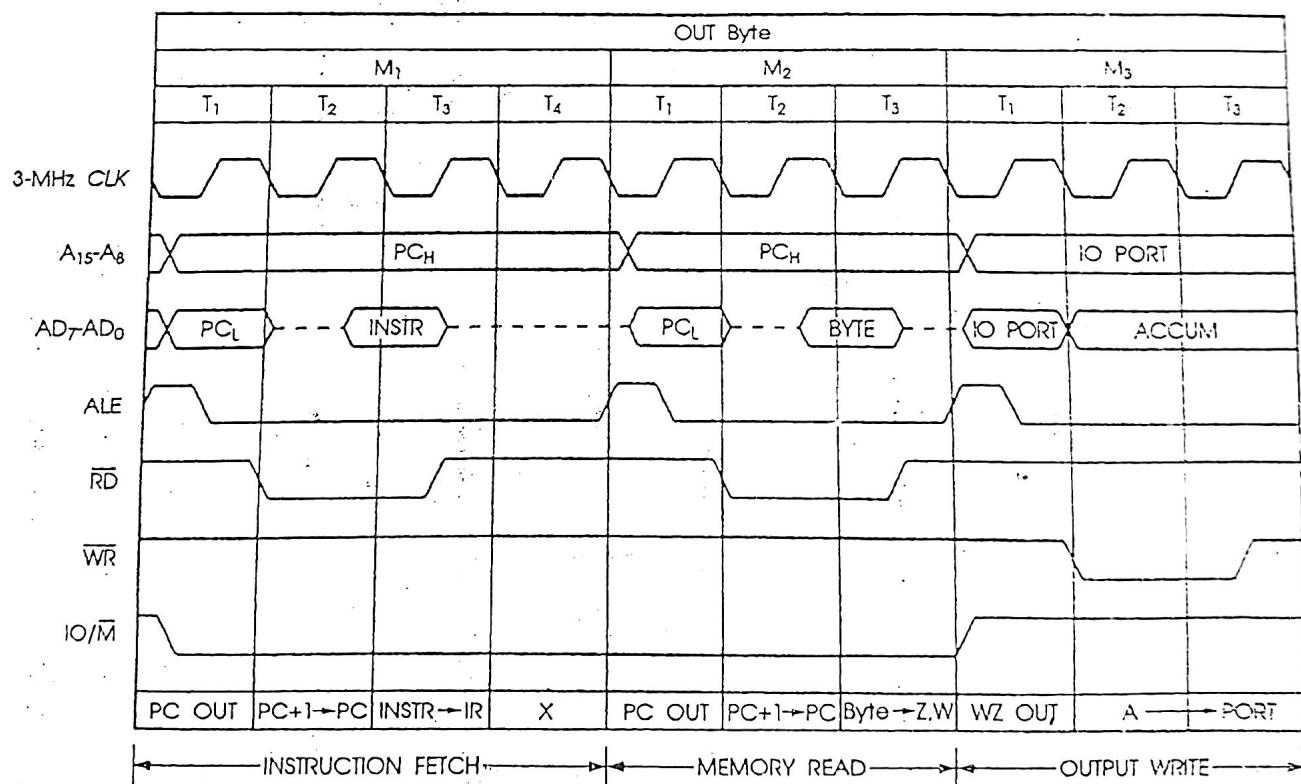


Fig. 2.65. Timing diagram for OUT instruction

EI (Enable Interrupts)

The interrupt system is enabled following the execution of next instruction. Interrupts are not recognized during the EI instruction.

1	1	1	1	1	0	1	1
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Flags : None

Note : Placing an EI instruction on the bus in response to INTA during an INTA cycle is prohibited.

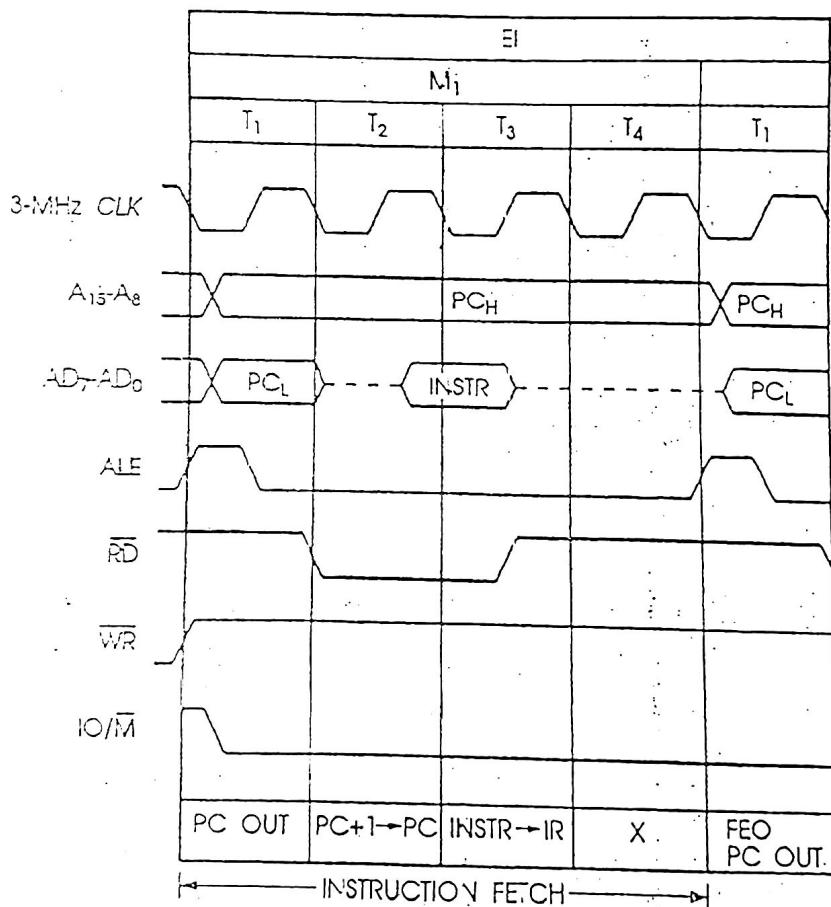


Fig. 2.66. Timing diagram for EI instruction

DI (Disable interrupts)

The interrupt system is disabled immediately following the execution of DI instruction. Interrupts are not recognized during the DI instruction.

1	1	1	1	0	0	1	1
---	---	---	---	---	---	---	---

Cycles : 1

States : 4

Flags : none

Note : Placing a DI instruction on the bus in response to INTA during an INTA cycle is prohibited.

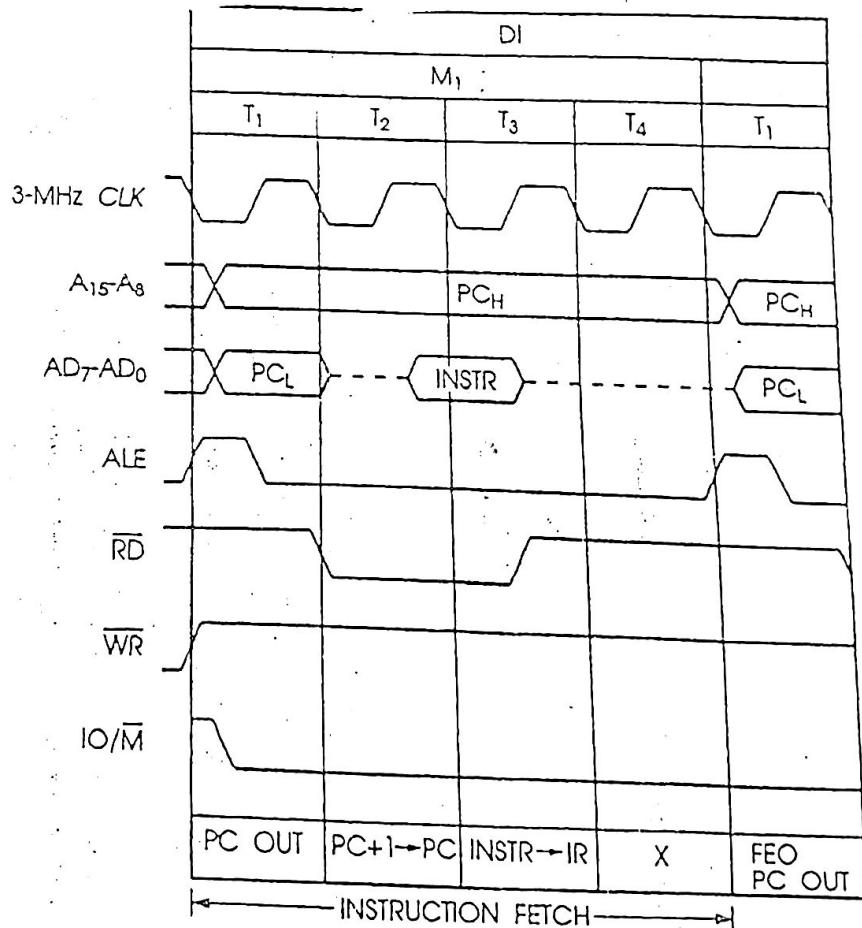


Fig. 2.67. Timing diagram for DI instruction

HLT (Halt)

The processor is stopped. The registers and flags are unaffected. A second ALE is generated during the execution of HLT to strobe out the halt cycle status information.

0	1	1	1	0	1	1	0
---	---	---	---	---	---	---	---

Cycles : 1
 States : 5
 Flags : none

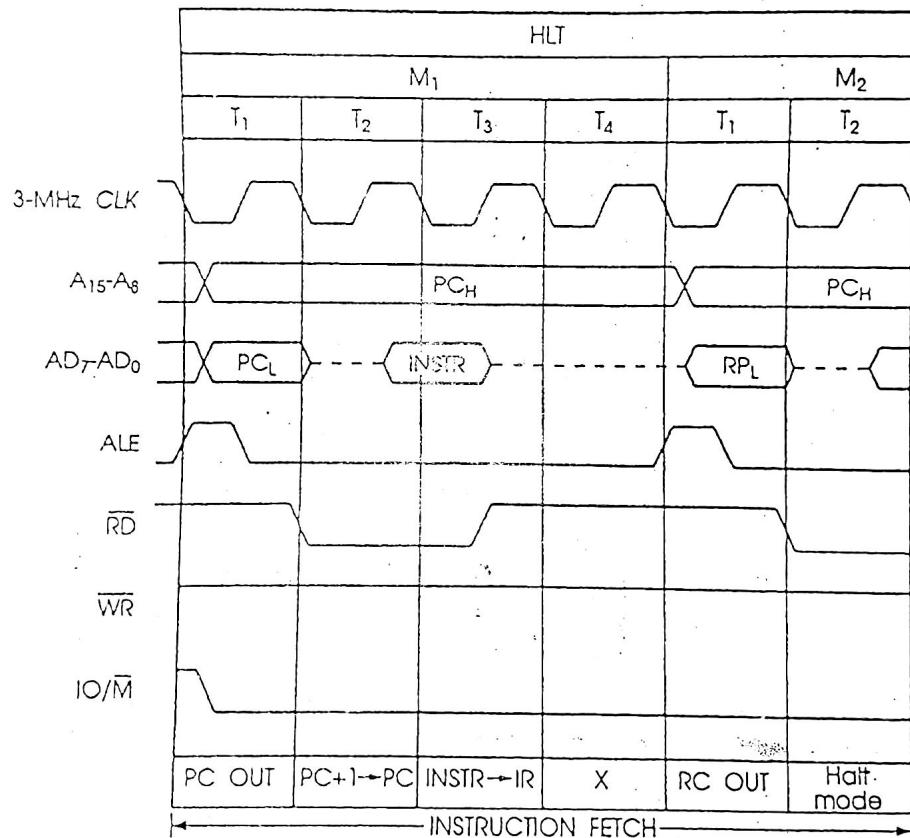


Fig. 2.68. Timing diagram for HLT instruction

INSTRUCTION SET OF 8085

NOP (No operation)

No operation is performed. The registers and flags are unaffected.

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

Cycles : 1
 States : 4
 Flags : none

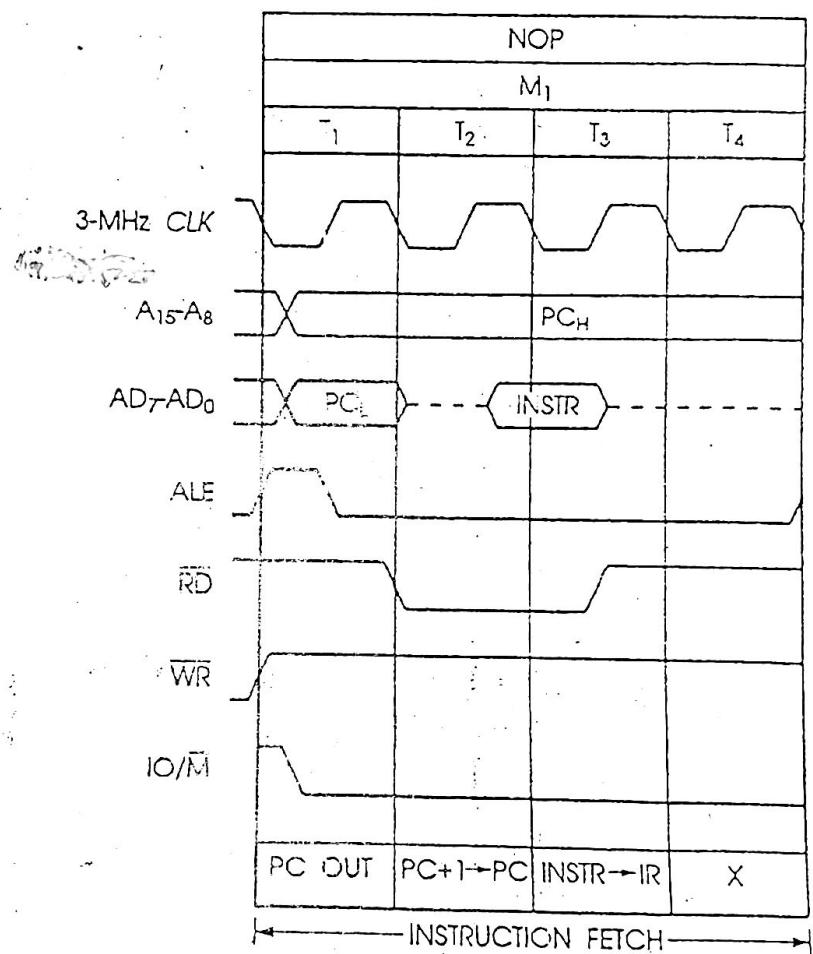


Fig. 2.69. Timing diagram for NOP instruction