MICROPROCESSORS

A Microprocessor is a multipurpose, Programmable clock-driven, register based electronic device that read binary instruction from a storage device called memory, accepts binary data as input and processes data according to those instructions and provides results as outputs.

> A Microprocessor is a clock driven semiconductor device consisting of electronic circuits manufactured by using either a LSI or VLSI technique.

> A typical programmable machine can be represented with three components : MPU(microprocessor) , Memory and I/O as shown in Figure 1 (a)

Microprocessor-based Computer System

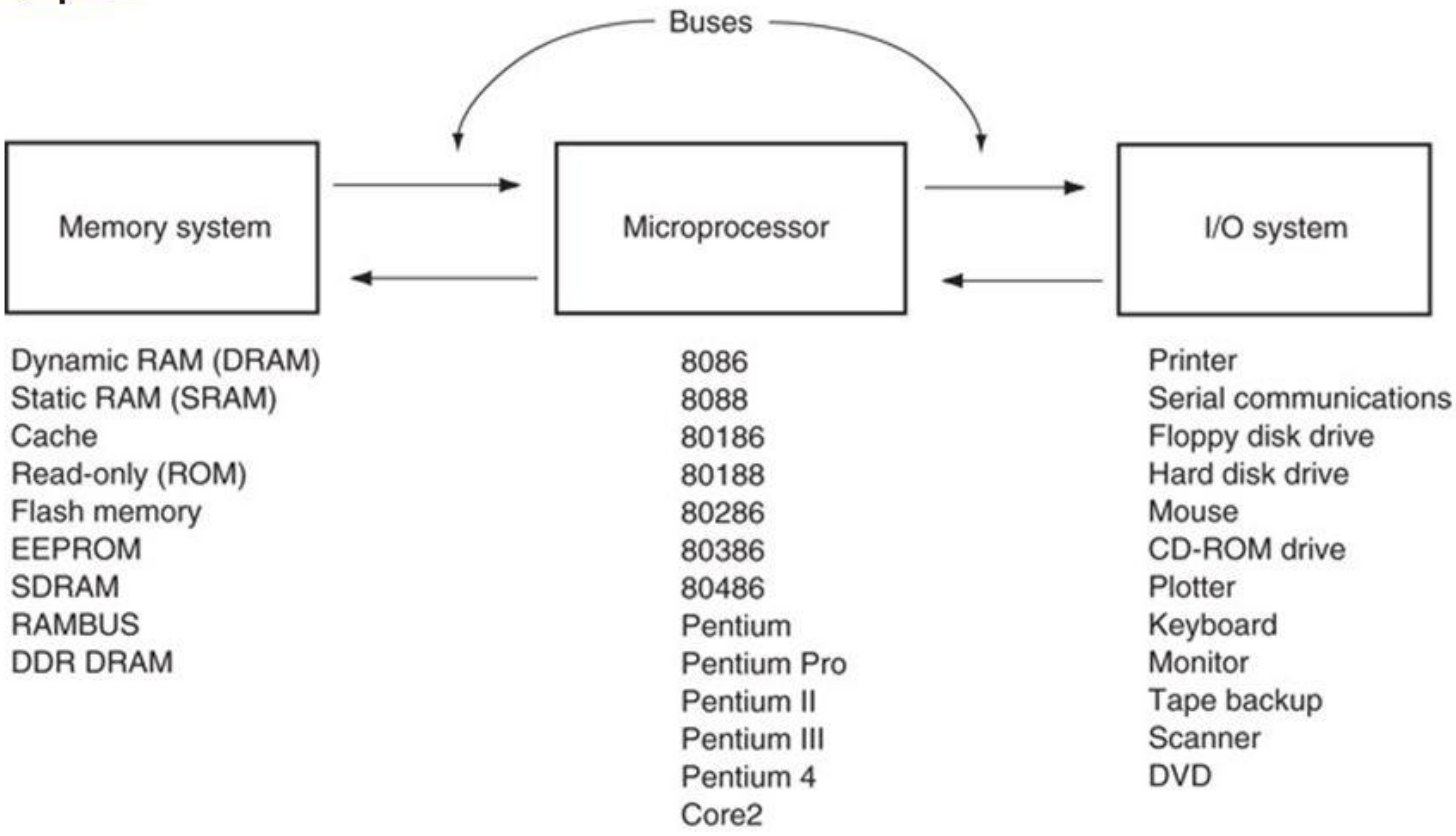


Figure 1(a)

- These three components work together or interact with each other to perform a given task; thus they comprise a system.
  > The machine (system) represented in above figure can be programmed to turn traffic lights on and off, compute mathematical functions, or keep trace of guidance system.
- > This system may be simple or sophisticated, depending on its applications.
- > The MPU applications are classified primarily in two categories : reprogrammable systems and embedded systems.
  > In reprogrammable systems, such as Microcomputers, the MPU is used for computing and data processing.
- > In embedded systems, the microprocessor is a part of a final product and is not available for reprogramming to end user.

MICROCOMPUTER

> As the name implies, Microcomputers are small computers .
> They range from small controllers that work directly with 4-bit words to larger units that work directly with 32-bit words.
> Some of the more powerful Microcomputers have all or most of the features of earlier minicomputers.
> Examples of Microcomputers are Intel 8051 controller-a single board computer, IBM PC and Apple Macintosh computer.

MICROCONTROLLER

> Single-chip Microcomputers are also known as Microcontrollers.
> They are used primarily to perform dedicated functions.
> They are used primarily to perform dedicated functions or as slaves in distributed processing.
> Generally they include all the essential elements of a computer on a single chip: MPU, R/W memory, ROM and I/O lines.
> Typical examples of the single-chip microcomputers are the Intel 8051, AT89C51, AT89C52 and Zilog Z8.
> Most of the microcontrollers have an 8-bit word size, at least 64 bytes of R/W memory, and 1K byte of ROM.
> I/O lines varies from 16 to 40.

APPLICATIONS OF MICROPROCESSORS

- Microcomputers
- Industrial Control
- Robotics
- Traffic Lights
- Washing Machines
- Microwave Oven
- Security Systems
- On Board Systems

EVOLUTION OF MICROPROCESSORS (Intel Series)

4 bit Microprocessors

4004
> Introduced in 1971
> First microprocessor by Intel
> It was a 4-bit microprocessor
> Its clock speed was 740 KHz
> It had 2,300 transistors
> It could execute around 60,000 instructions per seconds
> Used in calculators

4040
> Introduced in 1974
> 4-bit microprocessor
> 3,000 transistors were used
> Clock speed was 740 KHz
> Interrupt features were available

8 Bit Microprocessors

8008
> Introduced in 1972 it was first 8 bit microprocessor
> Its clock speed was 500 KHz
> Could execute 50,000 instruction per second
> Used in: Computer terminals, Calculator, Bottling Machines, industrial Robots

8080
> Introduced in 1974
> It was also 8-bit microprocessor
> Its clock speed was 2 MHz
> It has 6,000 transistors
> 10 times faster than 8008
> Could execute 500,000 instructions per second
> Used In: Calculators, Industrial Robots

8085
> Introduced in 1976
> It was also 8-bit microprocessor
> Its clock speed was 3 MHz
> Its data bus is 8 bit and address bus is 16 bit
> It has 6,500 transistors
> It could execute 769,230 instructions per second
> It could access 64KB of memory
> It has 246 instructions
> Used In: early PC, On-Board Instrument Data Processors

16 Bit Microprocessors

8086
> Introduced in 1978
> First 16-bit microprocessor
> Clock speed is 5 to 10 MHz
> Data bus is 16-bit and address bus is 20-bit
> It had 29,000 transistors
> It could execute 2.5 million instructions per second
> Could access 1MB of memory
> It had 22,000 instructions
> Used In: CPU of Microcomputers

8088
> Introduced in 1979
> It was also 16-bit microprocessor
> It was creates as cheaper version of Intel>s 8086
> 16-bit processor with an 8-bit data bus
> Could execute 2.5 million instructions per second
> The chip become the most popular in the computer industry when IBM used it for its first PC

80286
> Introduced in 1982
> It was 16-bit microprocessor
> Its clock speed was 8 MHz
> Data bus is 16-bit and address bus is 24-bit
> Could address 16 MB of memory
> It has 134,000 transistors
> Could execute 4-million instructions per second

32 Bit Microprocessors

80386
> Introduced in 1986
> First 32-bit microprocessor
> Data bus is 32 bit and address bus is 32-bit
> It could address 4GB of memory
> It has 275,000 transistors
> Clock speed varied from 16 MHz to 33 MHz depending upon different versions
> Different Versions 80386DX, 80386SX ,80386SL

80486
> Introduced in 1989
> 32-bit microprocessor
> Had 1.2 million transistors
> Clock speed varied from 16 MHz to 100 MHz depending upon the various versions
> It had five different versions 80486DX, 80486SX, 80486DX2, 80486SL, 80486DX4
> 8KB of cache memory was introduced

Pentium
> Introduced in 1993
> It was also 32-bit microprocessor
> Clock speed was 66 MHz
> Data bus is 32-bit and address bus is 32-bit
> Could address 4GB of memory
> Could execute 110 million instructions per second
> Cache memory
8KB for Instruction
8KB for data
> Upgraded Version: Pentium Pro

- Pentium II
  - > Introduced in 1997
  - > 32-bit microprocessor
  - > Clock speed was 233 to 450 MHz
  - > MMX technology was supported
  - > L2 cache and processor were on one circuit
  - > Upgraded Version: Pentium II Xenon

  Pentium III
  - > Introduced in 1999
  - > It was 32-bit microprocessor
  - > Clock speed varied from 500 MHz to 1.4 GHz
  - > It had 9.5 million transistors

  Pentium IV
  - > Introduced in 2000
  - > 32-bit microprocessor
  - > Clock speed was from 1.3 GHz to 3.8 GHz
  - > L1 cache was 32 KB and L2 cache was 256 KB
  - > It had 42 million transistors

  Intel Dual Core
  - > Introduced in 2006
  - > It is 32-bit or 64 bit Microprocessor
  - > It has 2-cores
  - > Both cores have their own internal bus and L1 cache but share the external bus and L2 cache
  - > Support SMT (Simultaneously Multithreading Technology)

64 Bit Microprocessors

Intel Core 2

> Introduced in 2006
> 64-bit microprocessor
> Clock speed is from 1.2 GHz to 3GHz
> It has 291 million transistors
> L1 cache- 64 KB per core
> L2 cache- 4 MB
> Versions:

Intel Core 2 Duo
Intel Core 2 Quad
Intel Core 2 Extreme

Intel Core i7

> Introduced in 2008
> 64-bit microprocessor
> It has 4 physical cores
> Clock speed is from 2.67GHz to 3.33 GHz
> It has 731 million transistors
> L1 cache- 64 KB per core
> L2 cache- 256 KB
> L3 cache- 8 MB

Intel Core i5

- Introduced in 2009
  - It is a 64-bit microprocessor
  - It has 4 physical cores
  - Its clock speed is from 2.40 GHz to 3.60 GHz
  - It has 774 million transistors
  - L1 cache- 64 KB per core
  - L2 cache- 256 KB
  - L3 cache- 8 MB/4 MB

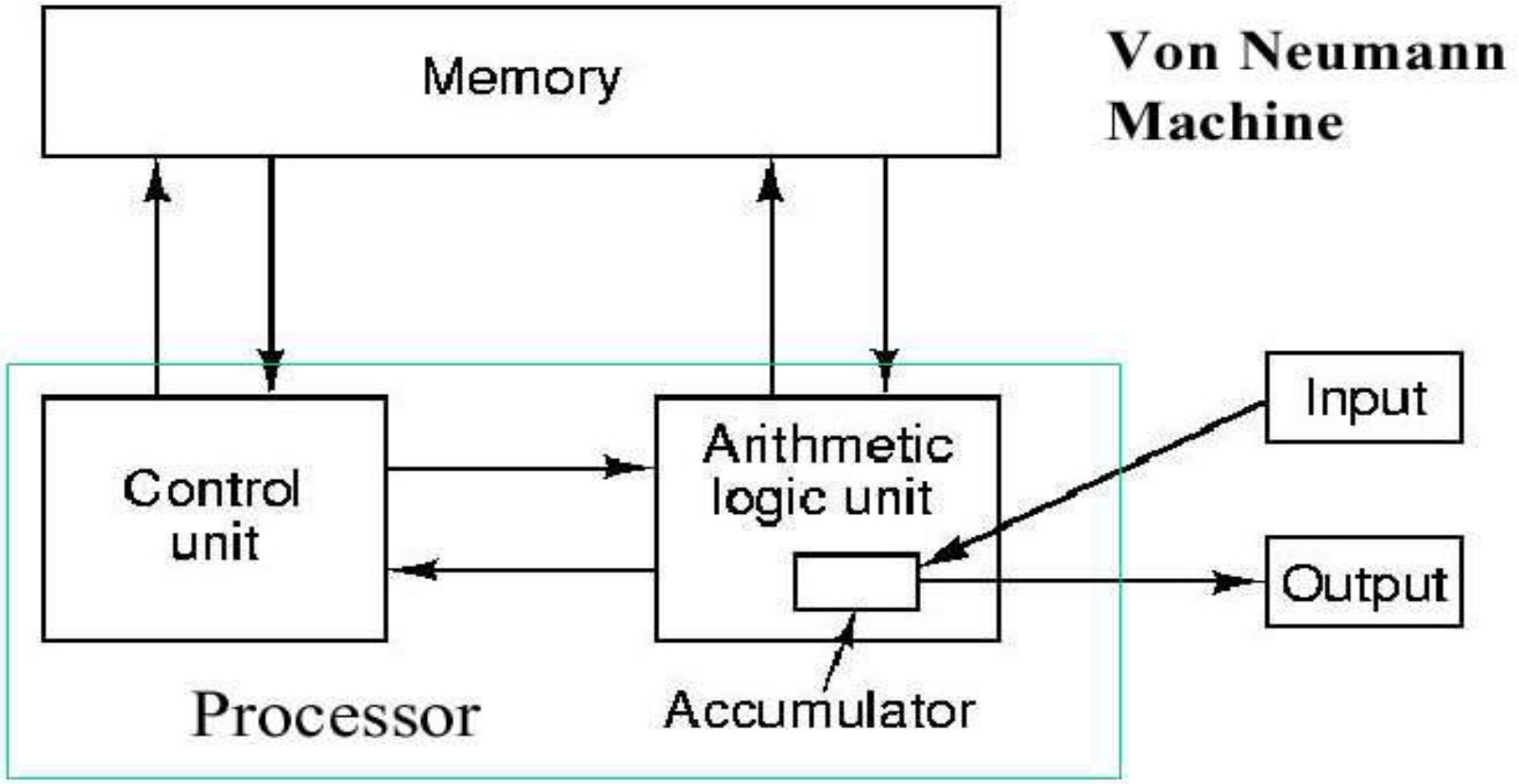
Intel Core i3

- Introduced in 2010
- 64-bit microprocessor
- It has 2 physical cores
- Clock speed is from 2.93 GHz to 3.33 GHz
- It has 382 million transistors
- L1 cache- 64 KB per core
- L2 cache- 256 KB
- L3 cache- 4 MB

Intel Core i9

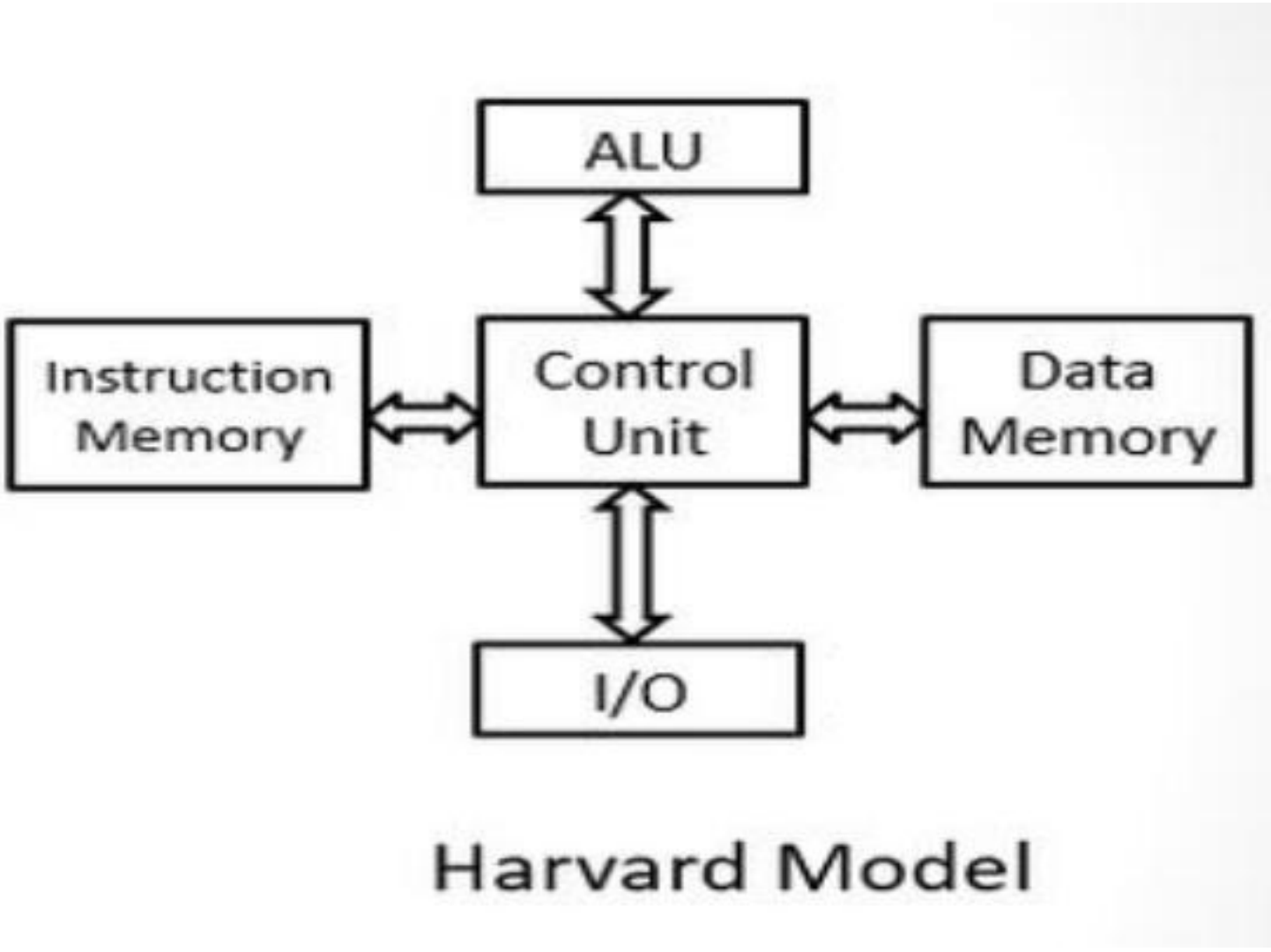
- Introduced in 2017
  - 64-bit microprocessor
  - Estimated from 6-18
  - Clock speed is from 3.33 GHz to 4 GHz
  - It has 781 million transistors
  - Estimated transistor to be 3.5 billions to 7 billions.
  - L2 cache- 1024 KB
  - L3 cache- 4 MB to 26 MB

Von Neumann and Harvard Architecture



>It is named after the mathematician and early computer scientist John Von Neumann.
>The computer has single storage system(memory) for storing data as well as program to be executed.
>It has single set of address/data buses between CPU and memory.
>Processor needs two clock cycles to complete instruction. Pipelining the instructions is not possible with this architecture.
>In the first clock cycle the processor gets the instruction from memory and decodes it. In the next clock cycle the required data is taken from memory.
>For each instruction this cycle repeats and hence needs two cycles to complete an instruction

Harvard Architecture:



>The name is originated from "Harvard Mark I" a relay based old computer.
>The computer has two separate memories for storing data and program.
>It has two set of address/data buses between CPU and memory.
>Processor can complete an instruction in one cycle if appropriate pipelining strategies are implemented.
>In the first stage of pipeline the instruction to be executed can be taken from program memory. In the second stage of pipeline data is taken from the data memory using the decoded instruction or address.
>Most of the modern computing architectures are based on Harvard architecture. But the number of stages in the pipeline varies from system to system.

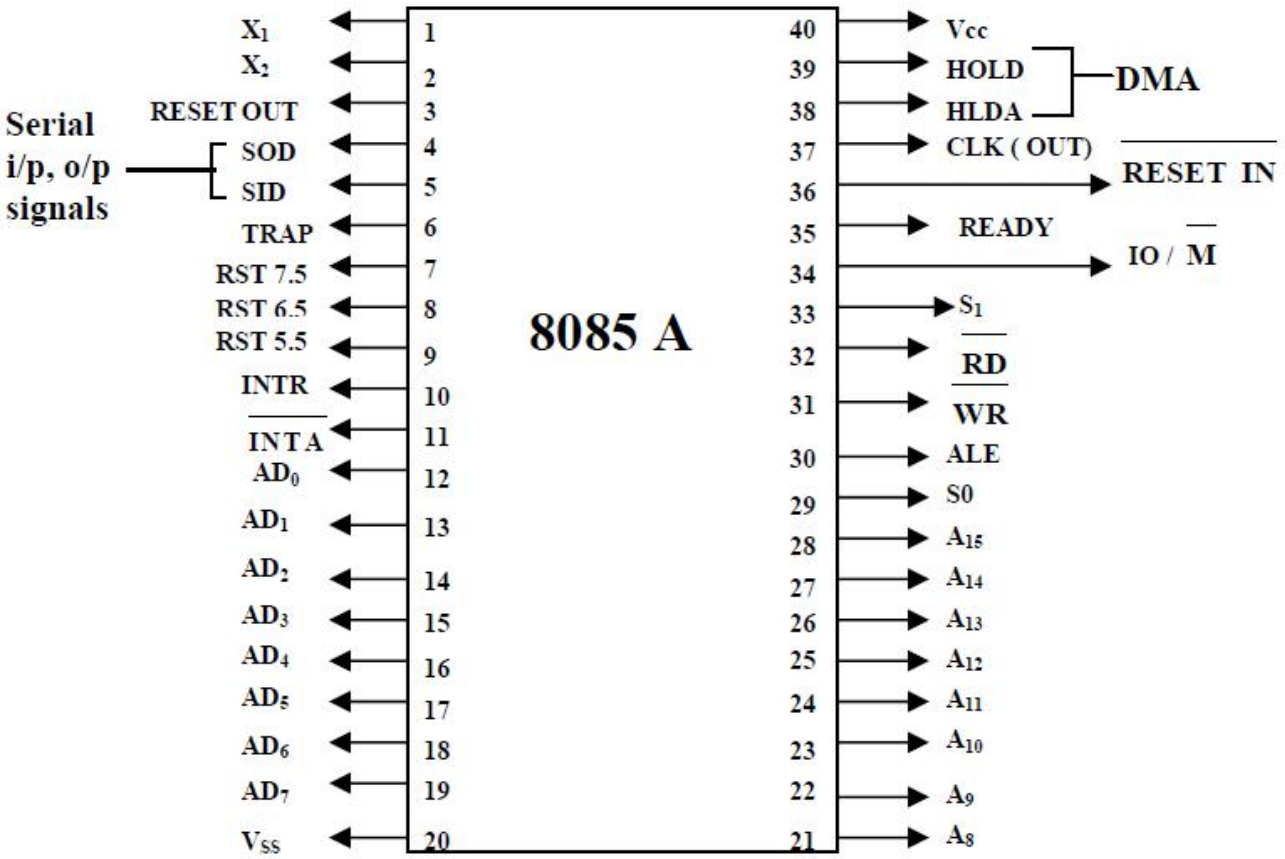
8085 microprocessor

8085 INTRODUCTION

The features of INTEL 8085 are:

> It is an 8 bit processor.
> It is a single chip N-MOS device with 40 pins.
> It works on 5 Volt dc power supply.
> The maximum clock frequency is 3 MHz while minimum frequency is 500 KHz.
> It provides 74 instructions with 5 different addressing modes.
> It has multiplexed address and data bus (AD0-AD7).
> It provides 16 address lines so it can access 216 =64K bytes of memory.
> It generates 8 bit I/O address so it can access 2^8=256 input ports.

Pin Diagram Of 8085



Pin Diagram of 8085

Some important pins are:

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> **AD0-AD7**: Multiplexed Address and data lines.
> **A8-A15:** Tri-stated higher order address lines.
> **ALE**: Address latch enable is an output signal. It goes high when operation is started by processor.
> **S0, S1**: These are the status signals used to indicate type of operation.
> **RD(Read)**: Read is active low input signal used to read data from I/O device or memory.
> **WR(Write**): Write is an active low output signal used write data on memory or an I/O device.
> **READY**: This an output signal used to check the status of output device. If it is low, >P will WAIT until it is high.
> **TRAP**: It is an Edge triggered highest priority, non-maskable interrupt. After TRAP, restart occurs and execution starts from address 0024H.
> **& VSS**=-GND reference

> **RST 5.5, 6.5, 7.5**: These are maskable interrupts and have low priority than TRAP.

> **INTR(Interrupt Request)& INTA(Interrupt Acknowledgment):** INTR is an interrupt request signal after which >P generates INTA or interrupt acknowledge signal.

> **IO/M(IO/Memory**): This is output pin or signal used to indicate whether 8085 is working in I/O mode (IO/M=1) or Memory mode (IO/M=0).

> **HOLD & HLDA**: HOLD is an input signal .When >P receives HOLD signal it completes current machine cycle and stops executing next instruction. In response to HOLD >P generates HLDA that is HOLD Acknowledge signal.

> **RESETIN(Reset In):** This is input signal. When RESETIN is low >p restarts and starts executing from location 0000H.

> **SID:** Serial input data is input pin used to accept serial 1 bit data.

> **SOD**: Serial output data is output pin used to send serial 1 bit data.

> **X1, X2:** These are clock input signals and are connected to external LC or RC circuit. These are divide by two so if 6 MHz is connected to X1X2, the operating frequency becomes 3 MHz.

> **VCC & VSS**: Power supply VCC=+ -5Volt& VSS=-GND reference

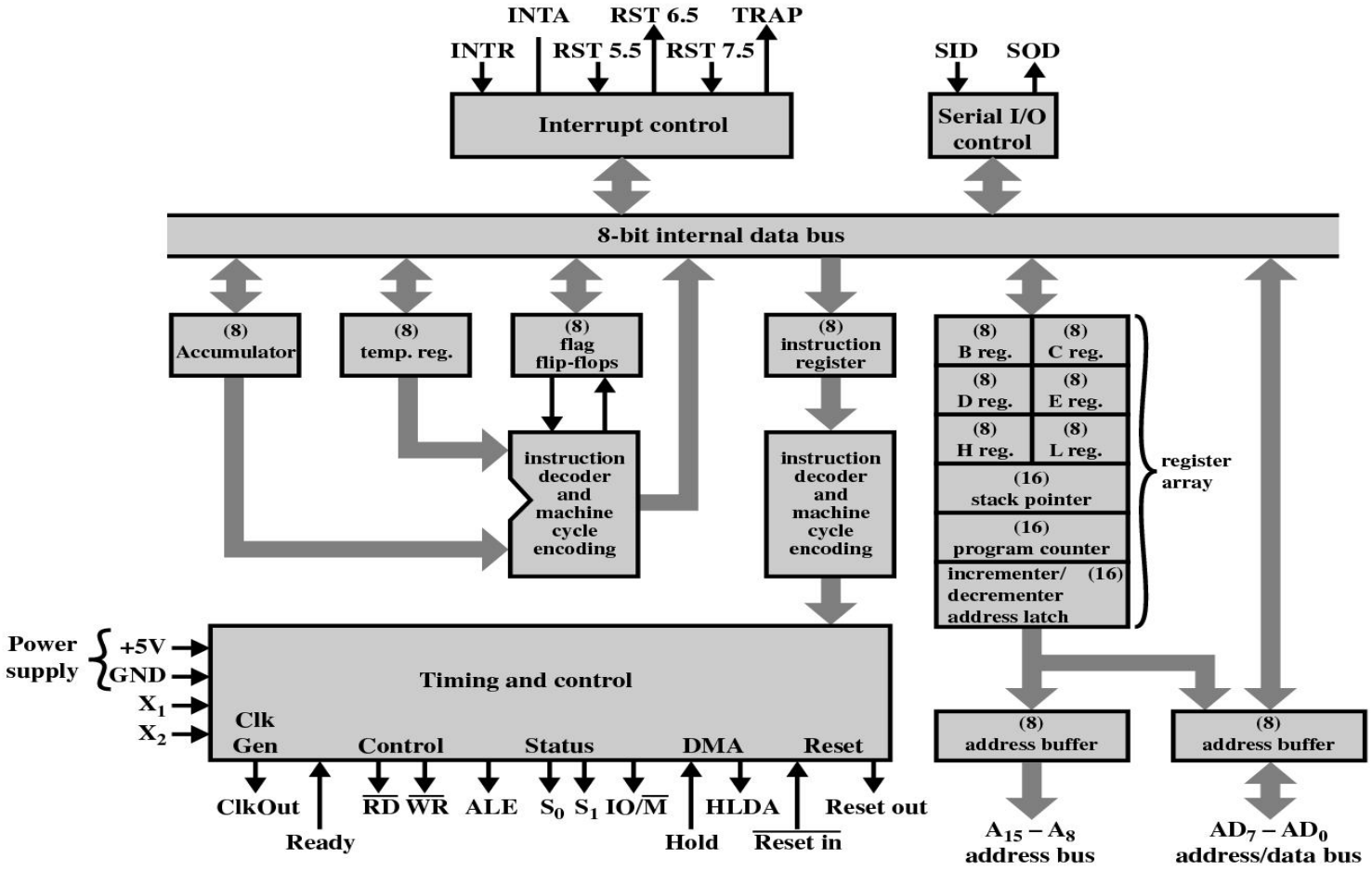


Fig: 8085 ARCHITECTURE

8085 ARCHITECTURE

ARITHMETIC AND LOGIC UNIT (ALU)
Accumulator:
It is 8 bit general purpose register. It is connected to ALU. So, most of the operations are done in Accumulator (A).

Temporary register:
It is not available for user. All the arithmetic and logical operations are done in the temporary register but user can't access it.

Flag Register: It is an 8-bit register which consists of 5 flip flops used to know status of various operations done.

S: Sign flag is set when result of an operation is negative.
Z: Zero flag is set when result of an operation is 0.
AC: Auxiliary carry flag is set when there is a carry out of lower nibble or lower four bits of the operation.
CY: Carry flag is set when there is carry generated by an operation.
P: Parity flag is set when result contains even number of 1's.
Rest are don't care flip flops and reserved for future use.

REGISTER ARRAY

Temporary registers (W, Z): These are not available for user. These are loaded only when there is an operation being performed.

General purpose: There are six 8-bit general purposes register in 8085 namely B, C, D, E, H and L. These are used for various data manipulations. They can be used in pairs as 16-bit registers. The register pairs are: BC pair, DE pair and HL pair.

Special purpose: There are two special purpose registers in 8085:

SP (Stack Pointer): It is a 16-bit register used to hold the address of stack during stack operation i.e PUSH and POP operations.

PC (Program Counter): It is a 16-bit register which holds the address of next instruction to be fetched. When a single byte instruction is executed PC is automatically incremented by 1. Upon reset PC contents are set to 0000H.

TIMIMG AND CONTROL UNIT

This unit synchronizes all the microprocessor operations with the clock and generates the control signals necessary for communication between the microprocessor and peripherals. The RD and WR signals are sync pulse indicating the availability of data on the data bus.

- **INSTRUCTION REGISTER AND DECODER**
  The instruction register and decoder are part of ALU. When an instruction is fetched from memory, it is loaded in the instruction register. The decoder decodes the instruction and establishes the sequence of events to flow. The instruction register is not programmable and cannot be accessed through any instructions.

  INTERRUPT CONTROL
  It accepts different interrupts like TRAP, RST 5.5, RST 6.5, RST 7.5 and INTR. INTA is interrupt acknowledgment signal.

  SERIAL IO CONTROL
  It is used to accept and send the serial 1 bit data by using SID and SOD signals and it can be performed by using SIM & RIM instructions.

Bus system in 8085

- A bus is a communication pathway connecting two or more device.
- A key Characteristics of a bus is that it is a shared transmission medium.
- Multiple device connect to the bus and a signal transmitted by any one device is available for reception by all other device attached to the bus.
- If the two device transmit at the same time their signal will overlap and become garbled.

- Thus only one device at a time can transmit.
- In 8085 there are following types of bus present.

1. **Address Bus**

- The address bus is a group of 16 lines generally identified as Ao to A15.
- The address bus is unidirectional i.e. the bit flow in one direction from MPU to perepheral or a memory location.

- If the process wish to read a word (8,16 or 32 bits) of data from memory, it puts the address bus determines the maximum memory capacity of the system.

2. Data Bus

They are the group of 8 lines used for data flow.

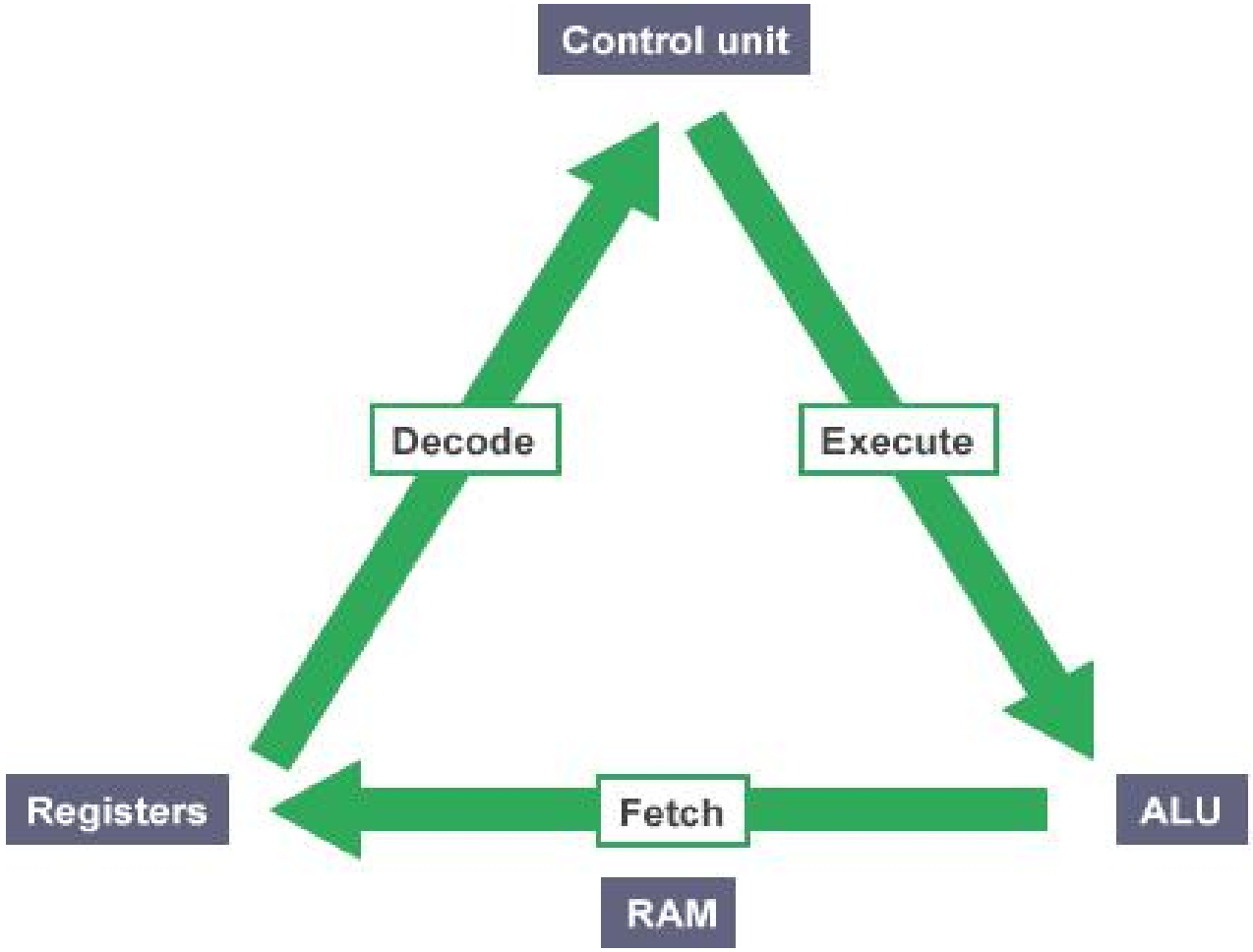
- These lines are in bidirectional nature i.e. data flow in both directioin between the MPU and memory and the pheripheral device.
- Each data line can carry only 1 bit at a time then the number of lines determines how many bits can be transferred at a time.
- The width of data bus is key factor in determining overall system performance.

- For example if the data bus is 8 bit wide and each instructions is 16 bit long then the processor must access the memory module twice during each instruction cycle.

3. **Control Bus**

- They are used to control the access to and the use of the data and address bus.
- Control bus carry the synchronized signal and timing signals.

Concept of Fetch, Decode and Execute



- The main job of the **CPU** is to **execute** programs using the **fetch-decode-execute cycle** (also known as the **instruction cycle**). This cycle begins as soon as you turn on a computer.
- To execute a program, the program code is copied from secondary storage into the main memory. The CPU's **program counter** is set to the memory location where the first instruction in the program has been stored, and execution begins. The program is now running.
- In a program, each **machine code** instruction takes up a slot in the main memory. These slots (or memory locations) each have a **unique memory address**. The program counter stores the address of each instruction and tells the CPU in what order they should be carried out.
- When a program is being executed, the CPU performs the fetch-decode-execute cycle, which repeats over and over again until reaching the STOP instruction.
- **Summary of the fetch-decode-execute cycle**
- The processor checks the program counter to see which instruction to run next.
- The program counter gives an address value in the memory of where the next instruction is.
- The processor fetches the instruction value from this memory location.
- Once the instruction has been fetched, it needs to be decoded and executed. For example, this could involve taking one value, putting it into the **ALU**, then taking a different value from a **register** and adding the two together.
- Once this is complete, the processor goes back to the program counter to find the next instruction.
- This cycle is repeated until the program ends.

Assignment Questions

1. Explain the block diagram of 8085 microprocessor.
2. What are the functions of the following 8085 pins: INTR, ALE, HOLD, TRAP, RESET
3. Explain 8085 flag register in detail.
4. Explain the evolution of intel series microprocessors from 16-bit to 64 bit microprocessors.

- 5. Differentiate between microprocessors and microcontrollers. And explain the applications of both.