

POKHARA UNIVERSITY

Level: Bachelor Semester – Spring Year : 2006
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Describe assembly process for assembly language programs. How does it differ from compilation process of high level language? 8

b) What is addressing modes? Describe different types of addressing modes. 7

2. a) Design the implementation of the simple system whose behaviour can be specified by the following RTL. 8

j:M<-A

o:A<-Y

h:R<-M

N:Y<-R, M<-R

(Use direct connections)

b) Explain the CPU organization of a basic computer with the help of appropriate block diagram. 7

3. a) What is the main difference between RTL and VHDL? Explain with the help of suitable example. 7

b) What are the points the designer should consider while choosing either of micro-programmed control unit or hardwired control unit? 8

4. A kind of very simple CPU has following instructions. 15

Instructions	Instruction Code	Operation
ADD	00AAAAAA	$AC \leftarrow AC + M[AAAAAA]$
AND	01AAAAAA	$AC \leftarrow AC \wedge M[AAAAAA]$
SKIP	10XXXXXX	$PC \leftarrow PC + 1$
INC	11XXXXXX	$AC \leftarrow AC + 1$

- a) Show the RTL for the fetch cycle and execute cycle of each

- instruction and state diagram.
- b) Design registers section and ALU section
 - c) Design Hardwired control unit with necessary control signals.
5. a) Differentiate vertical and horizontal microcode with examples. 7
- b) What do you understand by arithmetic pipeline? Do you think it will speed up the computation? Support your answer with derivation and suitable examples. 8
6. a) What are the different components of memory hierarchy? Explain all components in brief. 7
- b) What do you mean by destination initiated data transfer without handshaking? Illustrate with timing and implementation of an example. 8
7. Write short notes on **(Any Two)**: 5×2
- a) Use of RISC in special purpose computer
 - b) Organization of multi-processor system
 - c) System Buses
 - d) Types of Interrupts

7. Write Short notes on: (Any Two)

5×2

- a) RTL
- b) RISC vs CISC
- c) Parallelism in uniprocessing system
- d) VHDL

POKHARA UNIVERSITY

Level: Bachelor

Semester – Spring

Year : 2007

Programme: BE

Full Marks: 100

Course: Computer Organization and Architecture

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What do you mean by ISA? Differentiate between compilation and assembling process with neat diagrams. 2+6
- b) Write an assembly language program to add the contents of memory locations from 5000H to 5009H and store the result in memory locations 6000H and 6001H. 7
2. a) What are the elements of Machine Instruction? Draw the Instruction Cycle state diagram and explain the flow of instruction. 5
- b) Define bus. Differentiate between address, control and data bus. 5
- c) Show how the value 12345678H is stored in big Endian and Little Endian format. The value starts at location 80H. 5
3. Design a CPU that meets the following specifications. 15
 - a) It can access 64 words of memory, each word being 8 bits wide. The CPU does this by outputting a 6-bit address on its output pins A [5.0] and reading in the 8-bit value from memory on its input D[7.0].
 - b) The CPU contains a 6-bit address register (AR) and program counter; an 8-bit accumulator and data register (DR); and a 2-bit instruction register (IR).
 - c) The CPU must realize the following instruction set.

Instruction	Instruction Code	Operation
JMP1	00AAAAAA	PC<-AAAAAA+1
INC2	01XXXXXX	AC<-AC+2
ADD1	10AAAAAA	AC<-AC+M[AAAAAA]+1
SKIP	11XXXXXX	PC<-PC+1

- I. Show the RTL for each fetch cycle and execute cycle of each instruction and state diagram.

- II. Design registers section and ALU section.
- III. Design hardwired control unit with necessary control signals.
4. a) What do you mean by VHDL? What are the primary sections of VHDL? Explain by taking an example. 3+5
- b) What is the main objective of pipelining? How does it improve the speed of computation? 2+5
5. a) Differentiate between horizontal and vertical microcode. Write down the advantages of micro programmed control unit over hardwired control unit. 7
- b) What do you mean by virtual memory? How does segmentation help to organize memory? Explain with an example. 2+6
6. a) Write an algorithm to multiply two positive numbers. Also, draw the appropriate hardware to implement that algorithm. 8
- b) What are the objectives of hierarchical memory system? Describe the different levels of memory hierarchy. 7
7. Write short notes on *(Any Two)*: 2×5
- a) Universal asynchronous receiver transmitter
 - b) RISC versus CISC
 - c) Flynn's classification of computers
 - d) Branch conflicts in RISC pipeline
- | Question | Notes Taken | Information |
|--------------------|-------------|-------------|
| 1-AAAA>21 | AAAAAA00 | 100000 |
| AC-BC+5 | 00000010 | 0001 |
| 1-AAAAAA[AC+BC]>25 | 10000010 | 10010 |
| BC->25 | 10000000 | 10011 |

POKHARA UNIVERSITY

Level: Bachelor

Semester – Fall

Year : 2008

Programme: BE

Full Marks: 100

Course: Computer Organization and Architecture

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain different types of addressing modes with examples. 7
- b) Define different sections of CPU organization and show their connectivity. 8
2. a) A computer system with an 8-bit address bus and 8-bit data bus uses isolated I/O. It has 64 bytes of ROM starting at address 00H; 128 bytes of RAM starting at address 40H; an input device at address 40H. Show the design for this system. 8
- b) Explain design procedure to show the hardware to implement following RTL code in one combined system. 7
 - i) $X \leftarrow X + Y$
 - ii) $X \leftarrow X + Y' + 1$
 - iii) $X \leftarrow X^Y$
3. Very Simple CPU has the following instructions.
 - o JMP AAAAAAA (Jump to address AAAAAAA)
 - o ADD AAAAAAAA (Add content of accumulator to the binary value AAAAAAAA)
 - o LDA AAAAAAAA (Load accumulator with the binary value AAAAAAAA)
 - o STA AAAAAAA (load the given memory address with the content of accumulator)
 - a) Write the RTL code for micro-operations of each cycle. Also design state diagram. 7
 - b) Design Register and ALU section. 8
4. a) Differentiate between hardwired and micro-programmed control unit. 8

How does micro-sequencer work as control unit?

b) Why BCD format is important in computer world? Design a circuit for BCD addition. 7

5. a) What is the concept of hierarchical memory system? What are elements of memory hierarchy? 7

b) What are the different types of cache memory mapping techniques? Explain any one. 8

6. a) Explain the characteristics of RISC processor. 8

b) Describe some topologies of multiprocessor system. 7

7. Write short notes on *any two.* 2x5

a) IEEE 754 floating point standard.

b) UART

c) VHDL and its significance in design.

POKHARA UNIVERSITY

Level: Bachelor Semester – Fall Year : 2009
Programme: B.E. Full Marks : 100
Course: Computer organization and architecture Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the issues to consider while designing instruction set architecture? 7
b) How a 16 X 2 memory subsystem can be constructed from two 8 x2 ROM chips with low-order interleaving? Explain. 8

2. Design a very simple CPU that has 6-bit address register (AR), 6-bit program counter (PC), 8-bit data register (DR) and 2-bit instruction register (IR). The CPU must execute the following instructions:

Instruction	Instruction Code	Operation
COM	00XXXXXX	$AC \leftarrow AC'$
AND	01AAAAAA	$AC \leftarrow AC \wedge M[AAAAAA]$
JREL	10AAAAAA	$PC \leftarrow PC + AAAAAA$
SKIP	11XXXXXX	$PC \leftarrow PC + 1$

- | | |
|--|--------|
| <p>a) Show the RTL code for the fetch and execute cycles for each instruction and draw the state diagram.</p> <p>b) Show the final register section and hardwired control unit for the same CPU.</p> | 7
8 |
| <p>3. a) Taking the reference of the very simple CPU of question No.2, design a very simple microsequencer using horizontal microcode.</p> <p>b) For the same very simple CPU design a very simple microsequencer using vertical microcode. Compare the horizontal and vertical microcode from the above scenario.</p> | 7
8 |
| <p>4. a) Write the RTL code for the booth's Algorithm. Using the same code</p> | 8 |

- trace the multiplication of (-5) and (3).
- b) Explain different design issues of cache memory. 7
5. a) What are the significance of cache memory? Write different types of mapping technique. 7
- b) How DMA controller can be incorporated in a computer system? 8
6. a) Write about the instruction pipeline conflicts. Explain the remedy to overcome data conflicts. 8
- b) What do you understand by the term "Cache Coherence"? Explain how can we resolve the Cache coherence problem? 7
7. Write short notes on: (Any Two) 5x2
- a) VHDL
- b) RISC VS CISC
- c) Virtual Memory

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE

Semester – Spring

Year : 2009

Full Marks: 100

Pass Marks : 45

Course: Computer Organization and Architecture

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define addressing mode. Explain different types of addressing mode with example. 8
b) Define VHDL. Write the VHDL program for full adder. 7
 2. Design a very simple CPU that has 6-bit address register (AR), 6 bit program counter (PC), 8 bit data register (DR) and 2 bit instruction register (IR). The CPU must execute the following Instructions:
- | Instruction | Instruction Code | Operation |
|-------------|------------------|----------------------------------|
| COM | 00XXXXXX | $AC \leftarrow AC'$ |
| JMP 1 | 01AAAAAA | $PC \leftarrow AAAA+1$ |
| ADD 1 | 10AAAAAA | $AC \leftarrow AC + M[AAAAAA]+1$ |
| SKIP | 11XXXXXX | $PC \leftarrow PC+1$ |
- a) Write the RTL code of micro-operations for fetch and execute cycles of each instruction. 8
b) Design the register and ALU section to implement those micro-operations. 7
 3. a) A computer system with an 8 bit address bus and an 8 bit data bus uses isolated I/O. It has 64 bytes of EEPROM starting at address 00H; 64 bytes of RAM starting at address next to the last address of EEPROM and an input device at address F0H. Show the design for this system. Include all necessary logic. 8
b) Write the differences between hardwired and micro-programmed control unit. 7
 4. a) What is the purpose of using BCD in computer system? Design 8

- hardware for a BCD adder. *(Any Two)*
- b) Write the RTL code for Booth's algorithm. Using same code trace the multiplication of (-5) and (3). 7
5. a) What is hierarchical memory system. Explain all the elements of memory hierarchy? 7
- b) What is virtual memory? Explain about paging and segmentation techniques regarding the memory management. 8
6. a) Mention different I/O techniques. Differentiate programmed I/O and interrupt I/O. 8
- b) Describe different types of topologies of multiprocessor system. 7
7. Write short notes on **(Any Two)**: 5×2
- a) DMA
 - b) Hit ratio
 - c) Instruction Set Architecture

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE

Semester – Fall

Year : 2010
Full Marks : 100
Pass Mark : 45
Time : 3 hrs

Course: Computer Organization and Architecture

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a. Describe the assembly process for assembly language programs. 8
How does it differ from the compilation process?
- b. Design the 16x 4 memory subsystem constructed from two 7
16 X2 ROM chips with
 - i. High Order Interleaving
 - ii. Low Order Interleaving
2. a. Show the hardware to implement the following RTL code. 7
 - i. $M : X \leftarrow X + Y$
 - ii. $N : X \leftarrow X + Y' + 1$
 - iii. $O : X \leftarrow X^Y$
- b. What do you mean by micro sequencer ?Explain with the generic micro sequencer organization. 8
3. a. For a very simple CPU with the following instruction sets: 8

Instruction	Operation	Instruction code
ADD AAAAAAA	$AC \leftarrow AC + M[AAAAAAA]$	00AAAAAA
AND AAAAAAA	$AC \leftarrow AC \wedge M[AAAAAAA]$	01AAAAAA
COM	$AC \leftarrow AC'$	10XXXXXX
OR AAAAAAA	$AC \leftarrow AC \vee M[AAAAAAA]$	11AAAAAA

- i. Describe specifications and draw State diagram.
- ii. Design ALU and Register set

- b. For the question given in number 3,a. design a hardwired control unit. 7
4. a. Write the steps of Booth algorithm? Show the trace of the RTL code for Booths algorithm for $x = 0110$ and $Y = 1011$ 8
 - b. What are the different topologies used to interconnect MIMD

computers? Describe with suitable diagrams.

5. a. Define Memory hierarchy? How to convert the logical address to physical address .Explain with diagrams 8
- b. Why we use asynchronous data Transfer mechanism ?Explain source initiated data transfer with examples. 7
6. a. What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Also describe what the solutions to correct these conflicts are? 8
- b. Describe the microinstruction format? Explain the horizontal and vertical microcode. 7
7. Write short notes on (Any Two): 2×5
- a. VHDL
 - b. DMA
 - c. Instruction formats

POKHARA UNIVERSITY

Level: Bachelor

Semester – Fall

Year : 2011

Programme: BE

Full Marks: 100

Course: Computer Organization and Architecture

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | | | |
|----|---|---|
| 1. | a) What is system bus? Explain in details. | 7 |
| | b) Define ISA. Explain different addressing modes. | 8 |
| 2. | a) Define VHDL. Write the VHDL program for full adder. | 7 |
| | b) How a 16×2 memory sub system can be constructed from two 8×2 ROM chip with low order interleaving and high order interleaving. Explain with diagram. | 8 |

OR

- | | | |
|----|--|----|
| a) | What is RTL? Write the RTL for different arithmetic operations.
Design a 4-bit decimal right shifting circuit. | 7 |
| b) | What is instruction cycle? Explain instruction cycle state diagram. | 8 |
| 3. | Design a CPU that meets the following specification: | 15 |
| a) | It can access 64 bytes of memory each 8 bit wide. The CPU does this by outputting a 6 bit address on its output pin A[5...0] and reading 8-bit value from memory on its inputs D[7...0]. | |
| b) | The CPU contains 6-bit AR, 6-bit PC, 8-bit Dr and 2-bit IR. | |
| c) | The CPU realize following instruction: | |

Instruction	Instruction Code	Operation
SUB	00AAAAAA	$AC = AC - M[AAAAAA]$
AND	01AAAAAA	$AC = AC \wedge M[AAAAAA]$
JMP	10AAAAAA	GOTO AAAAAA
INC	11XXXXXX	$AC = AC + 1$

- i. Write the RTL for fetch and execute cycle and draw its register section for CPU.
- ii. Design a hardwired control unit for above CPU.
4. a) Differentiate a hardwired control unit with micro-programmed control unit. 7
- b) Write the RTL code for Booth's algorithm. Using same code trace the multiplication of (-5) and (3). 8
5. a) What is hierarchical memory system? Explain any one of the cache mapping technique? 7
- b) What do you mean by destination initiated data transfer without handshaking? Illustrate with timing and implementation of an example. 8
6. a) Explain different types of conflict in instruction pipeline with example. 8
- b) Describe different types of topologies of multiprocessor system. 7
- OR**
- a) What is parallelism? How can it be achieved in uniprocessor systems? 7
- b) Show the layout of the cache for a CPU that can address $1M \times 16$ of memory; the cache holds $8k \times 16$ of data and has the following mapping strategies: give the number of bits per location and total number of locations 8
- i. Fully Associative
 - ii. Direct Mapped
 - iii. Two-way associative
7. Write short notes on **any two:** 2×5
- a) DMA
 - b) RISC versus CISC
 - c) Virtual Memory

POKHARA UNIVERSITY

Level: Bachelor

Semester – Spring

Year : 2011

Programme: BE

Full Marks: 100

Course: Computer Organization and Architecture

Pass Marks: 45

Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a. What are the different types of instructions? Explain with example. 8
- b. Design the 16×2 memory subsystem using: 7
 - i. internal linear configuration
 - ii. two dimensional configuration.
2. a. What is DMA? Explain the different register section within a DMA, explain their uses. 8
- b. What is RTL? Write the RTL for different logical operations. 7
Design a 4-bit decimal left shifting circuit.
3. a. Design a very simple CPU with the following instruction set and show the RTL code for execute cycle for each instruction: 8

Instruction	Instruction Code	Operation
SHL	00AAAAAA	$AC \leftarrow AC + AC$
AND	01AAAAAA	$AC \leftarrow AC \wedge M[AAAAAA]$
OR	10AAAAAA	$AC \leftarrow AC \vee M[AAAAAA]$
NEG	11XXXXXX	$AC \leftarrow AC' + 1$

- b. From the above table also design the ALU and Hardwired control unit for the very simple CPU. 7
4. a. Describe the microinstruction format. Explain the advantages and disadvantages of horizontal and vertical microcode. 8
- b. What are the features distinguish RISC processors from their CISC processor? Explain. 7
5. a. Write the RTL code for the Booths' Algorithm. 7
- b. What is memory hierarchy? Explain the importance of cache memory and virtual memory in hierarchy. 8
6. a. Why we used asynchronous data transfer mechanism? Explain Programmed I/O with examples. 8
- b. Describe different system topologies used to organize multiprocessors. 7
7. Write short notes on **any two:** 2×5
 - a. MIMD architecture
 - b. VHDL
 - c. Register window

POKHARA UNIVERSITY

Level: Bachelor	Semester – Fall	Year : 2012
Programme: BE		Full Marks: 100
Course: Computer Organization and Architecture		Pass Marks: 45
		Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What do you mean by instruction format? What are the factors to be considered while designing the instruction set of a computer? 7
 - b) Design the 8×2 ROM memory using Linear and two dimensional Organization. 8
 2. a) What is RTL? Write the RTL for Arithmetic and Logical Instruction. 7
 - b) Design a very simple CPU that has the following instruction set and Show the RTL code for execute cycle of each Instruction. Also design the Register sections with ALU. 8
- | Instruction | Instruction Code | Operation |
|-------------|------------------|-----------------------------------|
| ADD | 00AAAAAA | $AC \leftarrow AC + M[AAAAAA]$ |
| OR | 01AAAAAA | $AC \leftarrow AC \vee M[AAAAAA]$ |
| JMP | 10AAAAAA | GOTO A'AAAAAA |
| INC | 11XXXXXX | $AC \leftarrow AC + 1$ |
3. a) For the question given in number 2.b), design a hardwired control unit. 7
 - b) Write the steps of booth algorithm? Show the trace of the RTL code for Booths Algorithm for (-8×5) 8
 4. a) What is virtual memory? Describe how paging is implemented in virtual memory. 7
 - b) Describe the working principle of DMA with suitable diagram. 8
 5. a) What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Describe the solutions to correct data conflicts. 8
 - b) Why we used Asynchronous Data Transfer mechanism ?Explain source initiated data transfer with examples 7
 6. a) Why parallel processing is necessary? Explain various types of 8

1

- Multiprocessor organisation.
- b) Describe the working principle of micro-programmed control unit of very simple CPU. How does horizontal microcode differ from vertical microcode? 7
7. Write short notes on any two: 2×5
 - a) VHDL
 - b) Cache memory
 - c) Compiling and Assembling Process

POKHARA UNIVERSITY

Level: Bachelor	Semester – Fall	Year : 2013
Programme: B.E		Full Marks: 100
Course: Computer Organization and Architecture		Pass Marks: 45
		Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the issues while designing an instruction set? Compare an assembling and compiling Process with an examples 7
b) Design a 16×2 ROM memory using 8×2 ROM in 8
i) Higher order interleaving ii) Lower lever Interleaving.
 2. a) Write a VHDL code for the Half Adder. 7
b) Design a very simple CPU has the following instruction set and Show the RTL code for execute cycle of each Instruction 8
- | Instruction | Instruction Code | Operation |
|-------------|------------------|-------------------------------------|
| SUB | 00AAAAAA | $AC \leftarrow AC - M[AAAAAA]$ |
| OR | 01AAAAAA | $AC \leftarrow AC \vee M[AAAAAA]$ |
| AND | 10AAAAAA | $AC \leftarrow AC \wedge M[AAAAAA]$ |
| DEC | 11XXXXXX | $AC \leftarrow AC - 1$ |
3. a) From the above table also design the ALU and Hardwired control unit for the very simple CPU. 7
b) Write do you mean by microinstruction? Describe the microinstruction format. 8
 4. a) Explain the Hardware implementation of addition and subtraction algorithm 7
b) Write the RTL code for the Shift Add Multiplication Algorithm. Use the same code to trace the multiplication of (3) and (4) 8
 5. a) Describe how a 1KB cache is mapped directly with a 1MB Main Memory. Use suitable diagram to show the configuration and determine the tag and index. 8
b) Describe the working principle of I/O Processors with suitable diagram. 1
 6. a) What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Describe the solutions to correct data conflicts 8
b) What are the different topologies used to interconnect MIMD computers? Illustrate with suitable diagrams. 7
 7. Write short notes on **any two:** 2×5
 - a) UART's Internal Configuration
 - b) Advance capabilities of VHDL •
 - c) Set Associative Mapping

POKHARA UNIVERSITY

Level: Bachelor	Semester: Spring	Year : 2013
Programme: BE		Full Marks: 100
Course: Computer Organization and Architecture		Pass Marks: 45
		Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the issues to consider while designing ISA? List out the advantages and disadvantages of Direct Addressing mode? 7
- b) How can a 8×4 memory subsystem constructed from two 8×2 ROM chips with control signals. Explain with diagram. 8
2. a) Explain the different sections of VHDL design code. Write VHDL code for D- Flip-flop. 8
- b) Define Instruction Cycle. Explain the structural components of computer with block diagram and bus connectivity? 7
3. ✓ Design a CPU that meets the following specification 15
 - a) It can access 64 bytes of memory each 8 bit wide. The CPU does this by outputting a 6 bit address on its output pin A{5...0} and reading 8-bit value from memory on its inputs D[7...0]
 - b) The CPU contains 6-bit AR, 6-bit PC, 8-bit Dr and 2-bit IR
 - c) The CPU realize following instruction

Instruction	Instruction code	operation
SUB	00AAAAAA	AC=AC - M[AAAAAA]
AND	01AAAAAA	AC=AC^M[AAAAAA]
JMP	10AAAAAA	GOTO AAAAAAA
INC	11XXXXXX	AC=AC+1

 - i. Write the RTL for fetch and execute cycle and draw state diagram.
 - ii. Design a register section and hardwired control unit for above CPU.
4. a) Explain the generation of micro-operation using horizontal as well as vertical microcode. Write two ways to reduce number of micro- 7

1

- instruction.
- b) Write the RTL code for shift-add multiplication algorithm. Using same code, trace the multiplication of (13) and (11). 8
5. a) Differentiate between Segmentation and Paging? Describe the four most common replacement algorithms related to design issues of cache memory? 7
- b) What do you mean by Source-initiated data transfer with handshaking? Illustrate with timing and implementation of an example. 8
6. a) Explain major set of design principles related to RISC architecture. Calculate the window size and total number of registers. Given: No. of Global registers=10, No. of Local registers=10, No. of common registers=6, No. of windows= 4. 8
- b) Define Mesh Topology. Describe different memory organization of multiprocessor system. 7
7. Write short notes on: *(Any Two)* 2×5
 - a) DMA
 - b) Arithmetic Pipelining
 - c) Microsequencer. (*Microsequencer*)

POKHARA UNIVERSITY

Level: Bachelor

Semester: Fall

Year : 2014

Programme: BE

Full Marks: 100

Course: Computer Organization and Architecture

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | | | |
|-------|--|----|
| 1. a) | Explain the assembling and compiling process with suitable examples. | 7 |
| b) | What is system bus? Explain in details. | 8 |
| 2. a) | A Computer system with an 8 bit address bus and an 8 bit data bus using isolated I/O. It has 16x8 ROM starting at the address 00H constructed using 8x8 chips; 64x8 of RAM starting at address 80 H constructed using 64x4 chips. There is an I/O device at 40 H. Show the design for the system. | 8 |
| b) | How a 16×2 memory sub system can be constructed from two 8×2 ROM chip with low order interleaving and high order interleaving. Explain with diagram. | 7 |
| 3. | Design a CPU that meets the following specification:
It can access 64 bytes of memory each 8 bit wide. The CPU does this by outputting a 6 bit address on its output pin A{5...0} and reading 8 bit value from memory on its input D{7...0}. | 15 |
| 4. a) | Describe the microinstruction format? Explain the horizontal and vertical micro code. | 7 |
| b) | Write the RTL code for Booth's algorithm. Using same code trace the multiplication of (-5) and (3). | 8 |
| 5. a) | Show the layout of the cache for a CPU that can address 1M x 16 of memory; the cache holds 8k x 16 of data and has the following mapping strategies. Given the number of bits per location and total number of locations as well.
i. Fully Associative
ii. Direct Mapped
iii. Two – way associative | 8 |

- | | | |
|-------|--|-----|
| 6. a) | What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Describe the solutions to correct data conflicts. | 7 |
| b) | Describe different types of topologies of multiprocessor system. | 8 |
| 7. | Write short notes on: (Any two)
a) BCD Numeric Addition
b) DMA
c) VHDL | 2×5 |

PO KHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Computer Organization and Architecture

Semester: Spring

Year : 2015
 Full Marks: 100
 Pass Marks: 45
 Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | 1. | a) Describe the assembly process for assembly-language programs. How does it differ from the compilation process? | 8 | | | | | | | | | | | | | | | |
|--|---|--------------------------------|-------------|------------------|-----------|-----|----------|---------------------|-----|----------|--------------------------------|------|----------|-----------------------------|------|----------|------------------------|
| b) Differentiate High order interleaving and Low order interleaving. Describe an output device with its interface and load logic for the register. | | 7 | | | | | | | | | | | | | | | |
| 2. | a) Explain modulo- 6 counter. Write down the VHDL code for modulo-6 counter using low level of abstraction. | 8 | | | | | | | | | | | | | | | |
| b) Design a very simple CPU that has 6-bit address register (AR), 6-bit program counter (PC), 8-bit data register (DR) and 2-bit instruction register (IR). The CPU must execute the following instructions: | | 7 | | | | | | | | | | | | | | | |
| <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%;">Instruction</th> <th style="width: 33%;">Instruction Code</th> <th style="width: 33%;">Operation</th> </tr> </thead> <tbody> <tr> <td>COM</td> <td>00XXXXXX</td> <td>$AC \leftarrow AC'$</td> </tr> <tr> <td>AND</td> <td>01AAAAAA</td> <td>$AC \leftarrow ac^A M[AAAAAA]$</td> </tr> <tr> <td>JREL</td> <td>10AAAAAA</td> <td>$PC \leftarrow PC + AAAAAA$</td> </tr> <tr> <td>SKIP</td> <td>11XXXXXX</td> <td>$PC \leftarrow PC + 1$</td> </tr> </tbody> </table> | | | Instruction | Instruction Code | Operation | COM | 00XXXXXX | $AC \leftarrow AC'$ | AND | 01AAAAAA | $AC \leftarrow ac^A M[AAAAAA]$ | JREL | 10AAAAAA | $PC \leftarrow PC + AAAAAA$ | SKIP | 11XXXXXX | $PC \leftarrow PC + 1$ |
| Instruction | Instruction Code | Operation | | | | | | | | | | | | | | | |
| COM | 00XXXXXX | $AC \leftarrow AC'$ | | | | | | | | | | | | | | | |
| AND | 01AAAAAA | $AC \leftarrow ac^A M[AAAAAA]$ | | | | | | | | | | | | | | | |
| JREL | 10AAAAAA | $PC \leftarrow PC + AAAAAA$ | | | | | | | | | | | | | | | |
| SKIP | 11XXXXXX | $PC \leftarrow PC + 1$ | | | | | | | | | | | | | | | |
| 3. | a) Describe Microsequencer design and operations. Differentiate between Microprogrammed control unit and Hardwired control unit. | 7 | | | | | | | | | | | | | | | |
| b) | Perform 7/3 division using unsigned binary division. | 8 | | | | | | | | | | | | | | | |
| 4. | a) What is Numeric format? Explain IEEE 754 floating point. | 7 | | | | | | | | | | | | | | | |
| b) | Differentiate cache memory and virtual memory. Show the conversion of logical address to physical address using segmentation with paging. | 8 | | | | | | | | | | | | | | | |
| 5. | a) Define DMA. Explain DMA transfer modes. | 8 | | | | | | | | | | | | | | | |
| b) | Show how instruction pipelining can improve performance of system. Explain the different instruction pipelining conflicts. | 7 | | | | | | | | | | | | | | | |
| 6. | a) Define Topology .Describe MIMD system topologies. | 7 | | | | | | | | | | | | | | | |
| b) | What are interrupts? Explain UART communication. | 8 | | | | | | | | | | | | | | | |
| 7. | Write short notes on: (Any two) | 2×5 | | | | | | | | | | | | | | | |
| | a) Wallace Tree Multiplier | | | | | | | | | | | | | | | | |
| | b) RS 232 | | | | | | | | | | | | | | | | |
| | c) Register windows | | | | | | | | | | | | | | | | |

POKHARA UNIVERSITY

Level: Bachelor Semester: Fall Year : 2016
 Programme: BE Full Marks: 100
 Course: Computer Organization and Architecture Pass Marks: 45
 Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What is instruction set architecture? List out and describe in brief, the two major factors to be considered while designing ISA. 5
- b) Explain the basic CPU organization in detail. 5
- c) Differentiate high order interleaving and low order interleaving with the design of 16×2 memory subsystem. 5

2. a) Write down the arithmetic and logical operations in RTL form. 5
- b) Design the system for the given RTL using bus: 5

A: $R1 \leftarrow R2$

B: $R2 \leftarrow R3, R4 \leftarrow R3$

C: $R1 \leftarrow R4$

D: $R3 \leftarrow R1$

3. a) For a very simple CPU with the following instruction sets: 8

Instruction	Operation	Instruction code
ADD AAAAAA	$AC \leftarrow AC + M[AAAAAA]$	00AAAAAA
AND AAAAAA	$AC \leftarrow AC \wedge M[AAAAAA]$	01AAAAAA
COM	$AC \leftarrow AC^*$	10XXXXXX
OR AAAAAA	$AC \leftarrow AC \vee M[AAAAAA]$	11AAAAAA

- i. Describe specifications and draw State diagram.
 - ii. Design ALU and Register set.
- b) Design the hardwired control unit for the system mentioned in question 3 a. 7
 - c) Explain the different instruction pipelining hazards. 5

4. a) Differentiate hardwired and microprogrammed control unit. Explain how address of control memory is selected in microprogrammed control unit. 7
- b) Explain Booth algorithm with diagram. Trace the multiplication of (-4) and (-5) using Booth algorithm. 8
5. a) What is Cache? Do you agree that system works without cache? Give suitable reasons to support your answer. 7
- b) Explain different modes of asynchronous data transfer. 8
6. a) What is DMA? Describe the working procedure of DMA with diagram. 7
- b) What is Flynn's Taxonomy? Describe the different systems illustrated by the Flynn's Taxonomy in brief. 8
7. Write short notes on: (Any two) 2×5
 - a) BCD addition
 - b) VHDL
 - c) RISC Vs CISC

POKHARA UNIVERSITY

Level: Bachelor Semester: Spring Year : 2017
 Programme: BE Full Marks: 100
 Course: Computer Organization and Architecture Pass Marks: 45
 Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Describe in brief with an arbitrary illustration, how addressing modes works? 5
- b) A computer has a CPU with 8 bit address bus and 8 bit data bus. The computer uses memory mapped I/O. It has a 32 Bytes of ROM at 10 H; constructed using two 16 Bytes ROM Chips. It also has a 32 Bytes of RAM at 80 H. The system has an input device at F7 H and an output device at F8 H. Show the design for the system including all the required logic. 10
2. a) Perform the circular left shift, circular right shift, linear left shift, arithmetic left shift and arithmetic right shift operations on a register holding the value 10100100. 5
- b) Write a VHDL code for generating the combinational circuit for a function $F(x, y, z) = \sum(1, 3, 4, 6)$. 5
- c) What is Lookup ROM? Show the memory content of a Lookup ROM equivalent to two input OR gate. 5
3. a) There is a Very simple CPU for the given set of Instructions: 8

Instruction	Instruction Code	Micro-operation
ADD	00 AAAAAA	$AC \leftarrow AC + M[AAAAAA]$
SUB	01 AAAAAA	$AC \leftarrow AC - M[AAAAAA]$
SKIP	10 XXXXXX	$PC \leftarrow PC + 1$
DEC2	11 XXXXXX	$AC \leftarrow AC - 2$

Let the instruction width be 8 bits and address is 6 bits. Design the CPU's Register Section, State Diagram and ALU.

- b) Design the hardwired control unit for the CPU described in question 7

3a.

4. a) Design a micro-sequencer control unit which directly generate control signals for the CPU described in question 3 b. 7
- b) Write the RTL code for Shift Add Algorithm. Show the hardware implementation for the RTL Code. 8

OR

- What is Arithmetic Pipelining? Describe in brief with an example. 7
5. a) What is memory hierarchy? Differentiate between different types of cache mapping. 8
 - b) Illustrate with an example how branch and data conflict occurs? List out the solutions to the data conflicts. 8
 6. a) What is DMA? Describe how they work using suitable diagram. 8
 - b) Describe in detail about different types of memory organization used in multiprocessor systems. 7

OR

- What is Flynn's Taxonomy? Describe in brief. Also explain in brief about cache coherence. 2×5
7. Write short notes on: (Any two)
- a) Paging
 - b) Signed and Unsigned number representation
 - c) Interrupts and Handling Interrupts

POKHARA UNIVERSITY

Level: Bachelor

Semester: Fall

Programme: BE

Course: Computer Organization and Architecture

Year : 2018
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Describe about ISA. What are the considerations to be made while ISA design? 5
- b) A computer has a CPU with 8 bit address bus and 16 bit data bus. The computer uses isolated I/O. It has a 64×16 ROM at 00 H; constructed using two 32×16 ROM Chips. It also has a 32×16 of RAM at C0 H. The system has an Input device at 17H and an Output Device at B5H. Show the design for the system including all the required logic 10
2. a) List out the RTL Codes for Arithmetic and Logical Operations. Also show the implementation of addition and subtraction using parallel adder. 5
- b) Write a VHDL code for generating the combinational circuit with three inputs A, B and C and an output F, where $F(A, B, C) = \sum(1, 3, 6, 7)$. 5
- c) Write down the RTL Code for Booth's Algorithm. 5
3. a) There is a Very simple CPU for the given set of Instructions: 8

Instruction	Instruction Code	Operations
STA	00 AAAAAA	$M[AAAAAA] \leftarrow AC$
XNOR	01 AAAAAA	$AC \leftarrow AC \oplus M[AAAAAA]$
JMP	10 AAAAAA	GOTO AAAAAA
SKIP	11 XXXXXX	$PC \leftarrow PC + 1$

Let the instruction width be 8 bits and address is 6 bits. Design the CPU's Register Section, State Diagram and ALU.

- b) Design the hardwired control unit for the CPU described in question 7

3 a.

4. a) Design a microsequencer control unit with horizontal microcode for the CPU described in question 3 b. 8
- b) What is Lookup ROM? Describe in brief demonstrating a Lookup ROM working as XOR Gate. 7
5. a) What is Memory Hierarchy? Describe the Significance of Cache and Virtual Memory. 7
- b) What is Register Windows? In a system, there are 5 windows of registers, each register share 4 input registers, and 4 output registers. Each of the windows has 10 local registers. The system has 20 Global registers. Calculate the total number of registers in the system. Show the pictorial representation as well. 8
6. a) Differentiate between:
 - i. Interrupt driven I/O and Programmed I/O
 - ii. Vectored and Non Vectored Interrupt Hardware
- b) What is paging? What is page table? How is page table used to convert logical address to physical address? Illustrate. 7
7. Write short notes on: (Any two) 2×5
 - a) Multi-byte Data
 - b) BCD Addition
 - c) DMA

POKHARA UNIVERSITY

Level: Bachelor Semester: Spring Year : 2018
 Programme: BE Full Marks: 100
 Course: Computer Organization and Architecture Pass Marks: 45
 Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Describe the different types of addressing modes with illustration. 5
- b) Define enable and load logic. Generate load logic for an output device at CFh. Assume the system being operated in isolated mode. 5
- c) Design an 8x4 ROM chips using 4x4 ROM chips. Illustrate the design using lower order interleaving. 5

2. a) Write a VHDL code to generate a function $F=ABC+A'B'C'$. 5
- b) Define RTL. Write RTL codes for arithmetic operations with circuitry. 5
- c) Trace RTL code of Shift add multiplication algorithm for multiplication of (3) and (4). 5

3. a) There is a very simple CPU for the given set of instructions: 8

Instruction	Instruction Code	Operations
STR	00 AAAAAA	$AC \rightarrow M[AAAAAA]$
NAND	01 AAAAAA	$AC \leftarrow (AC \wedge M[AAAAAA])$
JMP	10 AAAAAA	$PC \leftarrow AAAAAA$
INC2	11 XXXXXX	$AC \leftarrow AC + 2$

Let the instruction width be 8 bits and address is 6 bits. Design the CPU's Register Section, State Diagram and ALU.

- b) Design the hardwired control unit for the CPU described in question number 3 (a). 7

- a) Design a micro-sequencer control unit with horizontal microcode for the CPU described in question number 3 (b). 8

- b) What is Lookup ROM? Illustrate with an example how it works? 7
 - a) What is virtual memory? Differentiate between paging and segmentation. 7
 - b) Describe Register Windows. In a system, there are 8 windows of registers, each register share 8 input registers, and 8 output registers. Each of the windows has 4 local registers. The system has 10 Global registers. Calculate the total number of registers in the system. Show the pictorial representation as well. 8

 - a) What is DMA? Describe how it works. 8
 - b) How are memory organized in multiprocessor systems? Illustrate with suitable diagrams. 7

 7. Write short notes on: (Any two) 2×5
- a) Instruction and data types
 - b) BCD Adder
 - c) Interrupt Vector