POKHARA UNIVERSITY

Level: Bachelor Semester: Spring Year : 2017
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Describe in brief with an arbitrary illustration, how addressing modes works? 5
   b) A computer has a CPU with 8 bit address bus and 8 bit data bus. The computer uses memory mapped I/O. It has a 32 Bytes of ROM at 10 H; constructed using two 16 Bytes ROM Chips. It also has a 32 Bytes of RAM at 80 H. The system has an input device at F7 H and an output device at F8 H. Show the design for the system including all the required logic. 10
2. a) Perform the circular left shift, circular right shift, linear left shift, arithmetic left shift and arithmetic right shift operations on a register holding the value 10100100. 5
   b) Write a VHDL code for generating the combinational circuit for a function $F(x, y, z) = \sum(1,3,4,6)$. 5
   c) What is Lookup ROM? Show the memory content of a Lookup ROM equivalent to two input OR gate. 5
3. a) There is a Very simple CPU for the given set of Instructions: 8

Instruction	Instruction Code	Micro-operation
ADD	00 AAAAAA	AC←AC+M[AAAAAA]
SUB	01 AAAAAA	AC←AC-M[AAAAAA]
SKIP	10 XXXXXX	PC←PC+1
DEC2	11 XXXXXX	AC←AC-2

Let the instruction width be 8 bits and address is 6 bits. Design the CPU's Register Section, State Diagram and ALU.

   b) Design the hardwired control unit for the CPU described in question 3a. 7

4. a) Design a micro-sequencer control unit which directly generate control signals for the CPU described in question 3 b. 7
   b) Write the RTL code for Shift Add Algorithm. Show the hardware implementation for the RTL Code. 8

OR

What is Arithmetic Pipelining? Describe in brief with an example.

5. a) What is memory hierarchy? Differentiate between different types of cache mapping. 7
   b) Illustrate with an example how branch and data conflict occurs? List out the solutions to the data conflicts. 8
6. a) What is DMA? Describe how they work using suitable diagram. 8
   b) Describe in detail about different types of memory organization used in multiprocessor systems. 7

OR

What is Flynn's Taxonomy? Describe in brief. Also explain in brief about cache coherence.

7. Write short notes on: (**Any two**) 2×5
   a) Paging
   b) Signed and Unsigned number representation
   c) Interrupts and Handling Interrupts