## POKHARA UNIVERSITY

: 2018 Semester: Spring Year Level: Bachelor Full Marks: 100 Programme: BE Course: Computer Organization and Architecture Pass Marks: 45 Time . : 3hrs. Candidates are required to give their answers in their own words as far as practicable. The figures in the margin indicate full marks. Attempt all the questions. Describe the different types of addressing modes with illustration. 5 Define enable and load logic. Generate load logic for an output device at CFh. Assume the system being operated in isolated mode. 5 Design an 8x4 ROM chips using 4x4 ROM chips. Illustrate the design using lower order interleaving. 5 Write a VHDL code to generate a function F=ABC+A'B'C'. - 5 Define RTL. Write RTL codes for arithmetic operations with 5 circuitry. Trace RTL code of Shift add multiplication algorithm for 5 multiplication of (3) and (4). There is a very simple CPU for the given set of instructions: 8 **Operations** Instruction Instruction Code AC→M[AAAAAA] 00 AAAAAA STR AC←(AC^M[AAAAAA])` NAND 01 AAAAAA PC AAAAAA 10 AAAAAA **JMP** 11 XXXXXX AC←AC+2 INC<sub>2</sub> Let the instruction width be 8 bits and address is 6 bits. Design the CPU's Register Section, State Diagram and ALU. b) Design the hardwired control unit for the CPU described in question number 3 (a). Design a micro-sequencer control unit with horizontal microcode for

	b)	What is Lookup ROM? Illustrate with an example how it works?	7
5.	a)	What is virtual memory? Differentiate between paging and segmentation.	7
	b)	Describe Register Windows. In a system, there are 8 windows of registers, each register share 8 input registers, and 8 output registers. Each of the windows has 4 local registers. The system has 10 Global registers. Calculate the total number of registers in the system. Show the pictorial representation as well.	8
6.	a)	What is DMA? Describe how it works.	8
	b)	How are memory organized in multiprocessor systems? Illustrate with suitable diagrams.	7
7.	Write short notes on: (Any two)		2×5
	a)	Instruction and data types	
	b)	BCD Adder	
	c)	Interrupt Vector	
	:		

the CPU described in question number 3 (b).