POKHARA UNIVERSITY

Level: Bachelor | Semester – Fall | Year : 2011
Programme: BE | Full Marks: 100
Course: Computer Organization and Architecture | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What is system bus? Explain in details. 7

   b) Define ISA. Explain different addressing modes. 8

2. a) Define VHDL. Write the VHDL program for full adder. 7

   b) How a 16×2 memory sub system can be constructed from two 8×2 ROM chip with low order interleaving and high order interleaving. Explain with diagram. 8

OR

   a) What is RTL? Write the RTL for different arithmetic operations. Design a 4-bit decimal right shifting circuit. 7

   b) What is instruction cycle? Explain instruction cycle state diagram. 8

3. Design a CPU that meets the following specification: 15

   a) It can access 64 bytes of memory each 8 bit wide. The CPU does this by outputting a 6 bit address on its output pin A{5...0] and reading 8-bit value from memory on its inputs D[7...0].

   b) The CPU contains 6-bit AR, 6-bit PC, 8-bit Dr and 2-bit IR.

   c) The CPU realize following instruction:

Instruction	Instruction Code	Operation
SUB	00AAAAAA	AC = AC-M[AAAAAA]
AND	01AAAAAA	AC = AC^M[AAAAAA]
JMP	10AAAAAA	GOTO AAAAAA
INC	11XXXXXX	AC = AC + 1

i. Write the RTL for fetch and execute cycle and draw its register section for CPU.

ii. Design a hardwired control unit for above CPU.

4. a) Differentiate a hardwired control unit with micro-programmed control unit. 7

b) Write the RTL code for Booth's algorithm. Using same code trace the multiplication of (-5) and (3). 8

5. a) What is hierarchical memory system? Explain any one of the cache mapping technique? 7

b) What do you mean by destination initiated data transfer without handshaking? Illustrate with timing and implementation of an example. 8

6. a) Explain different types of conflict in instruction pipeline with example. 8

b) Describe different types of topologies of multiprocessor system. 7

OR

a) What is parallelism? How can it be achieved in uniprocessor systems? 7

b) Show the layout of the cache for a CPU that can address 1M×16 of memory; the cache holds 8k×16 of data and has the following mapping strategies: give the number of bits per location and total number of locations 8

i. Fully Associative

ii. Direct Mapped

iii. Two- way associative

7. Write short notes on **any two:** 2×5

a) DMA

b) RISC versus CISC

c) Virtual Memory