POKHARA UNIVERSITY

Level: Bachelor Semester – Spring Year:2020

Program: BE Full Marks: 70

Course: Computer Organization and Architecture Pass Marks: 31.5

Time: 2 hrs.

Candidates are required to answer in their own words as far as practicable. The figures in the margin indicate full marks.

Attempt all the questions.

Section - A: $(5 \times 10 = 50)$

Explain different types of addressing modes used in computer system, along with 10 their usages and application OR Write VHDL code for designing a full adder using half adder in structural model. 10 Q. N. 2 Design 16x4 memory sub-system constructed from 16x2 ROM chips with both 10 low-level and high-level interleaving. Perform -7x-2 using booth's algorithm, Can booths algorithms be used if both Q. N. 3 8+2numbers are positive, if yes how? Q. N. 4 What is cache memory? Explain associative, set associative and direct mapping in 2+8cache. What is instruction pipelining? Explain the data conflicts and branch conflicts Q. N. 5 2+8along with is remedies.

Section - B: $(1\times20=20)$

Q. N. 6 a) For a very simple CPU, has the following instruction set. Show the State diagram, Register Section, ALU design.

| Operation | Instruction Code | Instruction |
|-----------------|------------------|-------------|
| M[AAAAAA] <- AC | 00AAAAAA | STA |
| AC<- M[AAAAAA] | 01AAAAAA | LDA |
| AC<- AC+2 | 10XXXXXX | INC |
| AC<- AC' | 11 XXXXXX | COM |

b) Why do we need input output modules? Compare programmed I/O, interrupt driven data transfer and Direct memory Access(DMA)