POKHARA UNIVERSITY

Level: Bachelor | Semester: Fall | Year : 2021
Programme: BE | Full Marks: 100
Course: Computer Organization and Architecture | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define ISA. Describe the considerations to be made while designing ISA. 8
   b) Explain instruction cycle for read and write operations using their timing diagram. 7
2. a) Write a VHDL code to generate a function F=ABC+A'B'C'. 5
   b) Define RTL. Write RTL code for arithmetic operations with circuitry. 5
   c) Trace RTL code of Shift add multiplication algorithm for multiplication of (3) and (4). 5
3. a) There is a very simple CPU for the given set of Instructions: 8

Instruction	Instruction Code	Operations
OR	00 AAAAAA	AC←AC^{V}M[AAAAAA]
AND	01 AAAAAA	AC←AC^M[AAAAAA]
CMP	10 AAAAAA	AC←AC`
LDA	11 XXXXXX	AC←M[AAAAAA]

   Let the instruction width be 8 bits and address is 6 bits. Design the CPU's Register Section; State Diagram and ALU.
   b) Design the hardwired control unit for the CPU described in question 3 a. 7
4. a) Design a micro-sequencer control unit with horizontal microcode for the CPU described in question 3b. 8
   b) Write RTL code for Booth's Algorithm. Design its circuit. 7

5. a) What is virtual memory? Differentiate between paging and segmentation. 7
   b) Describe Register Windows. In a system, there are 8 windows of registers, each register share 8 input registers, and 8 output registers. Each of the windows has 4 local registers. The system has 10 Global registers. Calculate the total number of registers in the system. Show the pictorial representation as well. 8
6. a) What is DMA? Describe how it works. 8
   b) What is cache coherence? Describe how cache coherence can be dealt with? List them. 7
7. Write short notes on: (**Any two**) 2×5
   a) Instruction and data types
   b) USB
   c) Interrupt Vector