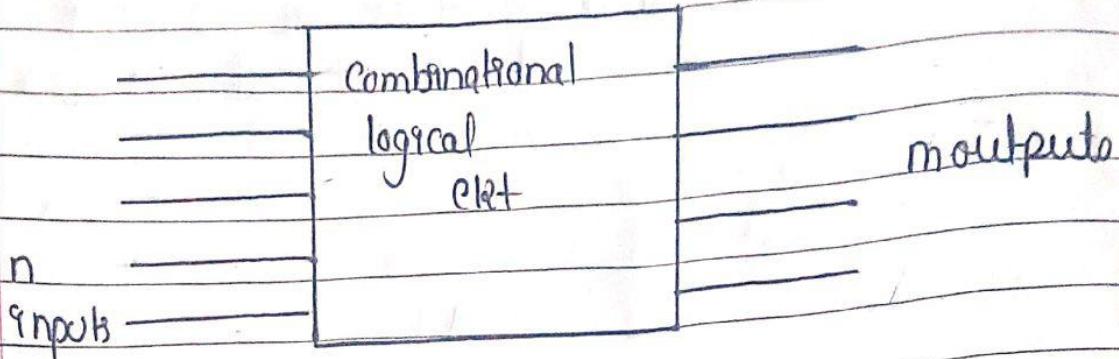


Combinational logicCombinational logic

- It consists of 'n' no of inputs and 'm' no of outputs.
- At any time o/p value solely depends upon the inputs.

# Design Procedure

1) Question is given to you.

2) From que you should find the number of inputs 'n' and no of outputs 'm'.

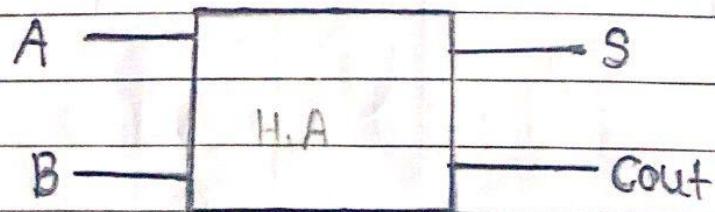
3) Draw the truth table.

4) Simplify the outputs using k-Map.

5) Draw the logic diagram.

# 1) Adder1) Half adder

It is combination circuit that is designed to add '2' bit only.



Truth table

A 1/p	B 1/p	S 1/p	Cout (carry) 1/p
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

K-map for sum term (S)

A 1/p	B 1/p	0	1
0	1	1	1
1	1	0	1

A 1/p	B 1/p	0	1
0	1	0	1
1	1	1	1

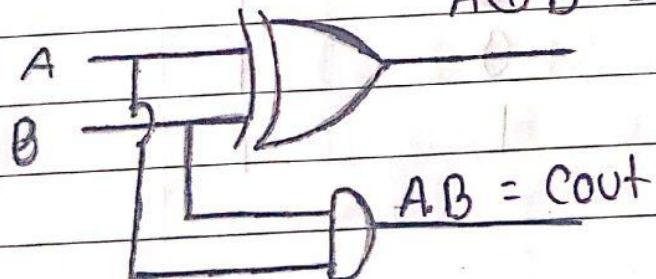
$$S = A \oplus B$$

$$= AB + BA$$

$$Cout = A * B$$

Realization of Combination logic

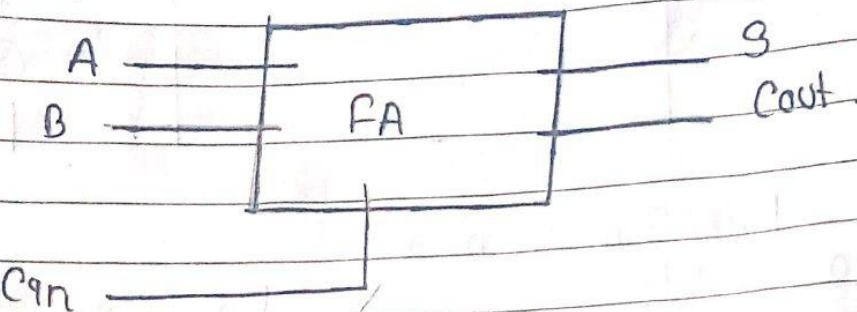
$$A \oplus B = S$$



Q27

### Full adder:

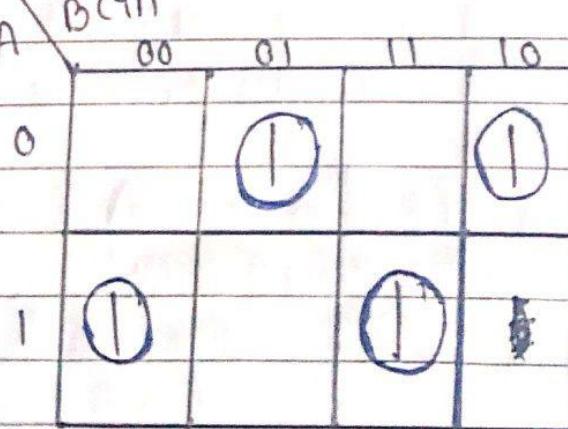
Full adder is a combinational ckt that is used to add 3 bit.



Truth table:

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

kmap  
For S



$$S = A\bar{B}\bar{Cin} + \bar{A}B\bar{Cin} + AB\bar{Cin} + \bar{A}B\bar{Cin}$$

$$\begin{aligned}
 &= A(\overline{B}C\bar{n} + B\bar{c}n) + \overline{A}(B\bar{c}n + \bar{C}\bar{n}B) \\
 &= AC\overline{B+C\bar{n}} + \overline{A}B\overline{C+C\bar{n}} \\
 &= A\oplus C(B\oplus C\bar{n})
 \end{aligned}$$

classmate

Data  
Page

3

for Cout

	$B\bar{c}n$	00	01	11	10
A	0			1	
1			1	0	1

$$Cout = AC\bar{n} + AB + B\bar{c}n$$

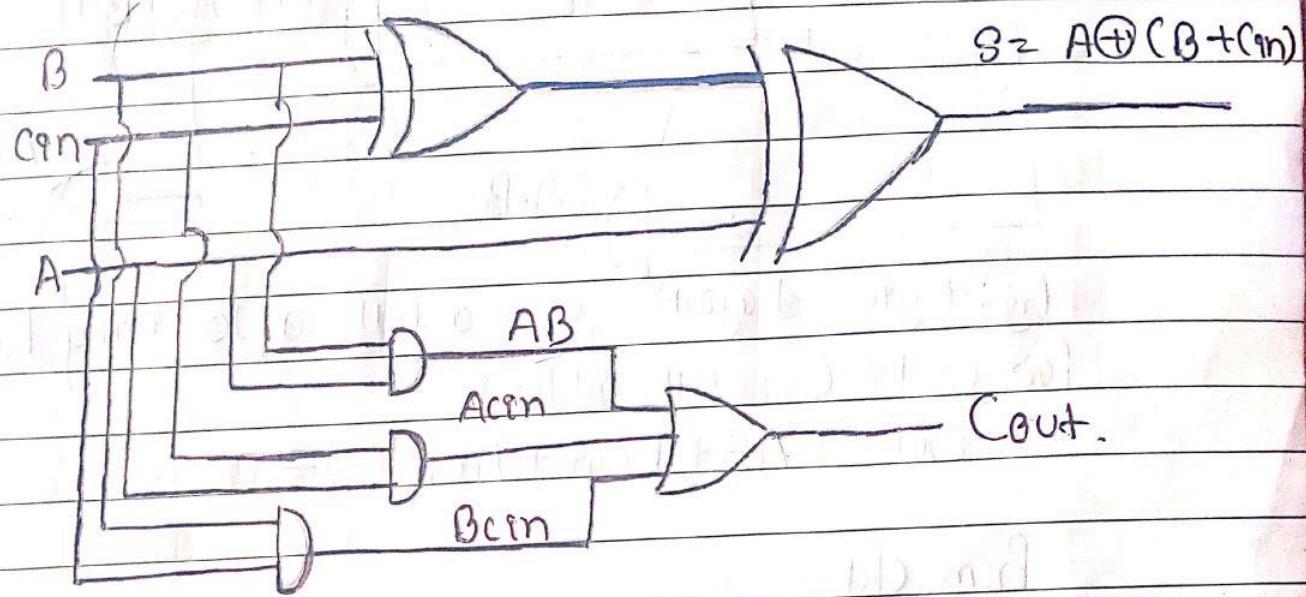


Fig: logic Diagram.

# Construct a full adder using two half adders.

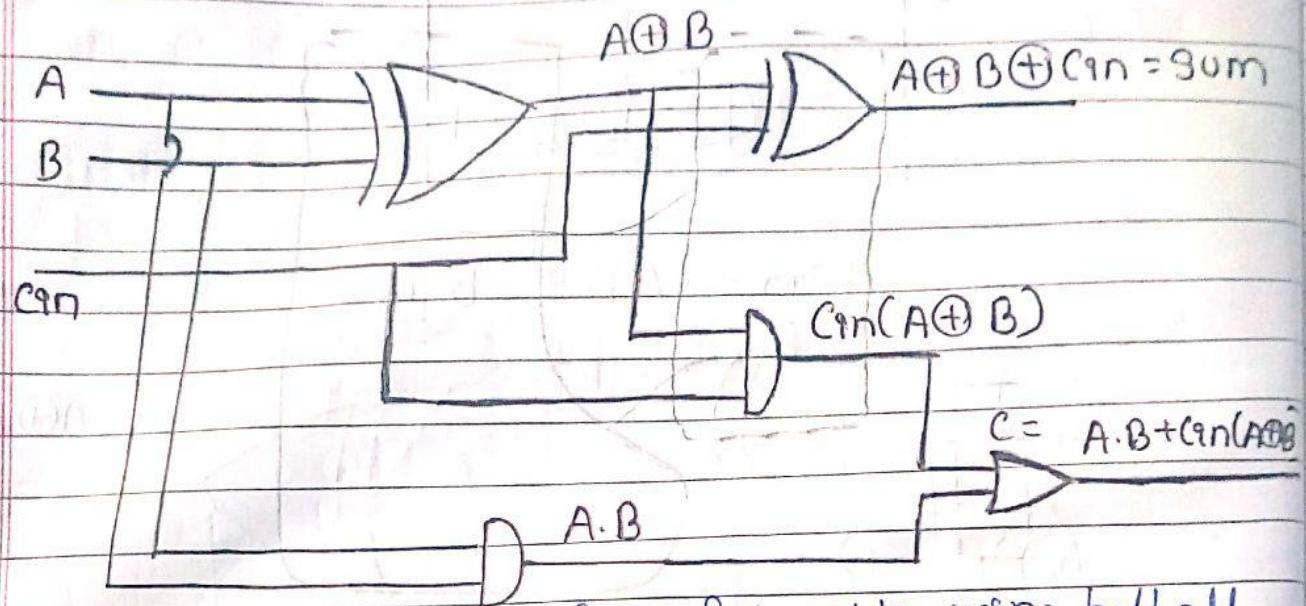


fig: logic diagram of a full adder using half adder  
for cout (for full adder)  
 $Cout = AB + BCin + ACin$  —①

From ckt,

$$Cout = A \cdot B + Cin(A \oplus B)$$

$$= AB + Cin(AB + \bar{A}B)$$

$$= AB + A\bar{B}Cin + \bar{A}Bcin$$

From ①,

$$Cout = AB + BCin(A + \bar{A}) + ACin(B + \bar{B})$$

$$= AB + ABcin + \bar{A}Bcin + ABcin + \bar{A}\bar{B}cin$$

$$= AB(1 + Cin) + A\bar{B}cin + \bar{A}Bcin$$

$$= AB + A\bar{B}cin + \bar{A}Bcin$$

Hence verified

## Subtractor

It is a combination of logic used to subtract two gates.

It is of two types;

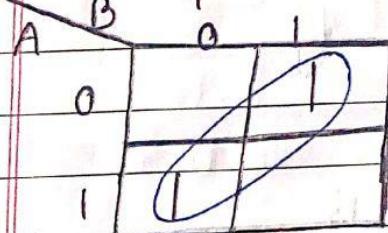
### Half ~~adder~~ Subtractor

It subtracts two bits.

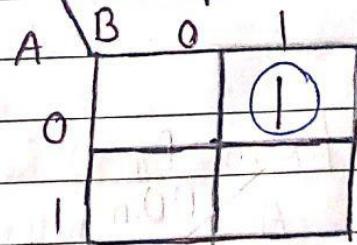
## Truth table

A	B	D	b	D = Difference b = borrow.
0	0	0	0	
0	1	1	1	
1	0	1	0	
1	1	0	0	

K-map for D



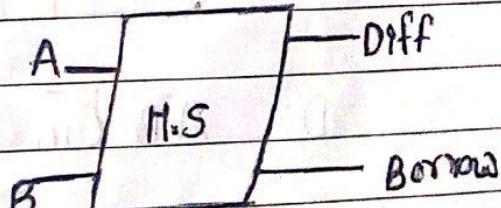
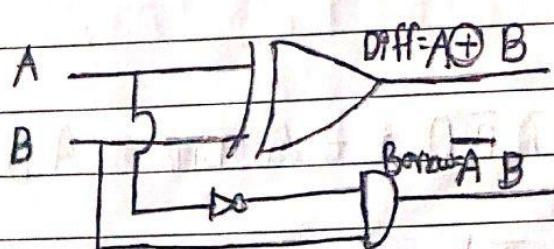
K-map for b



$$D = A\bar{B} + \bar{A}B$$

$$= A \oplus B$$

$$b = \bar{A}B$$



Half Subtractor

## 2) Full Subtractor

It subtracts 3 bits.

$$\text{no of } q/p = 3$$

$$\text{no of } o/p = 2$$

Truth table

A	B	$b_{in}$	D	$b_{out}$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Kmap for D

A'       $b_{in}$

	00	01	11	10
0		(1)		(1)
1	(1)		(1)	

$$D = A\bar{B}\bar{b}_{in} + \bar{A}\bar{B}b_{in} + AB\bar{b}_{in} + \bar{A}Bb_{in}$$

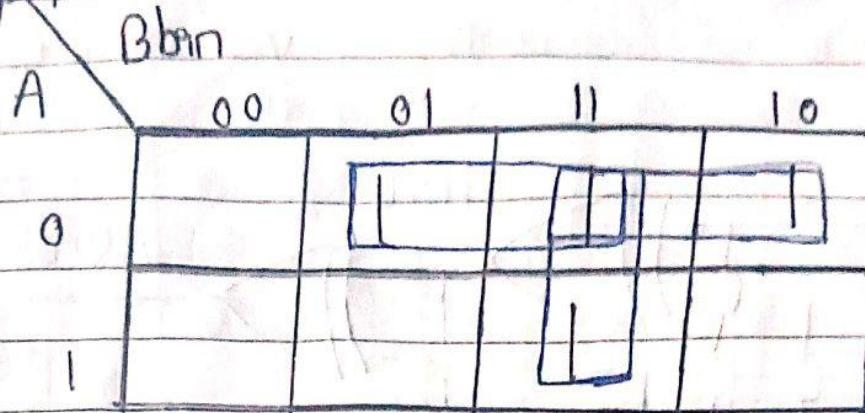
$$= \bar{B}(A\bar{b}_{in} + \bar{A}b_{in}) + B(A\bar{b}_{in} + \bar{A}b_{in})$$

$$= \bar{B}(A \oplus b_{in}) + B(\bar{A} \oplus b_{in})$$

$$= \bar{B} \oplus (A + b_{in})$$

$$= A \oplus B \oplus b_{in}$$

k-map for bout



$$\text{bout} = \overline{A} \text{ bin} + B \text{ bin} + \overline{A} B$$

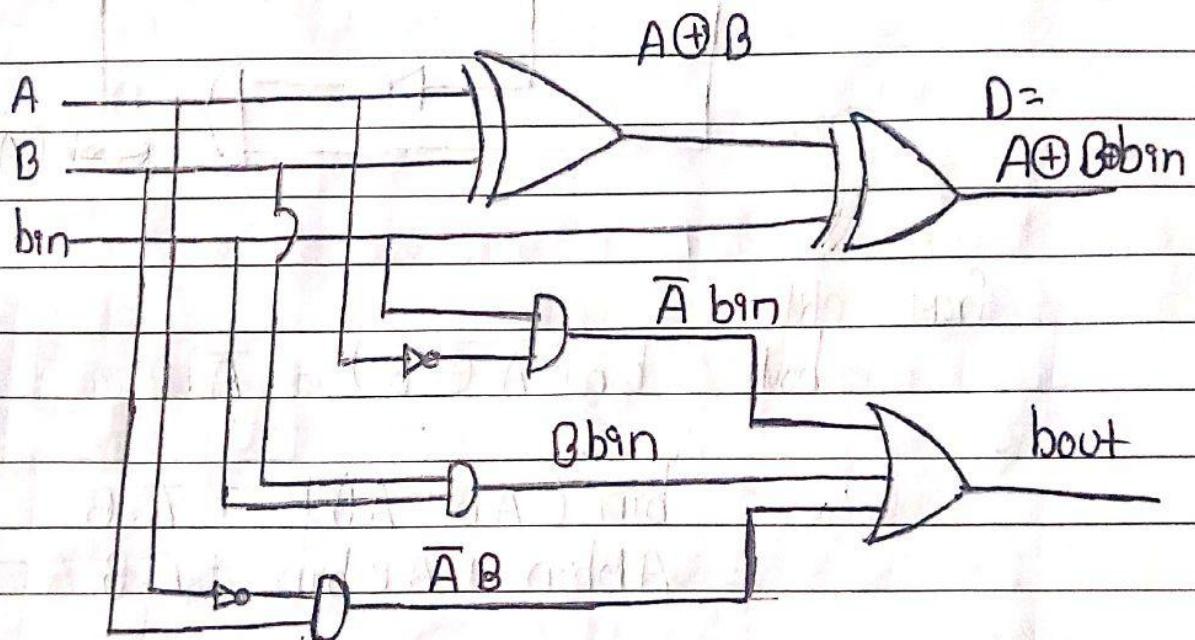
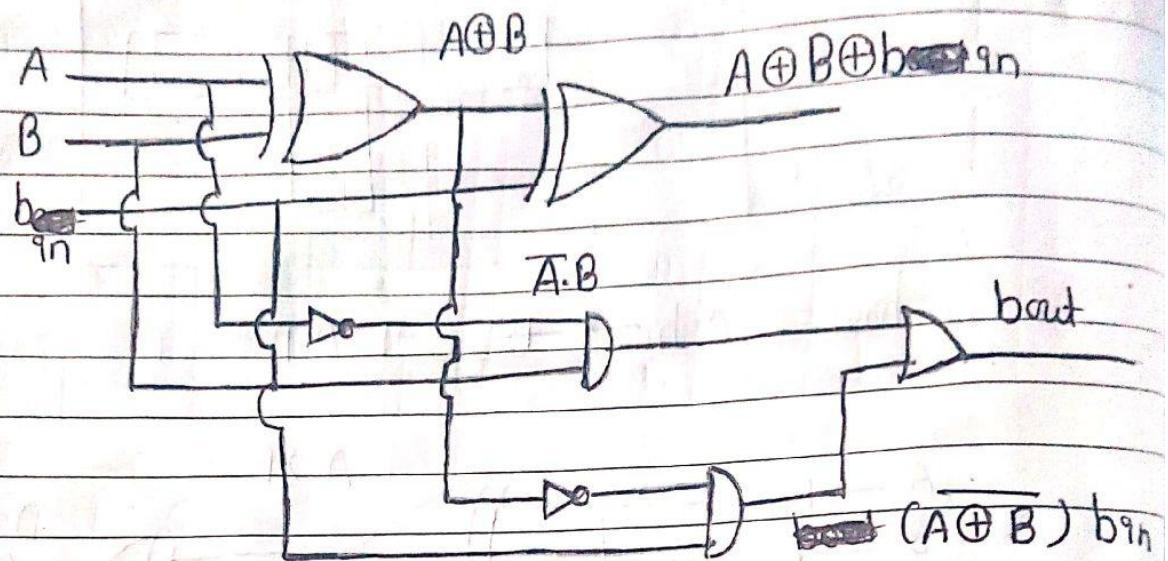


fig: logic Diagram

# Draw a full subtractor using two half subtractor & verify your answer.



From class

$$b_{out} = b_{in}(\overline{A} \oplus \overline{B}) + \overline{A} \cdot B$$

$$= b_{in}(AB + \overline{A}\overline{B}) + \overline{A} \cdot B$$

$$= ABb_{in} + \overline{A}\overline{B}b_{in} + \overline{A} \cdot B$$

— ①

We have,

$$b_{out} = \overline{A}b_{in} + Bb_{in} + \overline{A}\overline{B}$$

$$= \overline{A}b_{in}(B + \overline{B}) + Bb_{in}(A + \overline{A}) + \overline{A}\overline{B}$$

$$= \overline{A}b_{in}B + \overline{A}\overline{B}b_{in} + ABb_{in} + \overline{A}\overline{B}b_{in} + \overline{A}\overline{B}$$

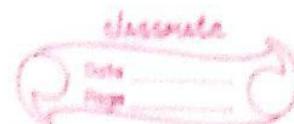
$$= \overline{A}\overline{B} + ABb_{in} + \overline{A}\overline{B}b_{in} + \overline{A}\overline{B}b_{in}$$

$$= \overline{A}\overline{B}(1 + b_{in}) + ABb_{in} + \overline{A}\overline{B}b_{in}$$

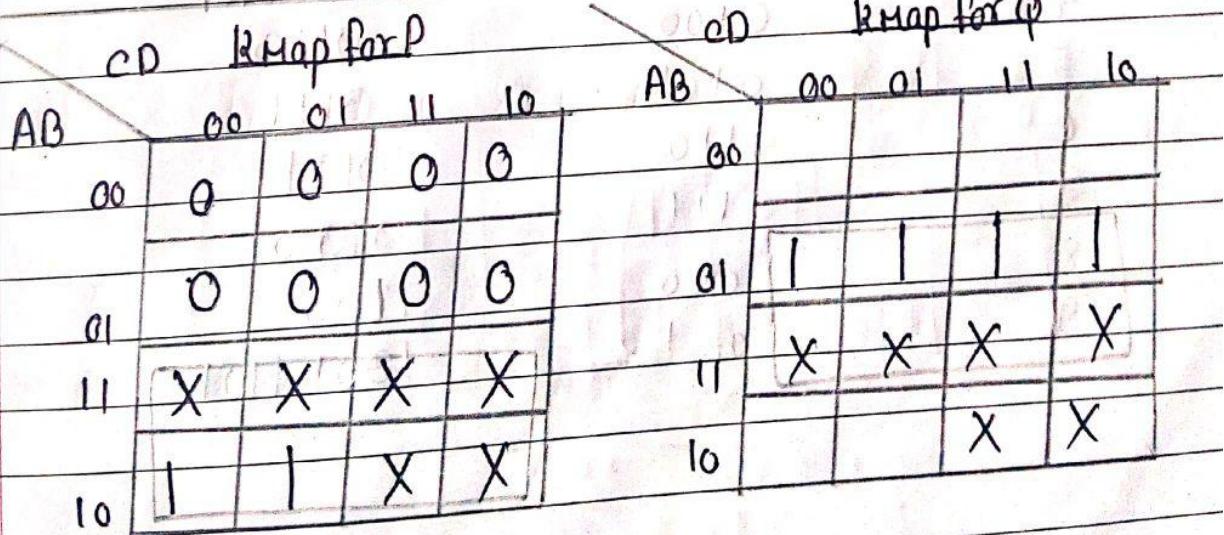
$$= \overline{A}\overline{B} + ABb_{in} + \overline{A}\overline{B}b_{in}$$

## Code Conversion:

17 Decimal to BCD to binary.



Decimal	Binary	BCD
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	C000
9	1001	1001
10	XXXX	XXXX
11	XXXX	XXXX
12	XXXX	XXXX
13	XXXX	XXXX
14	XXXX	XXXX
15	XXXX	XXXX



P = A

Q = B.

K-map for 'R'

AB	CD			
	00	01	11	10
00		1	1	
01	.	1	1	
11	X	X	X	X
10		X	X	

K-map for S

AB	CD			
	00	01	11	10
00		1	1	0
01	.	1	1	
11	X	X	X	X
10		1	X	X

$$R = C$$

$$S = D$$

27

Decimal or BCD to gray code:

Decimal	BCD	graycode
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0100
4	0100	0110
5	0101	0111
6	0110	1010
7	0111	1011
8	1000	1100
9	1001	1101

K-map for A

	xy	zw	00	01	11	10
00						
01						
11	X	X	X	X		
10	1	1	X	X		

$$A = \overline{xy} \cdot \overline{z} \cdot \overline{w}$$

K-map for B

	xy	zw	00	01	11	10
00						
01	I	I	I	I		
11	X	X	X	X		
10	1	1	X	X		

$$B = x + y$$

	xy	zw	00	01	11	10
00						
01	I	I				
11	X	X	X	X		
10			X	X		

K-map for C

	xy	zw	00	01	11	10
00						
01	I	I	I	I		
11	X	X	X	X		
10	1	1	X	X		

$$C = y\bar{z} + \bar{y}z$$

$$= y \oplus z$$

$$D = \bar{z}w + z\bar{w}$$

$$= z \oplus w$$

7 Octal to BCD  
Octal      binary  
A B C

0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

BCD	P Q R S
	0 0 0 0
	0 0 0 1
	0 0 1 0
	0 0 1 1
	0 1 0 0
	0 1 0 1
	0 1 1 0
	0 1 1 1

K-map for 'Q'

K-map for 'P'

A	BC	00	01	11	10
0		0	0	0	0
1		0	0	0	0

BC

A	BC	00	01	11	10
0		0	0	D	D
1		1	1	1	1

$$P = 1$$

$$Q = A$$

K-map for R

A	BC	00	01	11	10
0				1	1
1				1	1

$$R = B$$

K-map for S

A	BC	00	01	11	10
0		1	1		
1		1	1		

$$S = C$$

(1) Convert BCD to excess-3

	BCD				excess-3			
	A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	1	0	0	0
5	0	1	0	1	1	0	0	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	1	0
8	0	1	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

K-map for P

AB	CD	00	01	11	10
00					
01		1	1	1	1
11	X	X	X	X	
10	1	1	X	X	

K-map for Q

AB	CD	00	01	11	10
00					
01		1			
11	X		X	X	X
10		1	X	X	X

$$P = A + BD + BC$$

$$Q = \overline{BD} + \overline{BC}C + B\overline{C}\overline{D}$$

## # Parity generator and checker

classmate

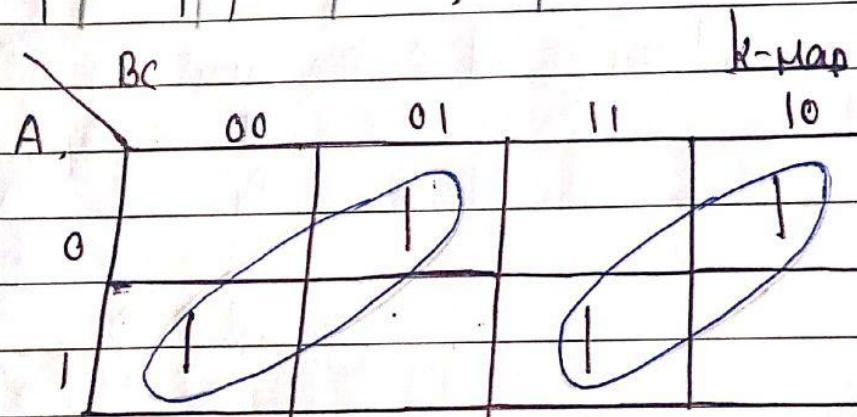
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### # 3 bit generator & 3 bit checker

(#) For even parity

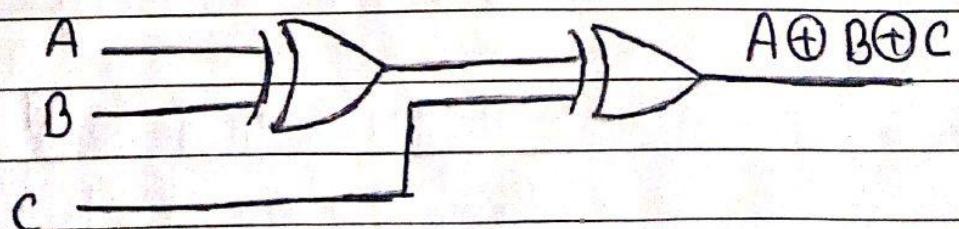
3 bit generator

A	B	C	EP
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



$$P = A \oplus B \oplus C$$

logic circuit

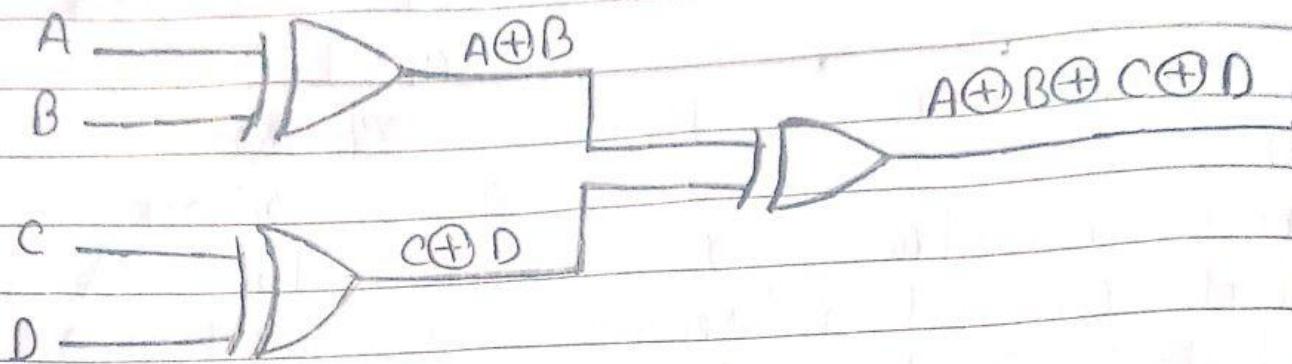


## 4 bit even parity checker

	A	B	C	D	checker (ch)
0)	0	0	0	0	0
1)	0	0	0	1	1
2)	0	0	1	0	1
3)	0	0	1	1	0
4)	0	1	0	0	1
5)	0	1	0	1	0
6)	0	1	1	0	0
7)	0	1	1	1	1
8)	1	0	0	0	1
9)	1	0	0	1	0
10)	1	0	1	0	1
11)	1	0	1	1	1
12)	1	1	0	0	0
13)	1	1	0	1	1
14)	1	1	1	0	1
15)	1	1	1	1	0

AB \ CD	00	01	11	10
00				
01				
11				
10				

$$ch = A \oplus B \oplus C \oplus D$$



If output  $p$  is equal to 1, the receiver will know that the bits are changed during transmission i.e. bits are in error if  $p=1$ .  
 If 'p' is connected to the parity checker clk becomes parity generator.

2(b) Design a circuit of a 3-bit parity generator and the circuit of 4-bit parity checker for odd parity.

Ans For odd parity

3-bit parity generator

A	B	C	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

		BC	00	01	11	10
		A	0	1	0	1
		0	1	0	1	0
		1	0	1	0	1

$$\begin{aligned}
 P &= \boxed{A \oplus B \oplus C} = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C} \\
 &= \bar{A}(\bar{B}\bar{C} + BC) + A(\bar{B}C + B\bar{C}) \\
 &= \bar{A}(B \oplus C) + A(B \oplus C) \\
 &= \overline{A \oplus (B \oplus C)} = A \oplus (B \oplus C)
 \end{aligned}$$

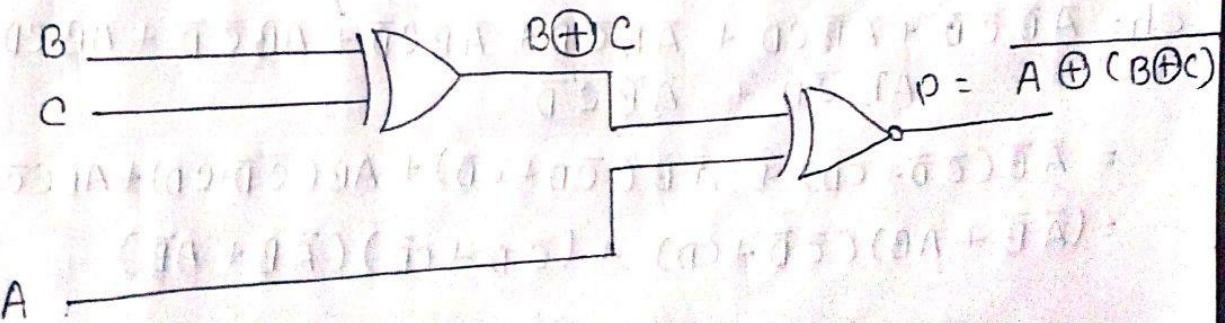


fig: 3-bit parity generator.

## 4-bit odd parity checker

A	B	C	D	ch
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

AB	CD	00	01	11	10
00	1	0	1	0	
01	0	1	0	1	
11	1	0	1	0	
10	0	1	0	1	

$$ch = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + \overline{ABC}\overline{D} + \overline{ABC}\overline{D} + A\overline{B}\overline{C}\overline{D} + A\overline{B}CD + \\ A\overline{B}\overline{C}D + A\overline{B}C\overline{D}$$

$$= \overline{A}\overline{B}(\overline{C}\overline{D} + CD) + \overline{ABC}(\overline{C}\overline{D} + C\overline{D}) + ABC(\overline{C}\overline{D} + C\overline{D}) + A\overline{B}C(\overline{C}\overline{D} + C\overline{D}) \\ = (\overline{A}\overline{B} + AB)(\overline{C}\overline{D} + CD) + (\overline{C}\overline{D} + C\overline{D})(\overline{A}\overline{B} + AB)$$

$$(\overline{A \oplus B})(\overline{C \oplus D}) + (A \oplus B)(C \oplus D)$$

$$\frac{(A \oplus B) \odot (C \oplus D)}{(A \oplus B) \oplus (C \oplus D)}$$

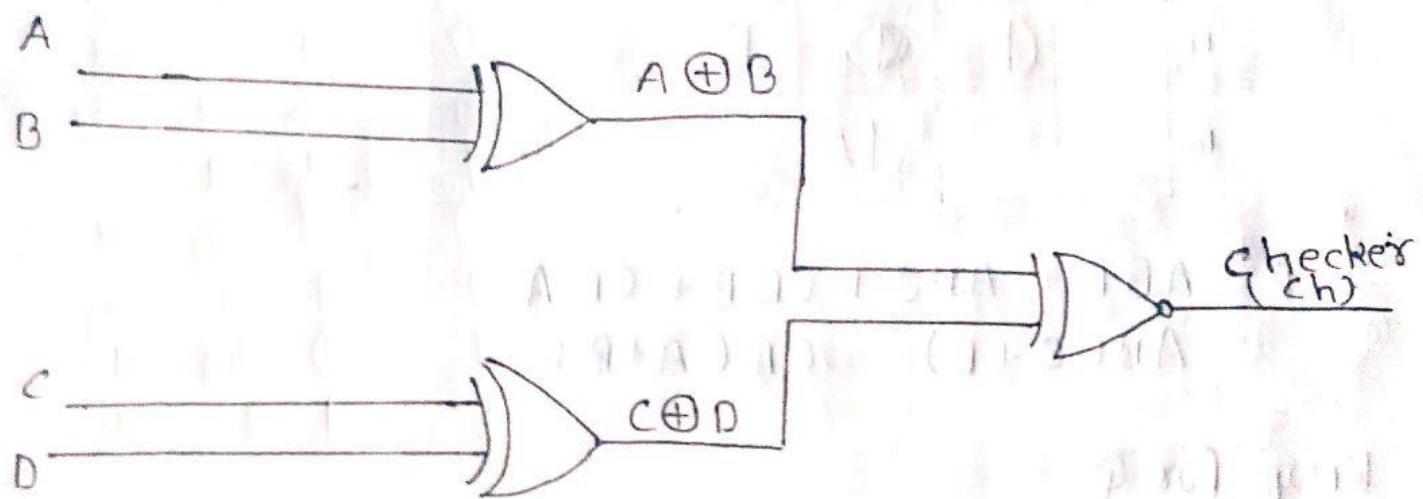


fig: circuit diagram of 4-bit odd parity checker