Chapter 9

Arithmetic and Logic Unit

Arithmeic and Logic Unit

- Deals with the calculation and processing.
- Consists of 2 parts.

1. Arithmetic Unit:

   -deals with the arithmetic operations of i/ps.

2. Logic Unit:

   -deals with the logical operations of i/ps.

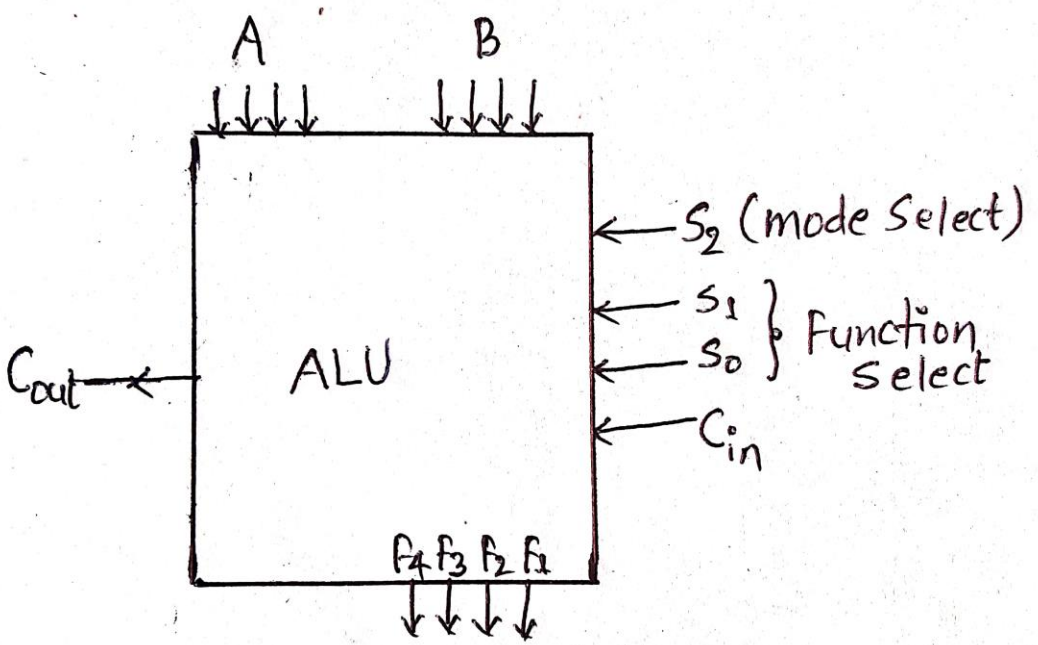
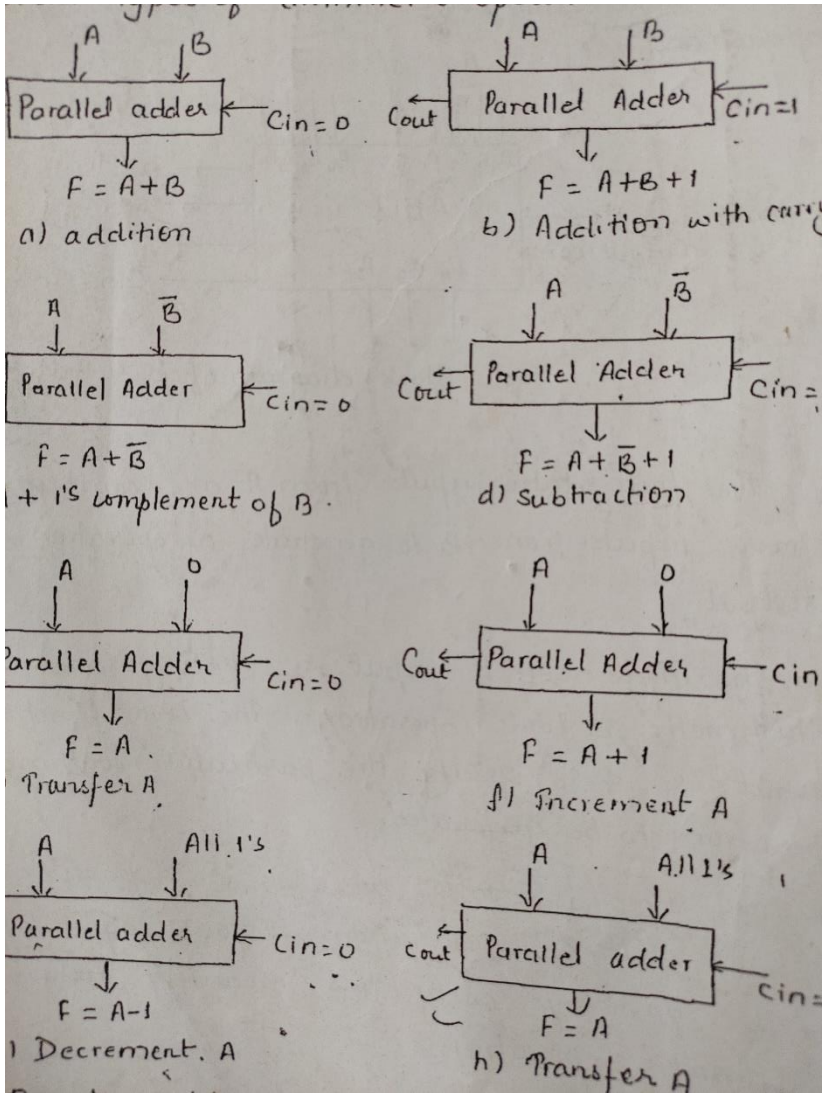


Fig: Block diagram of ALU

Eight different arithmetic operations

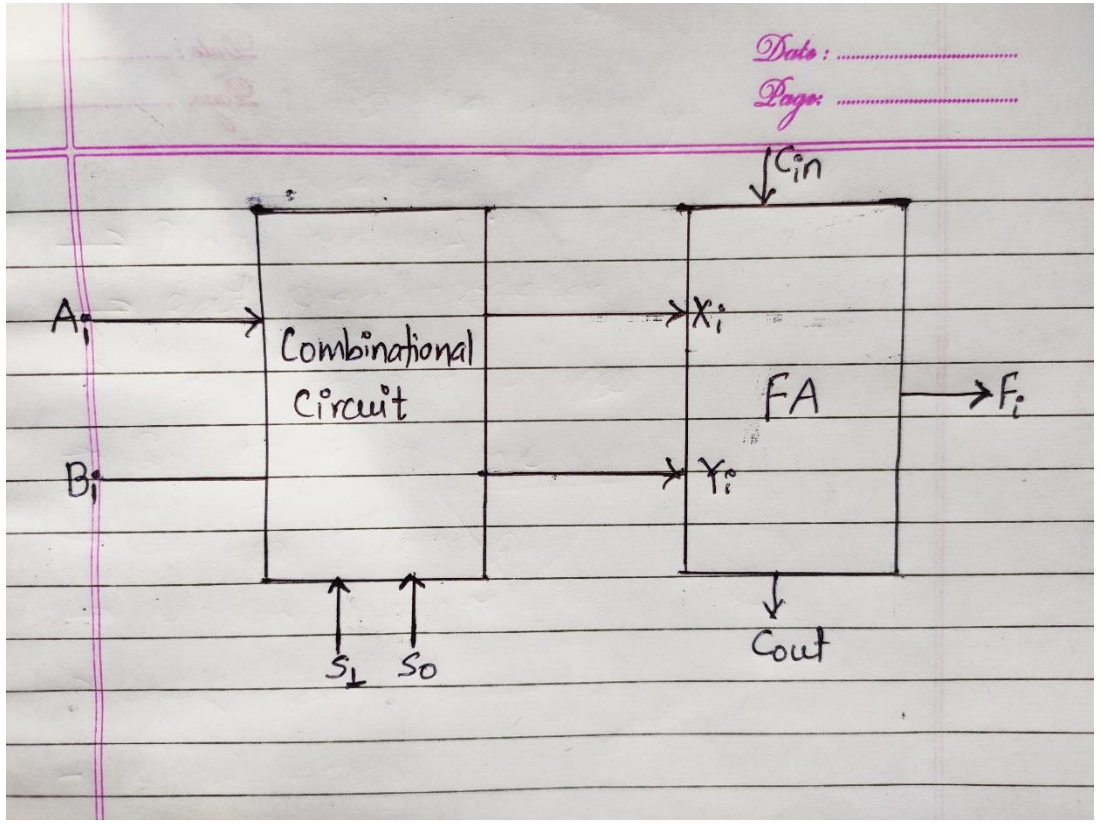
- The different operations are:

F=A+B	F=A+B+1
F=A+B‘	F=A+B‘+1
F=A+0’s	F=A+0’s+1
F=A+1’s	F=A+1’s+1
=A-1	=A



Design of Arithmetic Circuit

- The block diagram of arithmetic circuit is as shown in figure along side.
- Its design include the design of combinational circuit before the parallel adder.
- The design starts with the specification or function table given.



Function table;

Function table:

S_1	S_0	C_{in}	F_i
0	0	0	A_i $\Rightarrow A_i$ + all 0's
0	0	1	A_i+1 $\Rightarrow A_i$ + all 0's + 1
0	1	0	A_i+B_i
0	1	1	A_i+B_i+1
1	0	0	$A_i+\overline{B}_i$
1	0	1	$A_i+\overline{B}_i+1$ $\Rightarrow A_i-B_i$
1	1	0	A + all 1's $\Rightarrow A_i-1$
1	1	1	A + all 1's + 1 $\Rightarrow A_i$

Truthtable of the combinational logic:

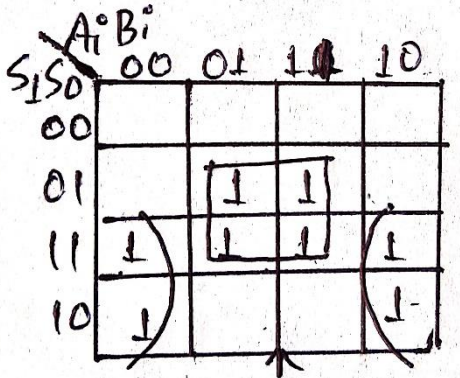
Truthtable of the combinational circuit

S_1	S_0	A_i	B_i	X_i	Y_i	Remarks
0	0	0	0	0	0	A_i + 0's
0	0	0	1	0	0	
0	0	1	0	1	0	
0	0	1	1	1	0	
0	1	0	0	0	0	A_i + B_i
0	1	0	1	0	1	
0	1	1	0	1	0	
0	1	1	1	1	1	
1	0	0	0	0	1	A_i + $\overline{B_i}$
1	0	0	1	0	0	
1	0	1	0	1	1	
1	0	1	1	1	0	
1	1	0	0	0	1	A_i + 1's
1	1	0	1	0	1	
1	1	1	0	1	1	
1	1	1	1	1	1	

Using K-map,

$X_i = A_i$

For Y_i,



$Y_i = S_1\overline{B_i} + S_0B_i$

Circuit diagram of the 4 bit arithmetic circuit:

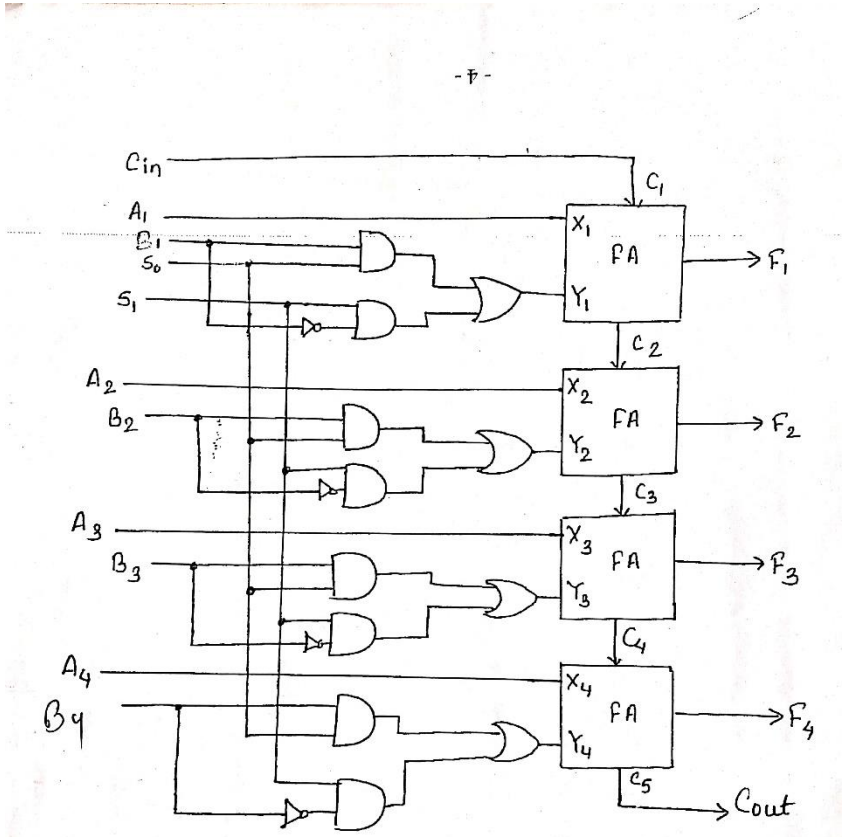


Fig: logic diagram of arithmetic circuit

$X_i = A_i$

$Y_i = B_i S_0 + B_i' S_1 \quad i = 1, 2, \ldots, n$

Design of Logic Unit:

- Select variables:

  S2 -> mode select

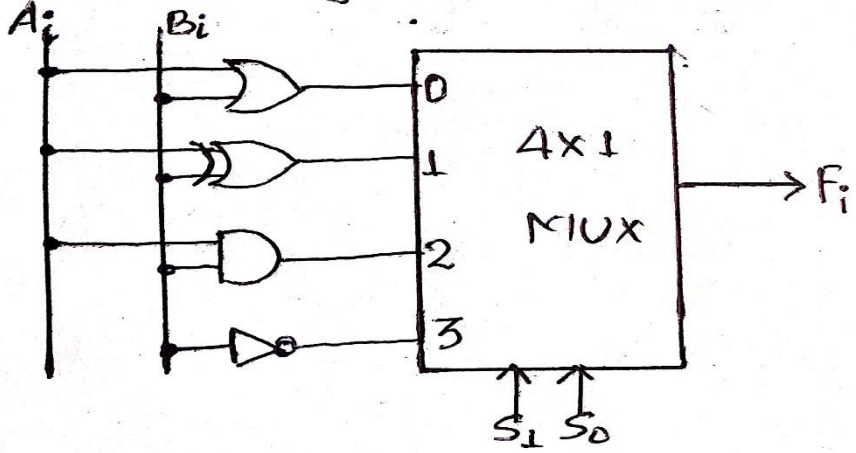
  S1,S0 -> function select
- Let the logical operations be:

  OR,XOR,AND,NOT
- For design, lets take a 4×1 MUX.

Function table:

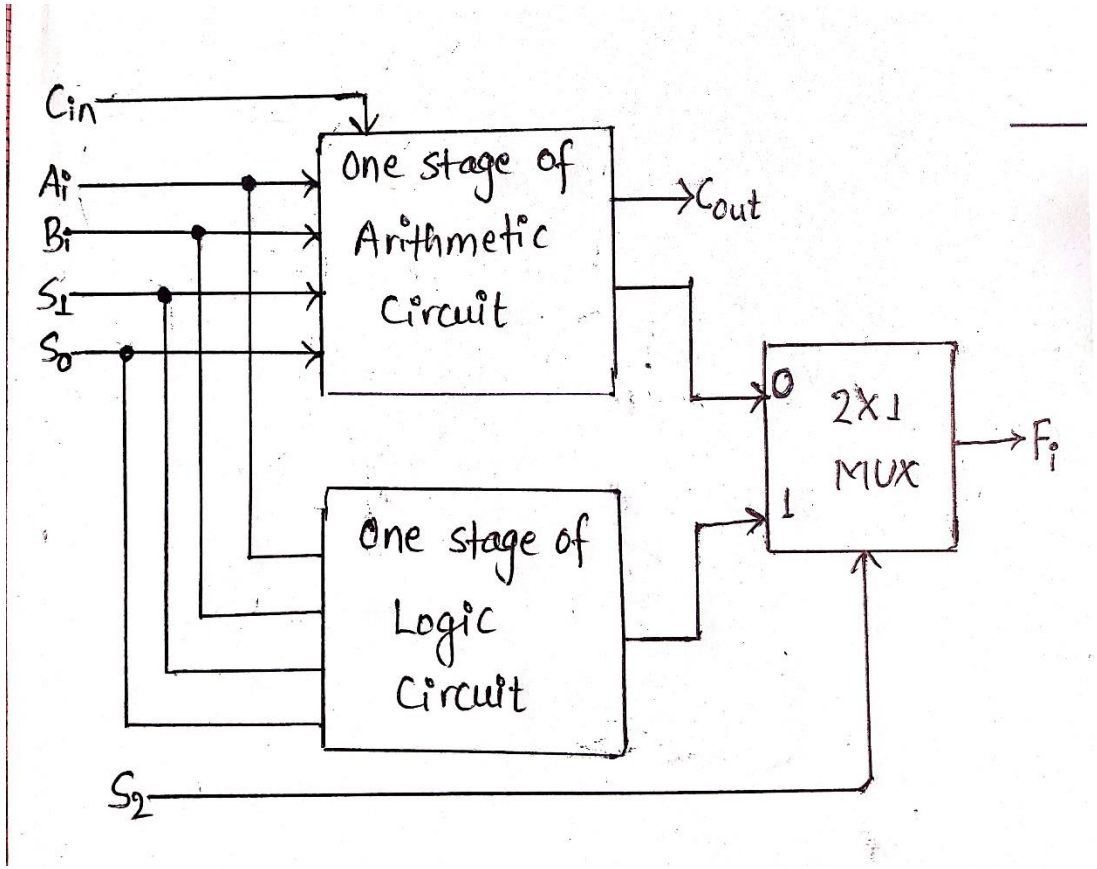
S_1	S_0	Function	operation
0	0	$A_i + B_i$	OR
0	1	$A_i \oplus B_i$	XOR
1	0	$A_i \cdot B_i$	AND
1	1	$\overline{B_i}$	NOT

Circuit diagram:



Single stage ALU:

- Now combining both arithmetic and logic units we can draw or design ALU.
- The single stage ALU is as shown along side.



Design of Shifter:

- Transfers the o/p of ALU to the bus.
- It is a shift register with parallel load.
- The circuit diagram and the function table is as shown in the figure.

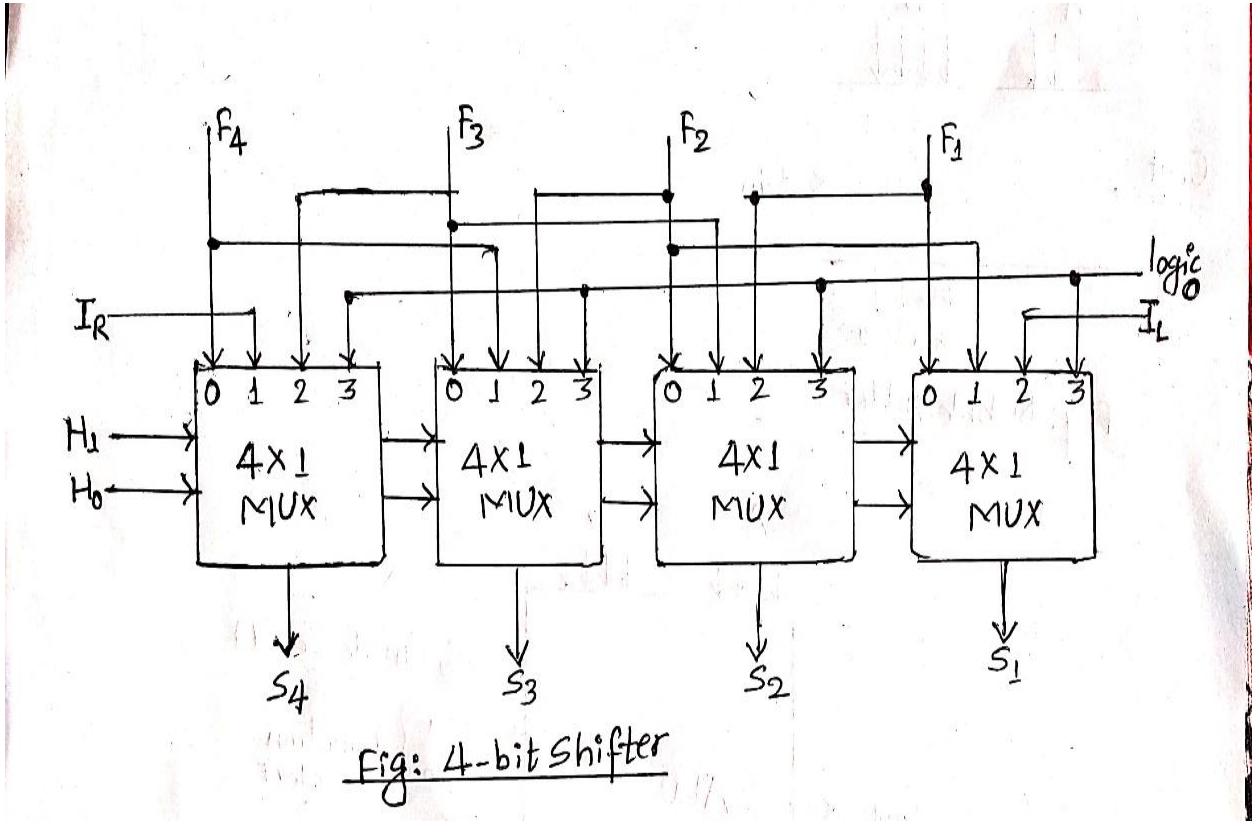


Fig: 4-bit Shifter

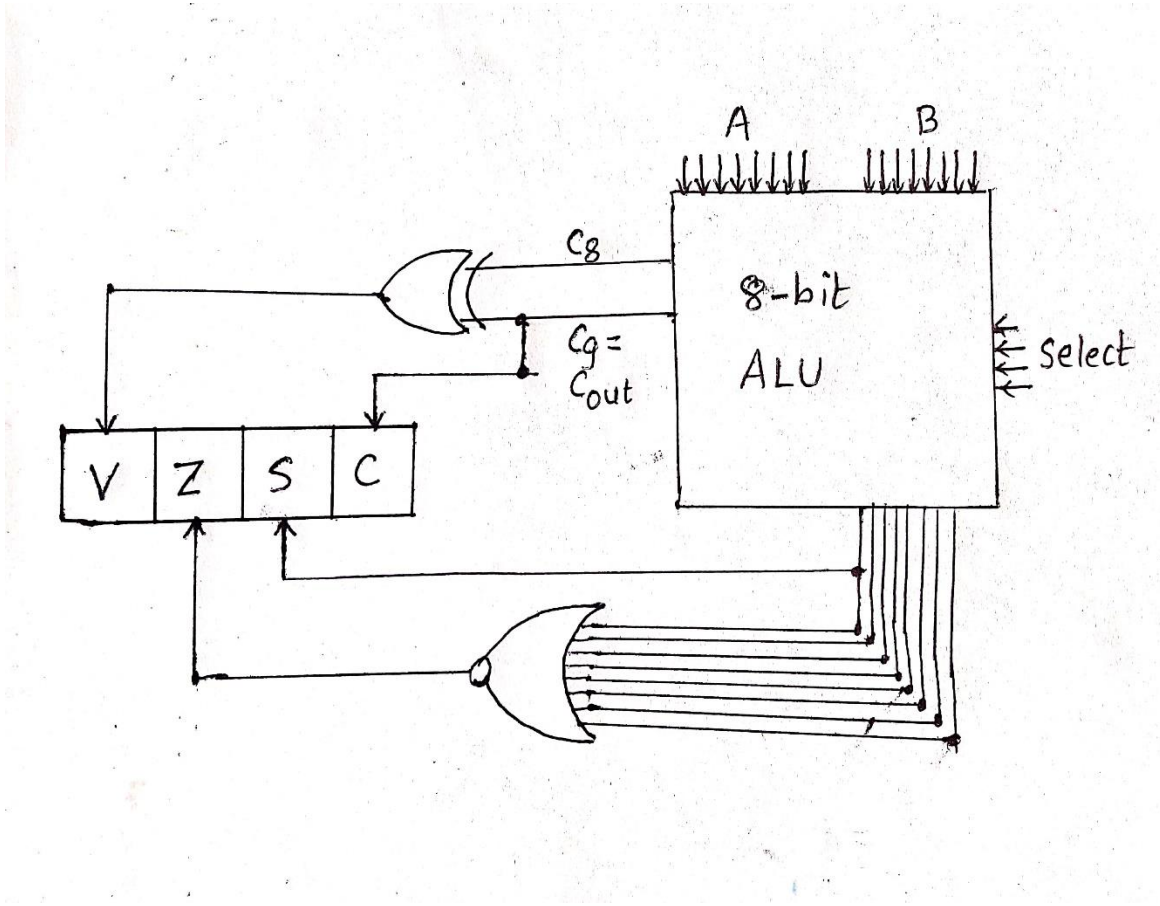
The function table of the 4 bit shifter is as:

Function table:

H_1	H_0	Operation	Function
0	0	$S \leftarrow F$	Transfer F to S
0	1	$S \leftarrow shr\ F$	Shift right F to S
1	0	$S \leftarrow shl\ F$	Shift left F to S
1	1	$S \leftarrow 0$	Transfer 0's into S

Status register

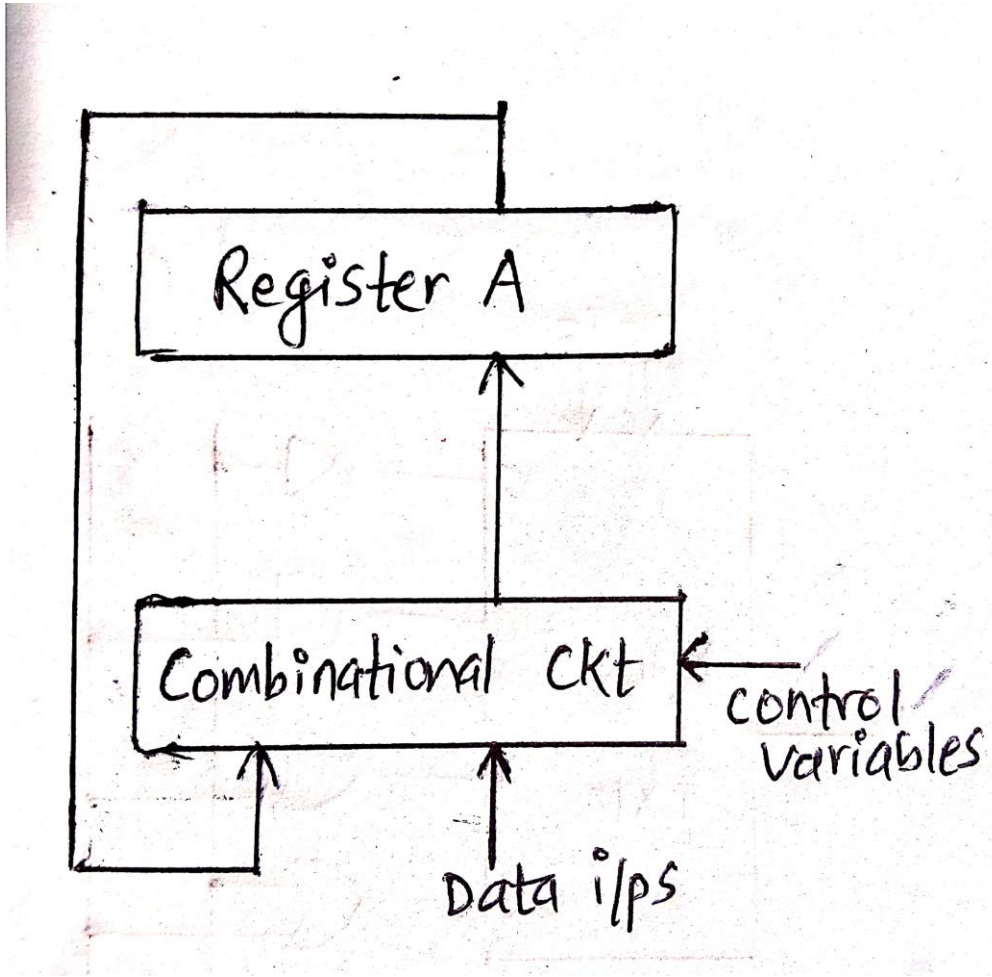
- Bit C (carry) is set if o/t carry of ALU is 1. It is cleared if the o/p is 0.
- Bit S (sign) is set if the highest order bit of the ALU o/p(the sign bit) is 1. It is cleared if the highest order bit is 0.
- Bit Z(zero) is set if o/p of ALU contains all 0's and cleared otherwise.
- Bit V (overflow) is set if the XOR of C8 and C9 is 1. This is the condition of overflow when the numbers are in sign 2's complement form.



Design of Accumulator

- Some processor units distinguish one register from all others and call it an accumulator register.
- Bidirectional register with parallel load connected to ALU.
- The accumulator an its associated logic constitute a sequential circuit.
- It consists n-stages and n-flip flops.
- Register A is referred to as accumulator and sometime denoted by AC.
- It is a multifunction register that can perform all the microoperations.
- Microoperations of an AC depends on the particular processor

The block diagram and the different micro operations of an accumulator is as shown



Control variables	Microoperations	Name
P_1	$A \leftarrow A+B$	Add
P_2	$A \leftarrow 0$	Clear
P_3	$A \leftarrow A'$	Complement
P_4	$A \leftarrow A \wedge B$	AND
P_5	$A \leftarrow A \vee B$	OR
P_6	$A \leftarrow A \oplus B$	XOR
P_7	$A \leftarrow$ Shr A	Shift right
P_8	$A \leftarrow$ Shl A	Shift left
P_9	$A \leftarrow A+1$	Increment

Processor unit

- Selection variables in a processor unit control the micro-operations executed within the processor during a CP.
- Selection variables control the buses, ALU, shifter and the destination register.
- Processor unit consists of registers and status register. The o/p of register go thru 2 MUX to select the i/p of ALU.
- I/p data from external source are also selected by the same MUX.
- O/p of ALU goes to the registers or external destination thru shifter.
- There are 16 selection variables in the unit and their operations are controlled by a control word.

Processor unit continue…

- 16 bit control word, when applied, specifies a micro operation.
- Bit of A selects source register for the i/p to left side of ALU and Bits of B selects the source register for i/p to right side of ALU.
- D field selects the destination register.
- F field together with Cin select a function for ALU.
- H field selects the type of shift in the shifter.
- All 16 bit control words are stored in control memory and each word specify a micro operation.
- The sequence of control word is read from the memory, one at a time, to initiate a desired micro operation. This type of control operation is called micro programming.

The diagram of a processor unit is shown below:

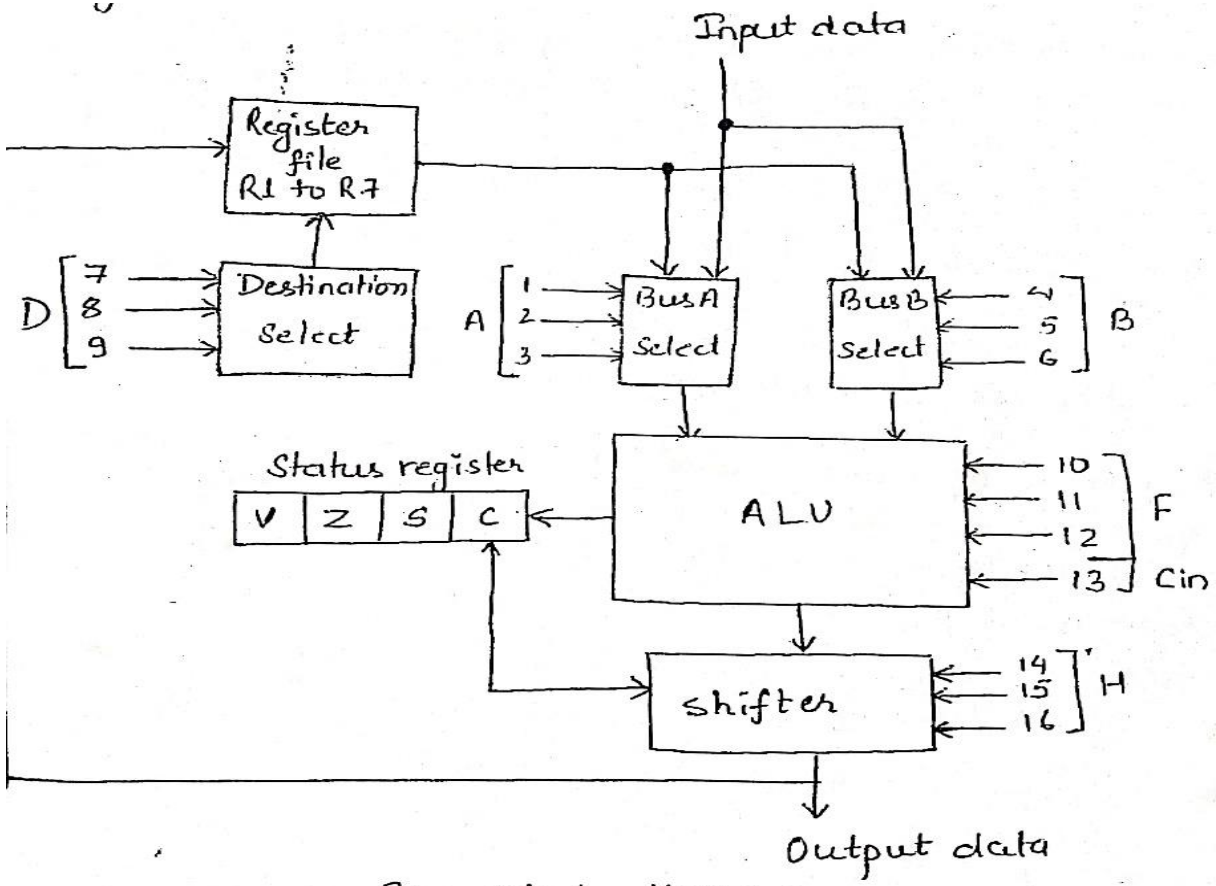


Fig: Block diagram

1 2 3	4 5 6	7 8 9	10 11 12	13	14 15 16
A	B	D	F	Cin	H

Control word