

EE671 : VLSI Design

Assignment 4

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No violations in connectivity (both signal and special routes)

```
EE671_31@vlsi73:~/Synthesis_ X + ▾
VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sat Oct 18 23:01:51 2025

Design Name: alu
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (59.4000, 59.0000)
Error Limit = 50; Warning Limit = 50
Check specified nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Oct 18 23:01:51 2025
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sat Oct 18 23:01:51 2025

Design Name: alu
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (59.4000, 59.0000)
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Check specified nets

Begin Summary
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End Time: Sat Oct 18 23:01:51 2025
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

No DRC violations :

```
EE671_31@vlsi73:~/Synthesis_<--> + <-->
```

Total Power

Total Internal Power:	0.94678721	90.9947%
Total Switching Power:	0.06768229	6.5049%
Total Leakage Power:	0.02601645	2.5004%
Total Power:	1.04048596	

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1485.31MB/3459.10MB/1588.65MB)

Output file is physical_design/power.rpt
#=check_same_via_cell_true # bool default=false user setting

*** Starting Verify DRC (MEM: 1723.1) ***

VERIFY DRC Starting Verification
VERIFY DRC Initializing
VERIFY DRC Deleting Existing Violations
VERIFY DRC Creating Sub-Areas
VERIFY DRC Using new threading
VERIFY DRC Sub-Area: {0.000 0.000 59.400 59.000} 1 of 1
VERIFY DRC Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 4.0M) ***

VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sat Oct 18 23:01:51 2025

Design Name: alu
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (59.4000, 59.0000)
Error Limit = 50; Warning Limit = 50
Check specified nets

Begin Summary
Found no problems or warnings.
End Summary

No Antenna violations:

```
EE671_31@vlsi73:~/Synthesis_<--> + <--> x
```

-----Output alu_netlist.v file-----
Writing Netlist "physical_design/alu_netlist.v" ...
Writing Netlist "physical_design/alu_netlist_pwr.v" ...
Pwr name (VDD).
Gnd name (VSS).
1 Pwr names and 1 Gnd names.
Creating all pg connections for top cell (alu).
Writing Netlist "physical_design/alu_netlist_nofil_pwr.v" ...
Pwr name (VDD).
Gnd name (VSS).
1 Pwr names and 1 Gnd names.
Creating all pg connections for top cell (alu).
Writing Netlist "physical_design/alu_netlist_nofil.v" ...
-----Save models for hierarchical flow-----
(saveModel) Begin generating models for alu (10/18/2025 23:01:53).
(saveModel) Running write_lef_abstract...

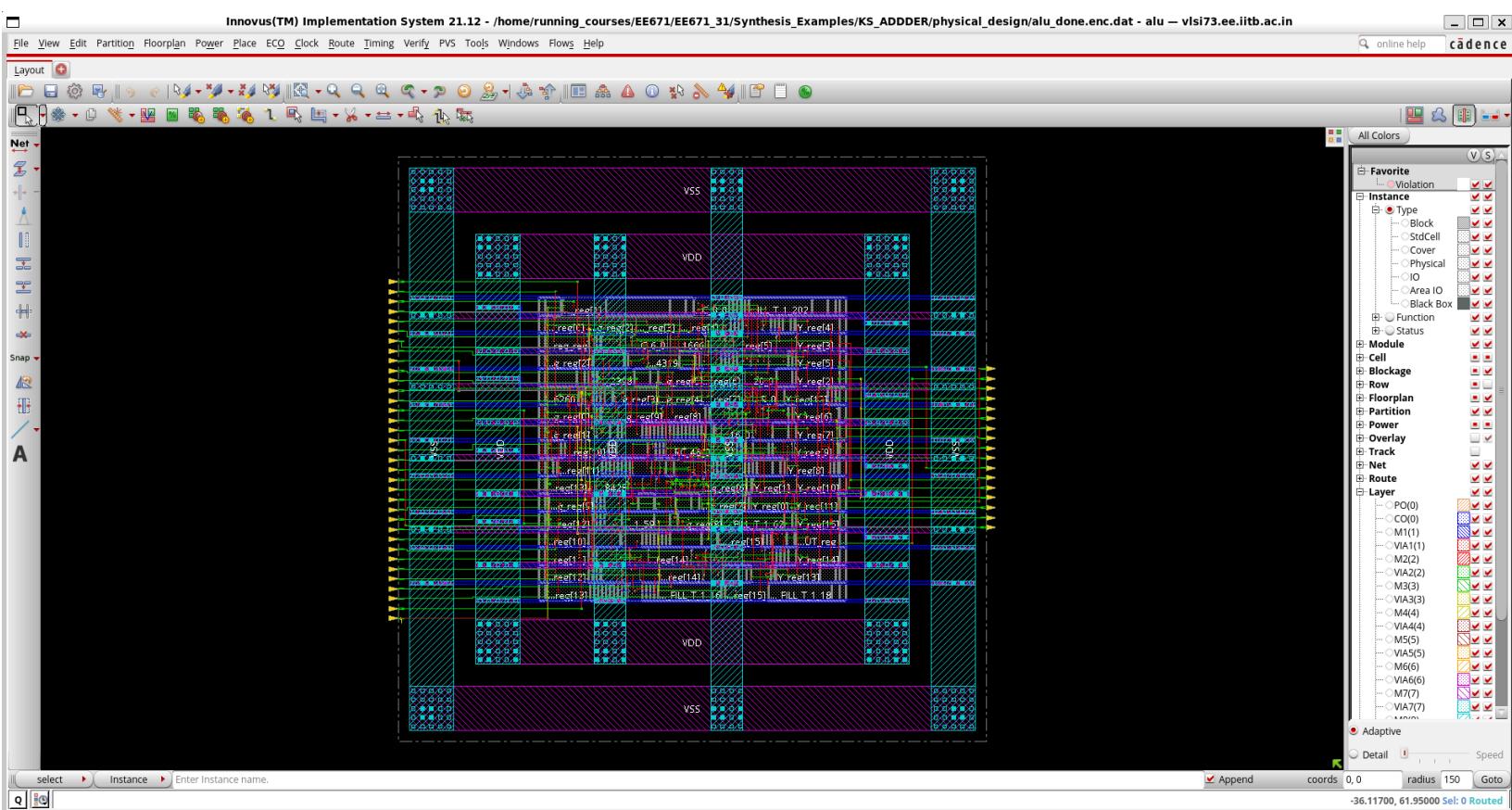
***** START VERIFY ANTENNA *****
Report File: alu.antenna.rpt
**WARN: (IMPVPA-55): Option -leffile for command verifyProcessAntenna is obsolete. Use 'lefOut -5.5 | -5.6 fileName' instead. The obsolete option still works in this release, but to avoid this warning and to ensure compatibility with future releases, remove -leffile from your script.
Type 'man IMPVPA-55' for more detail.
LEF Macro File: alu_hier_data/library/alu_antenna.lef
Verification Complete: 0 Violations
***** DONE VERIFY ANTENNA *****

2. Screenshot of the final Layout from the Innovus window.

[**Note:** If you have run the PnR flow using the script and not the GUI, exit the Innovus shell first. Launch Innovus again (a GUI will open). Then type the following command on the Innovus shell (replace alu with your cell name):

```
innovus 1> restoreDesign physical_design/alu_done.enc.dat/ alu
```

The GUI window should now show the entire layout.]



Following information from the post route timing, area and power reports:

Clock Frequency (MHz)	1000
Worst case setup slack [WNS in the report] (ns)	+0.015
Worst case hold slack [WNS in the report] (ns)	+0.051
Design area (μm^2)	3504.6
Power Consumption (Sequential Only) (μW)	886.3
Power Consumption (Combinational Only) (μW)	145.0
Total Power Consumption (Internal Only) (μW)	946.79
Total Power Consumption (Switching Only) (μW)	67.68
Total Power Consumption (Leakage Only) (μW)	26.02
Total Power Consumption (μW)	1040.49

Verify the post physical design RTL with a functional simulation using the same testbench that was used to verify the post synthesis RTL in assignment-3.
Provide a screenshot of the Gkwave waveform dump.

