EE671 : VLSI Design

Assignment 4

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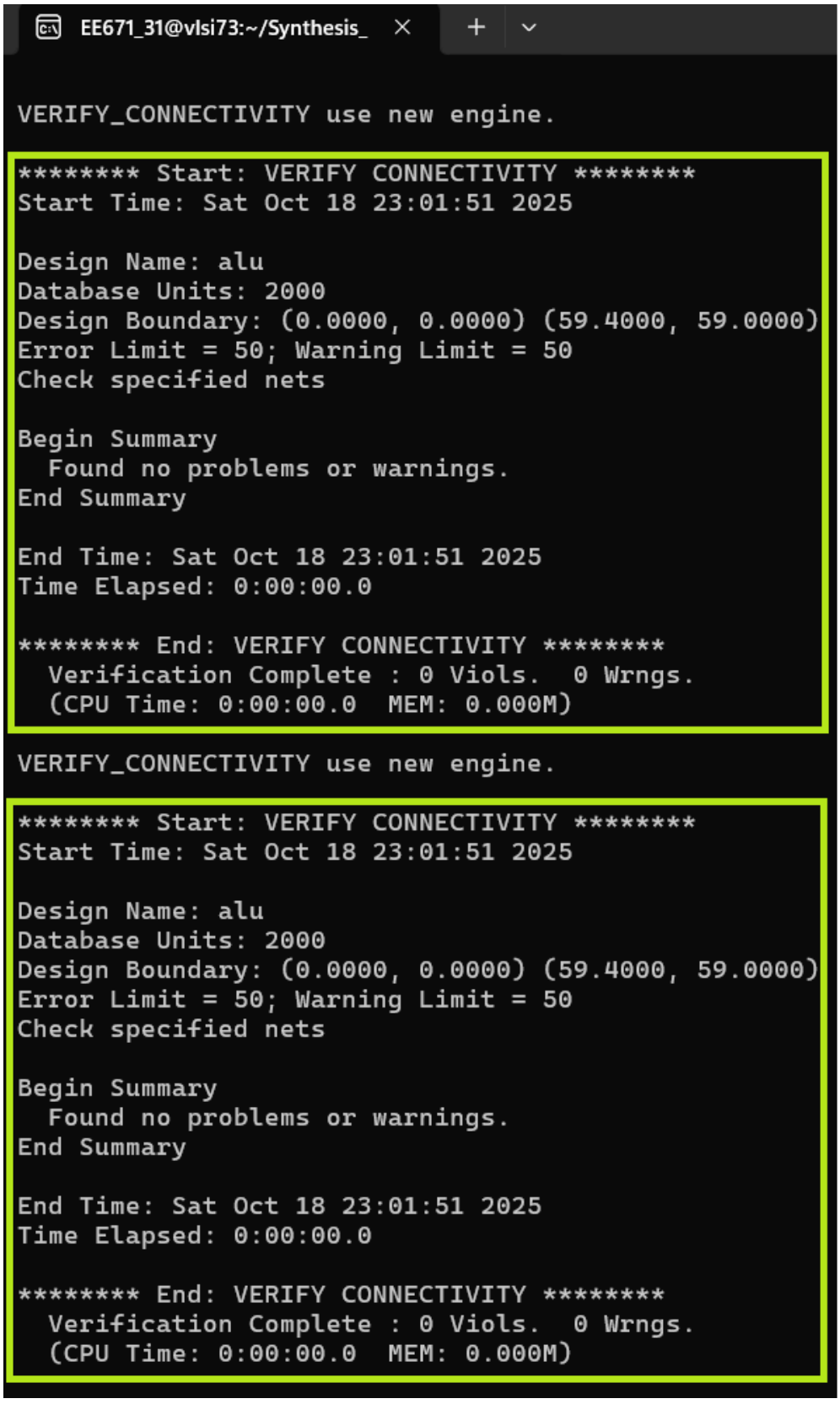
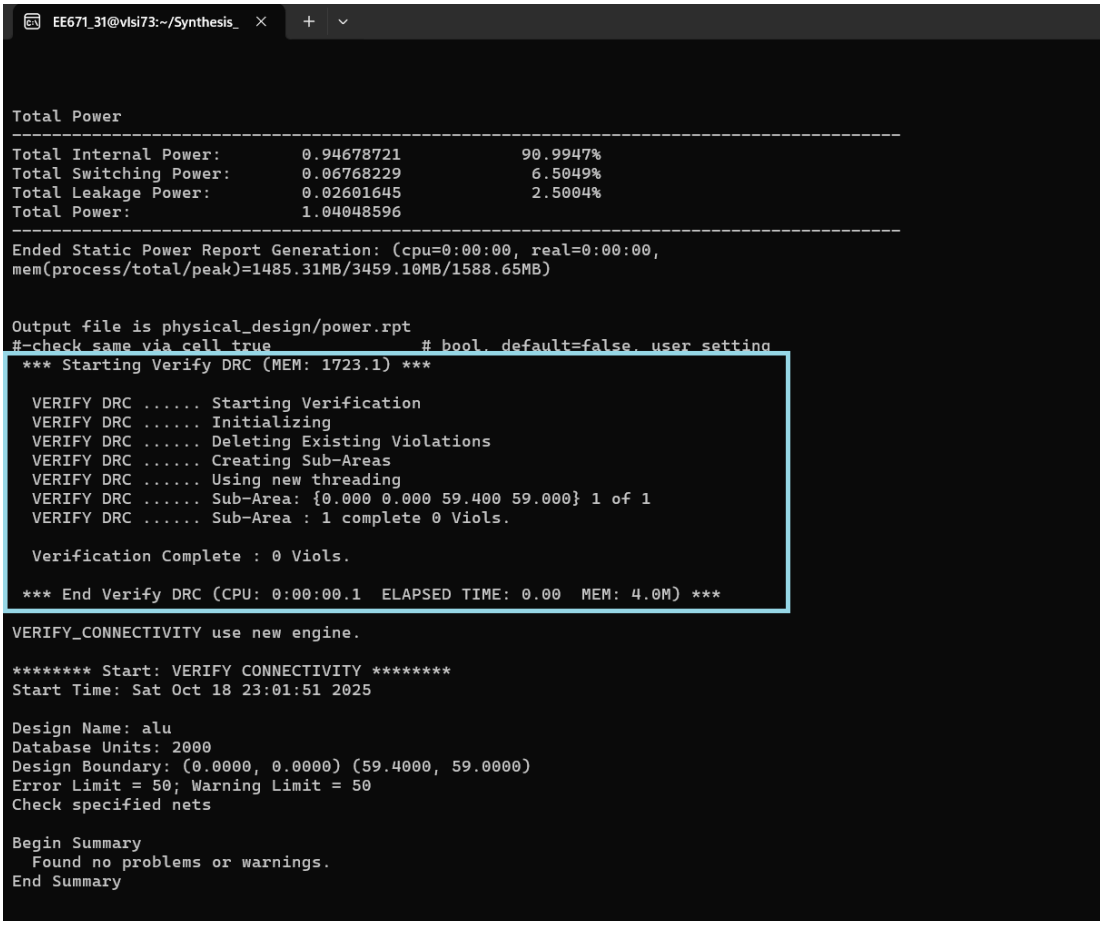
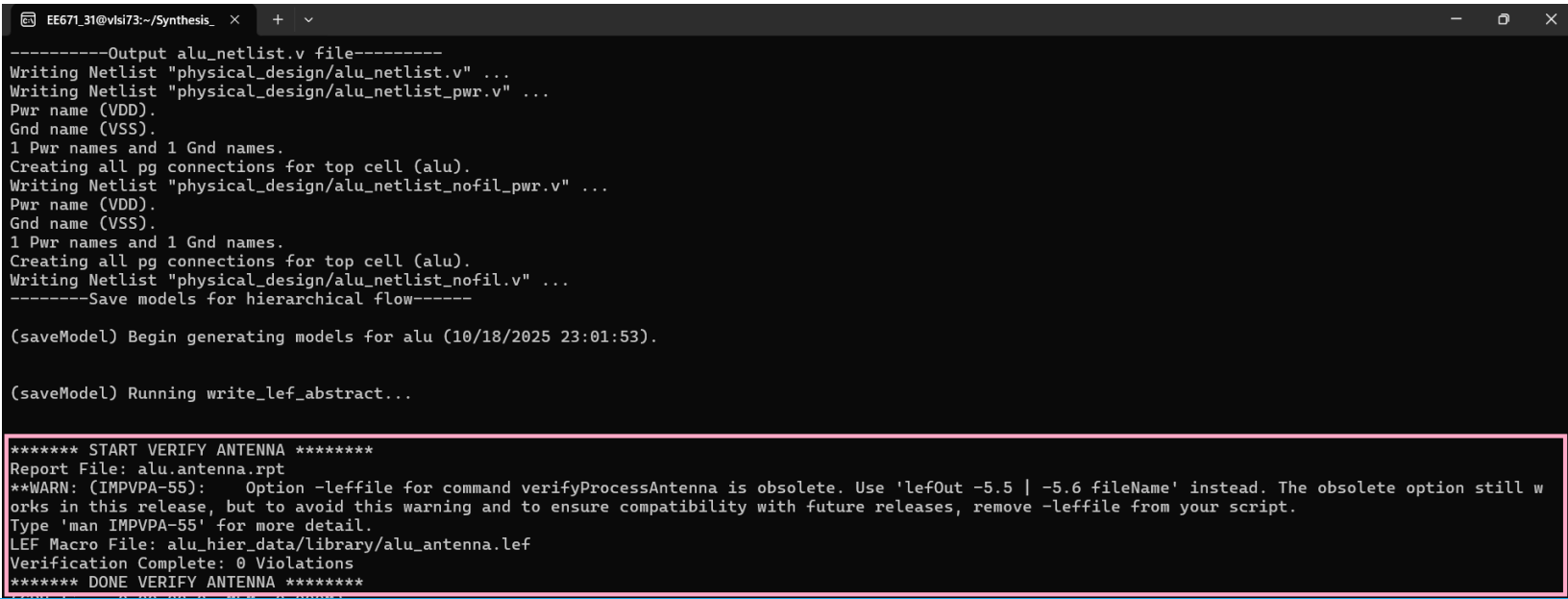
No violations in connectivity (both signal and special routes)



No DRC violations :



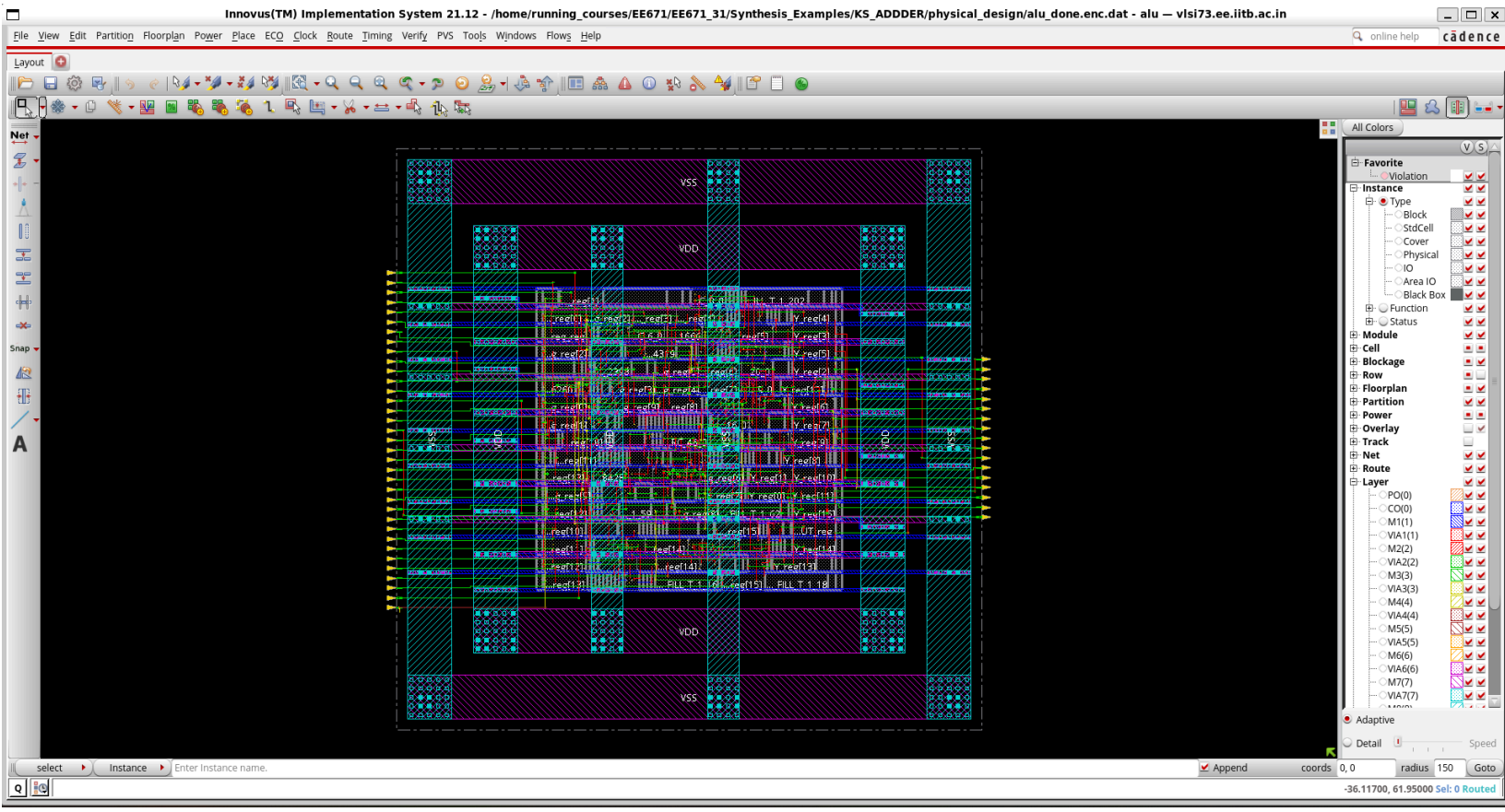
No Antenna violations:



2. Screenshot of the final Layout from the Innovus window.
[Note: If you have run the PnR flow using the script and not the GUI, exit the Innovus shell first. Launch Innovus again (a GUI will open). Then type the following command on the Innovus shell (replace alu with your cell name):

```
innovus 1> restoreDesign physical_design/alu_done.enc.dat/ alu
```

The GUI window should now show the entire layout.]



Following information from the post route timing, area and power reports:

Clock Frequency (MHz)	**1000**
Worst case setup slack [WNS in the report] (ns)	**+0.015**
Worst case hold slack [WNS in the report] (ns)	**+0.051**
Design area (µm2)	**3504.6**
Power Consumption (Sequential Only) (µW)	**886.3**
Power Consumption (Combinational Only) (µW)	**145.0**
Total Power Consumption (Internal Only) (µW)	**946.79**
Total Power Consumption (Switching Only) (µW)	**67.68**
Total Power Consumption (Leakage Only) (µW)	**26.02**
Total Power Consumption (µW)	**1040.49**

Verify the post physical design RTL with a functional simulation using the same testbench that was used to verify the post synthesis RTL in assignment-3. Provide a screenshot of the Gtkwave waveform dump.