Experiment 12 :
Sub-threshold Characteristics of N-channel MOSFET

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Aim of the Experiment

In this experiment , following tasks need to be performed :

1. Obtain the sub-threshold I_d vs V_{gs} characteristics of NMOS. The main aim is -
   A) Perform the experiment using an OP-AMP with low noise figure and plot I_d vs V_{gs} characteristics and compare the plots obtained.
2. Check the continuity of I_d vs V_{gs} characteristics beyond the sub-threshold region.
3. Employing the NMOS to be used as a Common Source Amplifier in sub-threshold region.

Background Theory

An N-channel MOSFET is Field Effect Transistor which has 4 terminals i.e 1) Drain 2) Gate 3) Source 4) Body. The body terminal of NMOS is connected to lowest voltage possible in the circuit i.e ground. For an NMOS to be 'ON', the applied Gate to Source Voltage must be greater than Threshold

Voltage V_{th} else it is assumed to be 'OFF', i.e. $V_{gs} \geq V_{th}$.

In true sense however the MOSFET is not 'OFF' but conducts some small amount of current. When the Gate to Source Voltage is less than threshold voltage, few electrons are still present inside the channel. When Drain Voltage is applied , there exists a depletion region near the drain junction and even lower concentration of minority carriers.

Thus electrons near the Source Junction begins to move towards Drain Junction primarily due to mechanism of Diffusion leading to Sub Threshold Current. The equation of Drain current in Sub Threshold region is given by the following equation.

$$I_d = I_o e^{(\frac{V_{gs}-V_{th}}{\eta V_t})}(1 - e^{\frac{-V_{ds}}{\eta V_t}})$$

where,

$$I_o = \mu_n C_{ox}\left(\frac{W}{L}\right){V_t}^2(\eta - 1)$$

I_d = Drain Current,
V_{gs} = Gate to Source Voltage,
V_{th} = Threshold Voltage of NMOS,
V_t = Thermal Voltage,
V_{ds} = Drain to Source Voltage,
μ_n = Mobility of electron,
C_{ox} = Gate Oxide Capacitance per unit area,
$(\frac{W}{L})$ = Aspect Ratio of NMOS,
$\eta = 1 + (\frac{C_d}{C_{ox}})$ where C_d is Depletion Capacitance. It is called as Sub Threshold Slope Factor.

Approach for designing the experiment

- As seen from equation above , equation for drain current in Sub Threshold region is a very complex equation. Hence before proceeding towards the design part of equation we should try to eliminate at-least one variable (preferably V_{ds} because we have to plot Id vs V_{gs} characteristics) to make it a function of one variable.

- We start with some assumption of the value of η, say 10. Value of $\eta V_t = 0.256$ at room temperature. If $V_{ds} = 2V$, the exponential term containing V_{ds} diminishes to zero. Thus the overall term containing V_{ds} becomes 1. This makes the problem simple. Thus we have,

$$I_d \approx I_o e^{(\frac{V_{gs}-V_{th}}{\eta Vt})}$$

- **VERY IMP NOTE** : We have assumed the value of η to be 10. After performing the experiment we will back calculate the value of η from some graph. If the value is less than 10, we are safe and the assumption of the exponential term containing V_{ds} diminishing to zero still holds. If η is greater than 10, we need to pick up another value of V_{ds} and perform the experiment again.

Methodology of designing the experiment

- The D.M.M. available in the laboratory/Personal D.M.M. can measure currents accurately to a value of around 100 μA . However , the Sub Threshold I_d current which you are about to measure is of order of few hundreds of nA.

- Hence we should employ a different methodology for measuring these small currents , perhaps an indirect way of measuring current (i.e measure some Voltage, V in the order of few volts and thus obtain I_d from the measured V) .

- This is done using an OP-AMP and Resistor in Negative Feedback fashion. The Low Noise figure of OP-AMP and High Precision of resistors are very important as the current we are about to measure are small in magnitude. Having an OP-AMP with high noise figure can cause it to be driven into Saturation easily.

Components Necessary

- ALD1106 NMOS I.C.

- TLV9161 OP-AMP

- Keithley Power Supply

- 10 M Ω and 1 M Ω resistor - 2 quantities

- 100 Ω Potentiometer
- 3 D.M.M. (1 from Lab and 2 from Self)

Pin Diagram of ALD1106

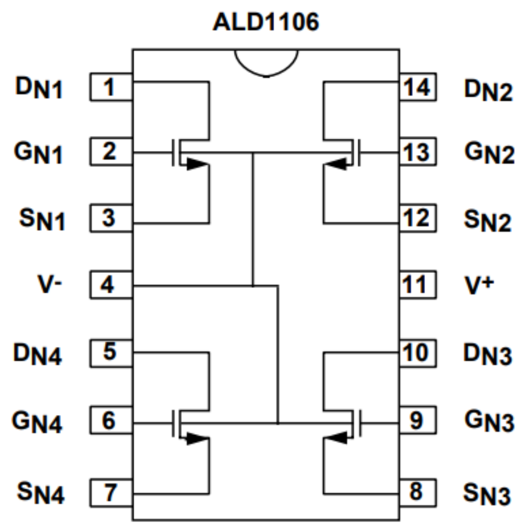

Figure 1: ALD1106 Pinout

Pin Diagram and functions of TLV9161

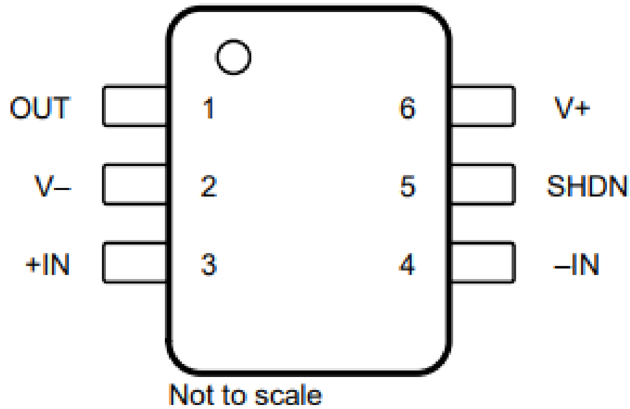

Figure 2: TLV9161 Pinout in SOT-23 package

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output
SHDN	5	I	Shutdown: low = amplifier enabled, high = amplifier disabled
V+	6	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

Figure 3: Pin Functions of TLV9161

Part - 1 : Transfer Characteristics of NMOS

Part A)

Measure I_d vs V_{gs} using Low Noise Figure OP-AMP (TLV9161) in Sub-threshold Region.
Follow the pin diagram given in subsection **2.6** for connections. Note that V_+ should be connected to $+8V$ and V_- should be connected to $-8V$.
Also connect the pin SHDN to $-8V$ as it enables the OP-AMP. The circuit diagram shown in the following figure.

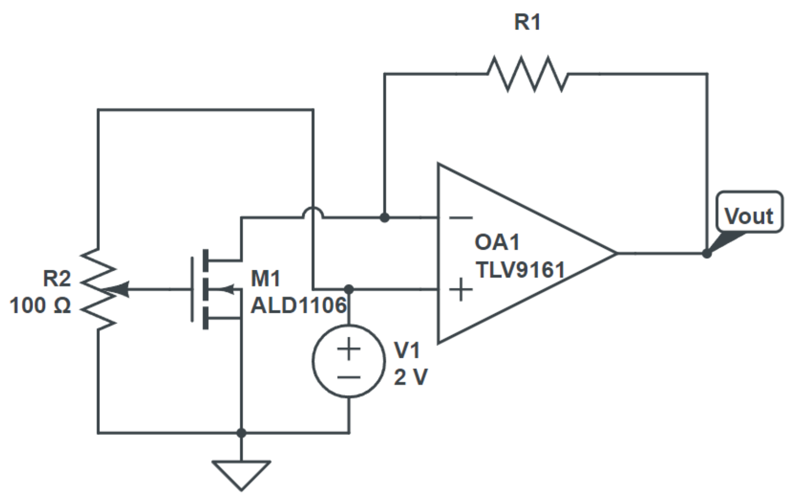

Figure 4: Circuit Diagram for Sub-threshold Current Measurement

1. Connect the Laboratory D.M.M. such that it measures V_{gs} .
2. Connect the D.M.M. you have purchased to measure V_{out} of OP-AMP .
3. If you have a look at the data sheet of ALD1106, the threshold voltage of NMOS is somewhere between $0.4V$ to $1V$. Vary V_{gs} from $0V$ to the point where the OP-AMP's output voltage, V_{out} saturates. The step size of the measurement should be of $0.02V$.

Clarification on Circuit Operation-

- The circuit uses an OP-AMP in negative feedback . The Virtual Short ensures that $V_{ds} = V_{inv} = 2V$ (which is equal to $V_{non-inv}$) .
- The current I_d which is set up in the circuit is given by the equations as mentioned in the **Approach**. This same current I_d flows through 20 $M\Omega$ resistor because the OP-AMP draws no current.
- Equation governing the flow of current through resistor is that of simple Ohm's Law. Hence,

$$I_d = \left(\frac{V_{out} - V_{inv}}{20}\right) \mu A$$

  You can convert this to nA as well. Plot I_d vs V_{gs} characteristics.

Points to remember-

- Use the Keithley Power Supply for taking the readings.
- It is very important to have a look at values of V_{inv} and V_{out}.
- We know that as we increase the value of V_{gs}, the current I_d increases. However till the point the Virtual Short is maintained, V_{inv} will be maintained at potential equal to $V_{non-inv}$. This means that as I_d increases, V_{out} also increases. It might so happen that at some V_{gs}, the OP-AMP Voltage V_{out} saturates. Hence it is important to keep an eye at the value of V_{inv}. Once the OP-AMP saturates, the Virtual Short fails and hence the claims we made above including Ohm's Law fails. Hence we should stop taking readings beyond that point.
- Once you see the V_{inv} ($= V_{non-inv}$) changing from fixed value or V_{out} saturating (whichever happens first) , one should stop taking the readings.
- Do not change the range settings on D.M.M. while measuring the Voltage values.
- When you start changing the value of Voltage V_{gs} from $0V$ to some value V_{01}, it might so happen that V_{out} might not change for these range of values of V_{gs}. This happens because the current I_d flowing might not be sufficient enough to produce measurable

change (measurable change on D.M.M.) in V_{out}. Once you start seeing some changes in the values of V_{out}, it is at this point one should should start taking the readings. The corresponding V_{gs} value of should be considered as the first reading and the values of V_{gs} prior to that must be discarded.

- Make sure to connect the Source and Body terminals of ALD1106 NMOS to Ground.

4. Initially take $R_1 = 10M\Omega$.

5. Compute the values of I_d by changing the value of V_{gs} in a fashion similar to what we did in PART A. Stop taking the readings when either the OP-AMP saturates or the V_{inv} starts to change. Make sure not to change the value of V_{gs} beyond this point.

6. Now carefully remove the 10 $M\Omega$ resistance without disturbing the circuit and insert R1 = 1 $M\Omega$ in place of 10 $M\Omega$ resistor. Start by taking the values of I_d from the point where you stopped changing the value of V_{gs} for R = 10 $M\Omega$ resistor (This is for maintaining continuity in the readings). Now increase the value of V_{gs} and keep on taking the readings again till the OP-AMP saturates or $V_{Inverting}$ changes . Note the value of V_{gs} where you have stopped taking the readings .

7. Concatenate the values of I_d received from 10 $M\Omega$ and 1 $M\Omega$ resistors and plot the resultant I_d vs V_{gs} graph.

8. **Conclusions you need to draw from the readings-**

   (a) Plot the I_d vs V_{gs} Sub Threshold Characteristics obtained.

   (b) For Part B readings , one should also plot the $\log_{10} I_d$ vs V_{gs} and measure the Sub threshold Swing . Remember we have assumed the value of η and we need to cross verify if the assumed value holds or not . For this we will calculate the value of Sub Threshold Swing , S which is equal to -

$$S = \frac{dV_{gs}}{d(\log_{10} Id)}$$

(c) The value of S is obtained by taking the slope of the graph $\log_{10} Id$ vs V_{gs} and taking inverse of it . Make sure you express the value of S in $\frac{mV}{decade}$. The slope of $\log_{10} Id$ vs V_{gs} is also known as Sub Threshold Slope .

(d) For a long channel transistor, the value of S is around 60 $\frac{mV}{decade}$. This assumes that the value of η is 1. For a FET such as ALD1106 the value of S is equal to,

$$S = 60\eta \, \frac{mV}{decade}$$

(e) From this we can calculate the value of η. If the value of $\eta \geq 10$, we need to change the value of V_{ds} and repeat the whole process again. Else we are good with the readings.

9. The graph of $\log_{10} Id$ vs V_{gs} cuts the Y-axis at some point. Let us call that point I_{off}. It is called as Off Current of NMOS. This becomes an important parameter in circuit design. Basically it tells us what would be the value of current I_d flowing through the MOSFET even if the value of $V_{gs} = 0$. This gives an idea about Static Power dissipation in the circuits which uses MOSFETs. State the value of I_{off} obtained. Also calculate the power dissipated in the MOSFET under such conditions. Any value greater than few nW is dangerously high!

Part -2 : Graph continuity

1) Remember for **Part B** of the readings you were asked to stop taking readings for some V_{gs} for the case of R1 = $1M\Omega$. We will be making measurements beyond this value now. This V_{gs} would be somewhere around $0.7V$ - $0.8V$. Increase the value of V_{gs} beyond this point using the potentiometer.

2) Also note that by this point V_{gs} value is sufficiently high such that we do not need the circuit in Part - 1 of the measurements. We can directly measure I_d because currents would be in order of few μA.

3) Make the connections as shown in the figure below-

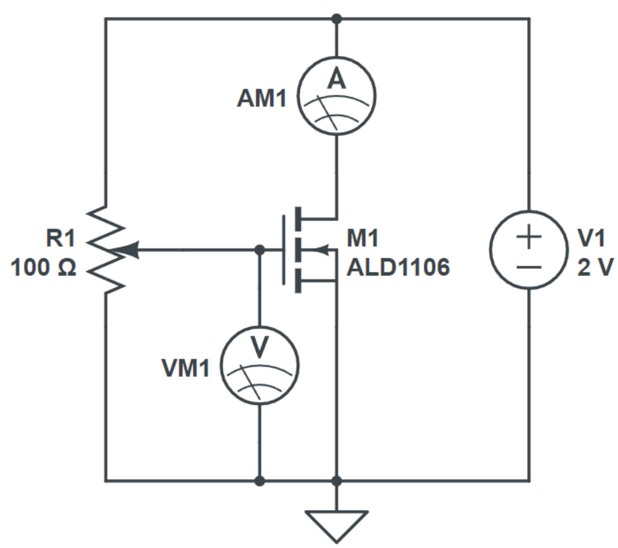

Figure 5: Circuit Diagram for testing continuity of Characteristics

4) Increase the value of V_{gs} and measure corresponding value of I_d. The step size in which you will increase V_{gs} should be of $0.1V$. Stop taking readings when V_{gs} is around $1.9V$.

Conclusions to be drawn from the readings -

1) Carefully note that once the V_{gs} value crosses $1V$ we are somewhat sure that NMOS is not in Sub-threshold region. It is in some other region. Comment down what region NMOS is in in this case.

Part -3 : Common Source Amplifier using MOSFET biased in Sub-Threshold

- You would have heard of Common Source Amplifier which makes use of MOSFET in Saturation Region. One can manage to get a decent gain of roughly around 15 to 20 using discrete transistors and components. However, as our technology nodes become smaller, with it comes the challenge of using smaller and smaller voltages to ensure our transistors are operating in Saturation. This leaves with very little headroom for our transistors to manage their output swings to stay in Saturation region and also strains power dissipation that can happen in the circuit. So how about using transistor in Sub-Threshold region?

- We already know that Sub-Threshold regions use smaller Voltages. Coupled to it the currents are in order of few nA. This can help us design an amplifier. Even though the gain may not be great, we can always cascade amplifiers and get desired gain.

Steps to follow -

1. Connect the circuit as shown in the figure. Set the V_{gs} value by making D.C. Offset on function generator = 400 mV . Do not provide sine wave as of now . Also make sure not to connect the the V_{out} to D.S.O.
2. Connect a D.M.M. to the drain node and vary V3 till the D.M.M. reads $2V$. This sets the V_{ds} to $2V$. Remove the D.M.M.
3. For Input Small Signal settings, set the function generator so that it applies a sine wave of frequency $50Hz$, $50mV$ Peak to Peak . Let the D.C. Offset be 400 mV . The D.C. offset of 400 mV will be superimposed on the sine wave .
4. Now connect the V_{out} node to D.S.O. and observe the Peak to Peak Voltage of the V_{out}. Note down the Value.
5. Gain of Amplifier = $\frac{V_{out(p-p)}}{V_{in(p-p)}}$
6. Report the gain.

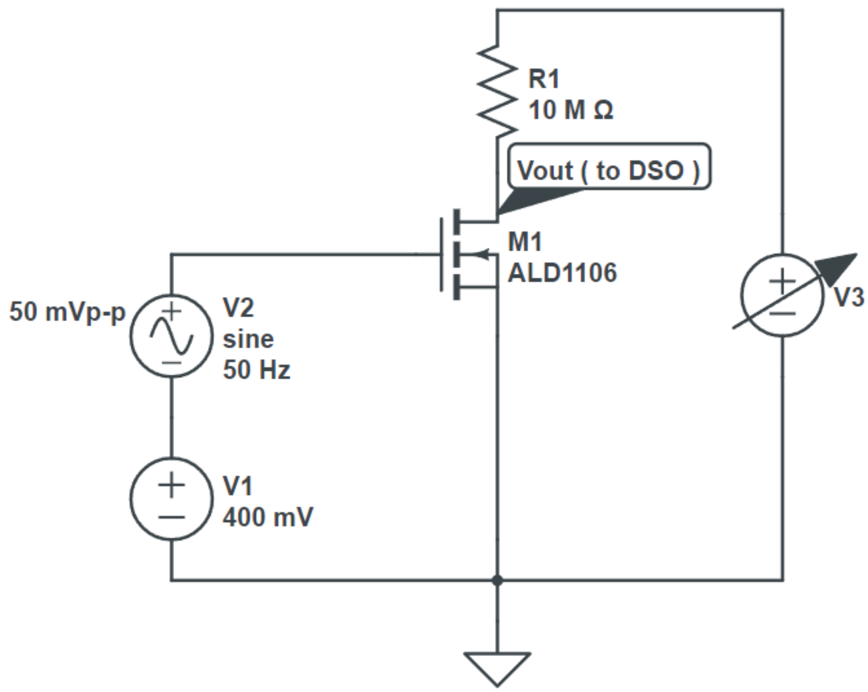

Figure 6: Common Source Amplifier Design

Conclusions to be drawn from the circuit -

1. Gain of a Basic Common Source Amplifier in Sub-threshold Region might be poor compared to Saturation Region of Operation. But it is respectable enough to allow it to be used as an Amplifier.
2. Note that the currents involved in Sub-threshold Region of Operation are of the order of few nA. Hence the current driving capability of the amplifiers are pretty much limited unlike the Saturation region. Which is why we cannot use them in applications which needs high current drives.