N-channel MOSFET I-V Characteristics

Electronic Devices and Characterization
Experiment 9

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Think it. Make it. Prove it.

Aim of the experiment

In this experiment, the following tasks need to be performed:

- Obtain output and transfer characteristics of an N-channel enhancement type MOSFET (also called NMOS).
- Measure of trans-conductance and output resistance from the obtained characteristics.
- Investigate the effect of body bias on the characteristics of the NMOS.

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Background Information

- The MOSFET is the commonly used transistor in both digital and analog circuits.
- It has four terminals- Gate (G), Drain (D), Source (S) and Body (B).
- The device working principle is that the voltage applied between its gate and source terminal controls the current through the source and drain terminals.
- The body terminal of an PMOS is connected to the highest voltage in the circuit i.e, V_{DD} while that of an NMOS is connected to ground.

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Background Information

- For an NMOS to be "ON", the applied gate-source voltage must be greater than the threshold voltage i.e. $V_{GS} > V_T$. Otherwise it is said to be "OFF" (or in cut-off region).
- Conditions for different operating regions of an NMOS that is turned on-
  - Linear Region : $V_{DS} < V_{GS} - V_T$
  - Saturation Region : $V_{DS} \geq V_{GS} - V_T$

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Background Information

The NMOS current equation (in different regions):

$$I_D \approx 0 \qquad \text{Cut-off region}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} V_{DS} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \qquad \text{Linear region}$$

$$I_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \qquad \text{Saturation region}$$

μ_n - mobility of charge carriers (electrons in NMOS)
C_{ox} - per unit area capacitance between the gate and body
W, L - width and length of the channel respectively
λ - channel length modulation factor

The trans-conductance and the output resistance are respectively given by-

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{const\ V_{DS}} \qquad r_o = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{const\ V_{GS}}$$

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Components Necessary

- CD4007 IC
- 1k Potentiometer $\times 2$
- Breadboard and connecting wire
- DC power supply [Note: Ensure that when using the Keithley power supply, the current limit on all channels is set to 1A. This prevents the supply from saturating at a specific voltage and operating as a constant current source.]

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CD4007 MOS

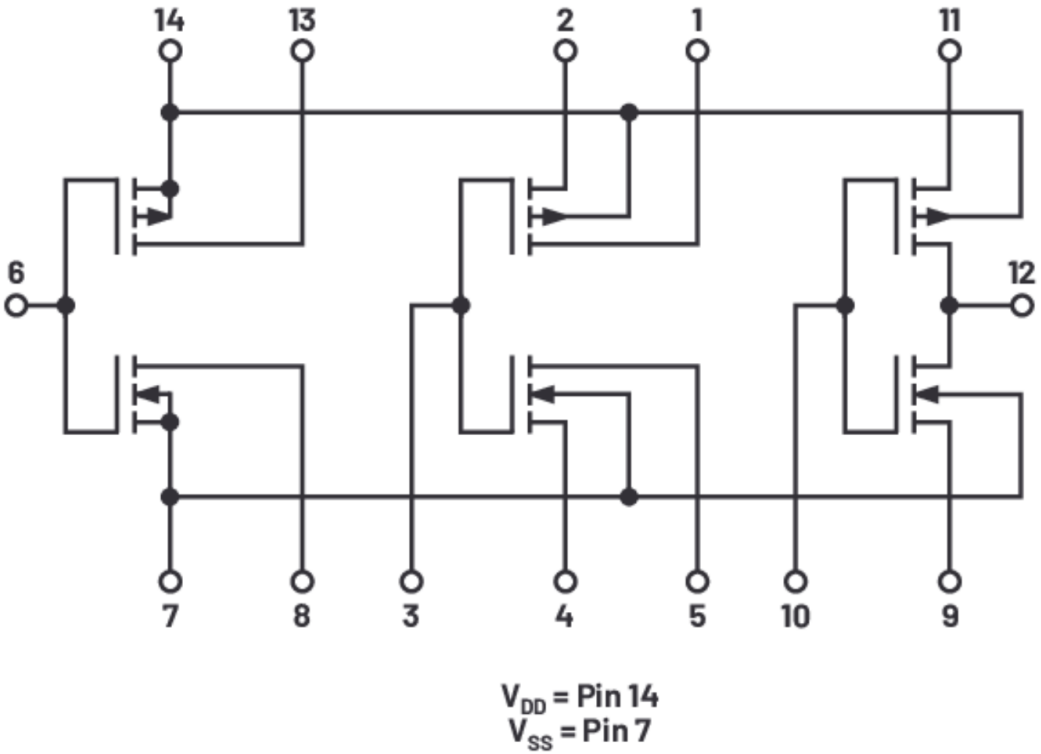

Figure: CD4007

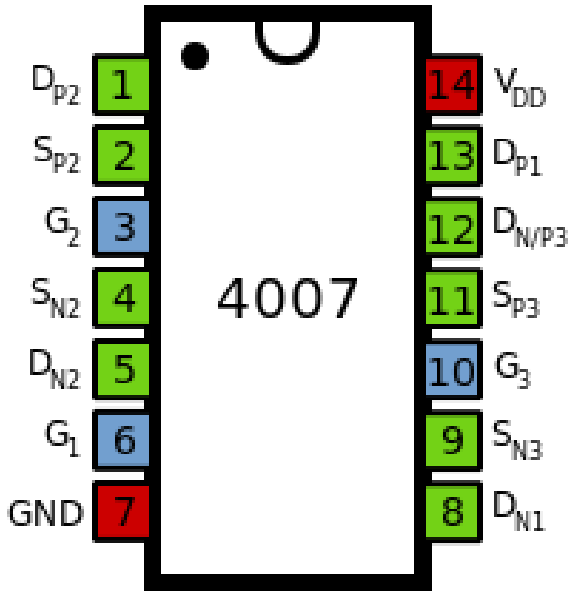

Figure: CD4007 pinout

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Part I : Transfer Characteristics (Linear)

Estimate the value of threshold voltage and trans-conductance in linear region:

- Bias the transistor in linear region by keeping $V_{DS} = 200\ mV$.
- Plot I_D vs V_{GS} characteristics by varying V_{GS} from 0 to $3V$.
- From this characteristic, obtain V_T and g_m.

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Part I : Transfer Characteristics (Saturation)

Estimate the value of threshold voltage and trans-conductance in saturation region:

- Bias the transistor in saturation region by keeping $V_{DS} = 3V$.
- Plot I_D vs V_{GS} characteristics by varying V_{GS} from 0 to $3V$.
- From this characteristic, obtain V_T and g_m.

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Part II : Drain Characteristics

For the drain characteristics, I_D vs V_{DS} must be plotted for multiple (3 different) V_{GS} values.

- Measure I_D vs V_{DS} by varying V_{DS} from 0 to $5V$, while keeping V_{GS} constant at $1.5V$.
- Repeat the same for $V_{GS} = 2.5V$ and $3.5V$.
- Plot all the 3 characteristics in a single plot to observe the drain characteristics.
- Find the output resistance r_o using the slope of the plot for $V_{GS} = 3.5V$, in saturation region.

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Circuit for Part I and Part II

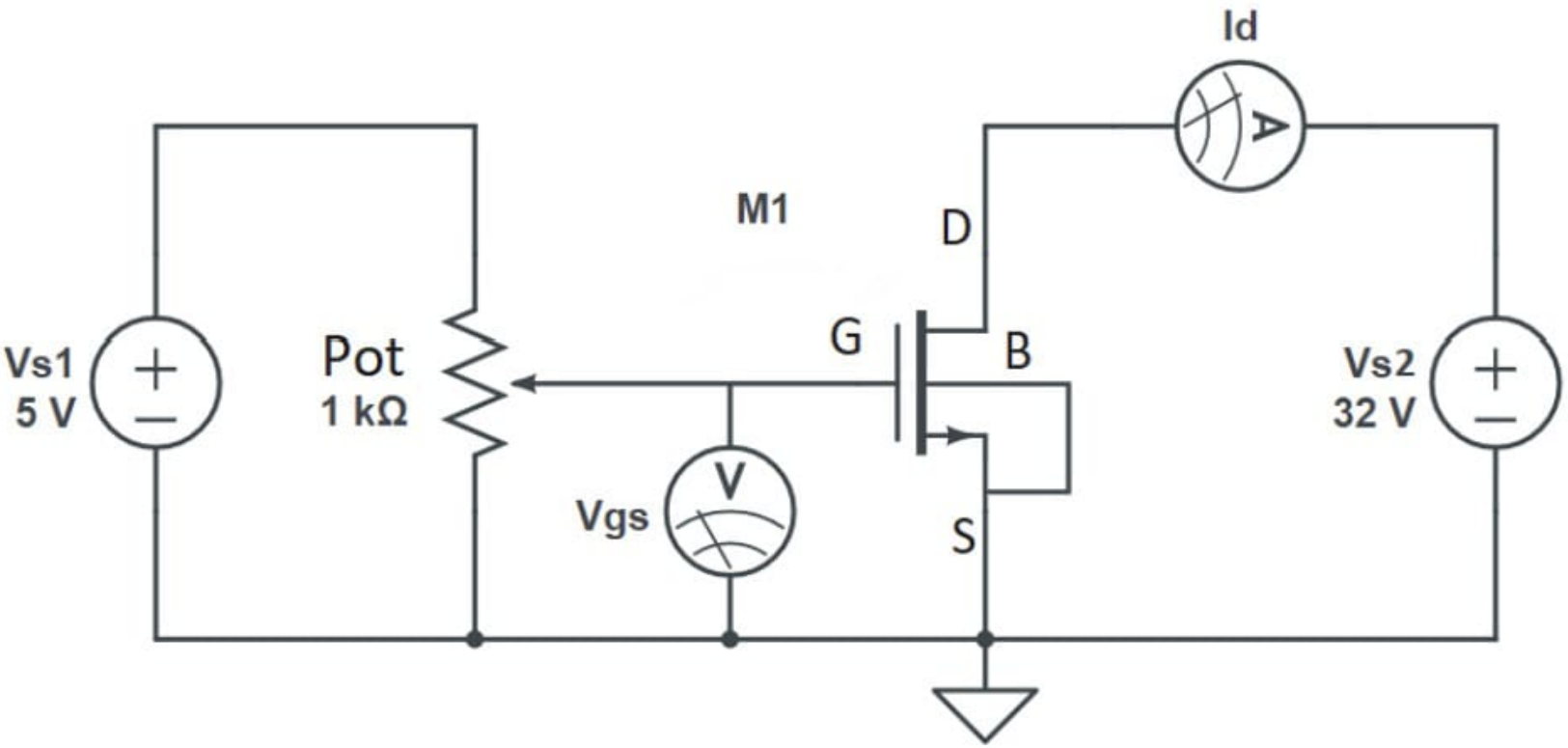

Figure: NMOS I-V circuit

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Part III : Body Effect

- Bias the transistor in linear region by keeping $V_{DS} = 200mV$.
- Repeat the step from Part I (linear) to get 3 more sets of I_D vs V_{GS} characteristics for $V_{SB} = 1V, 2V$ and $3V$.
- Show all five I_D vs V_{GS} characteristics on the same plot.
- Obtain the value of threshold voltage from each plot.
- Plot V_T vs V_{SB} and obtain body effect coefficient (γ) using below equation.

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s}\right)$$

Here, ϕ_s is Surface Potential $= 0.9V$ and V_{T0} is the threshold voltage when $V_{SB} = 0V$.

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Circuit for Part III

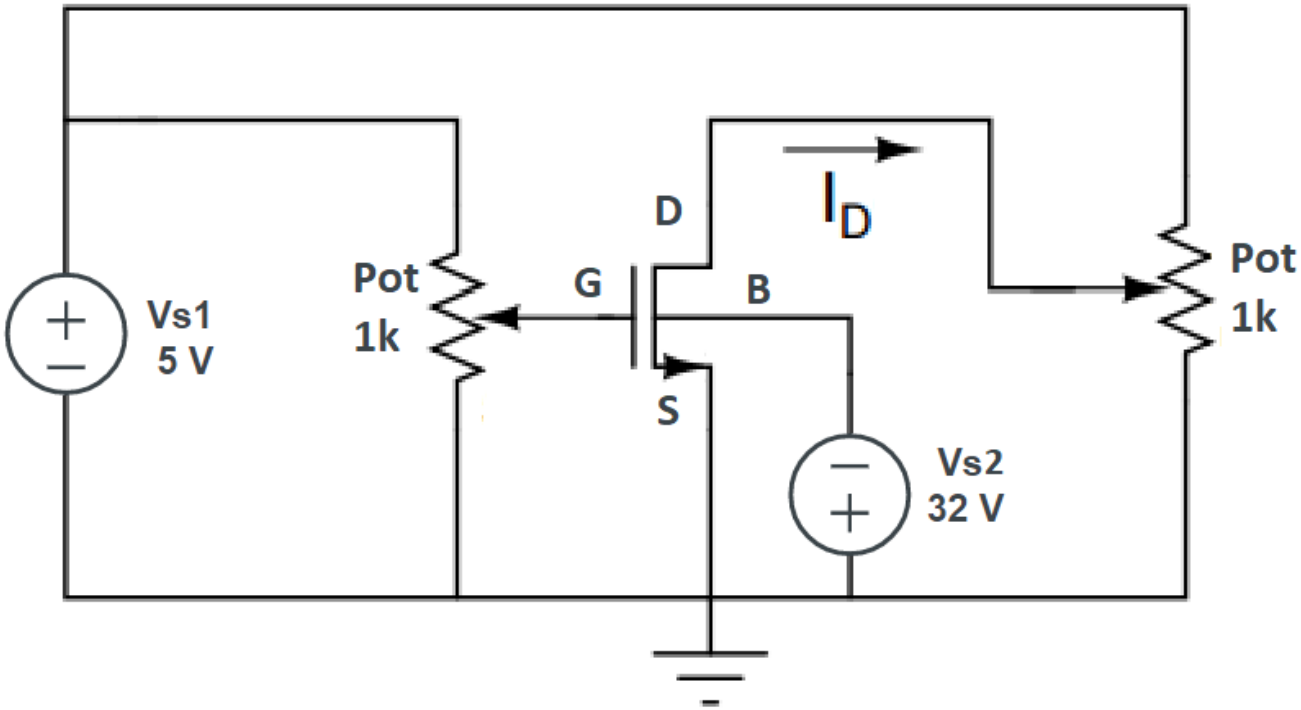

Figure: NMOS Body effect circuit

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