EE236 : Electronic Devices Lab
Lab 5 [Tuesday Batch]

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1 Aim of The Experiment

1. The following is done in dark conditions :
   - Plot I_D-V_D and ln(I_D)-V_D characteristics at all temperatures.
   - From I_D-V_D plots find voltage at 1 mA, 2 mA and 5 mA at each temperature.
   - From ln(I_D)-V_D plots obtain ideality factor(μ) at all temperatures.
2. The following to be done under lighted conditions:
   - Plot I_L-V_L and P_L-V_L characteristics under lighted condition at all temperatures.
   - Obtain fill factor (FF) for all temperatures and plot FF v/s temperature.
   - Plot V_D v/s temperature and V_{OC} v/s temperature.

2 Part 1

2.1 Circuit Design

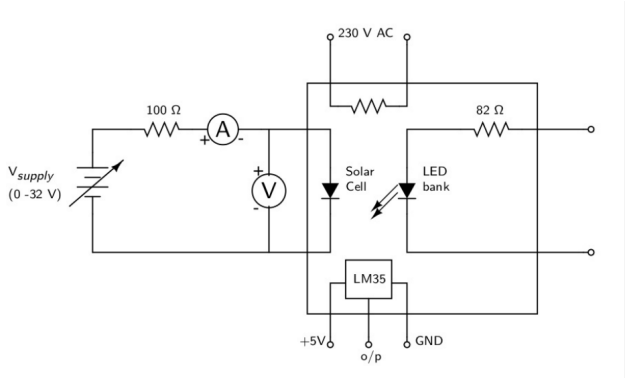
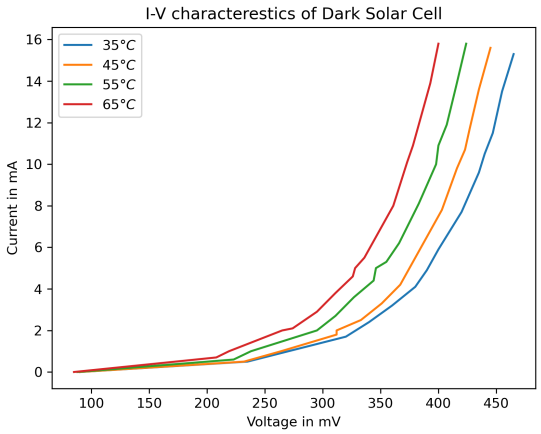
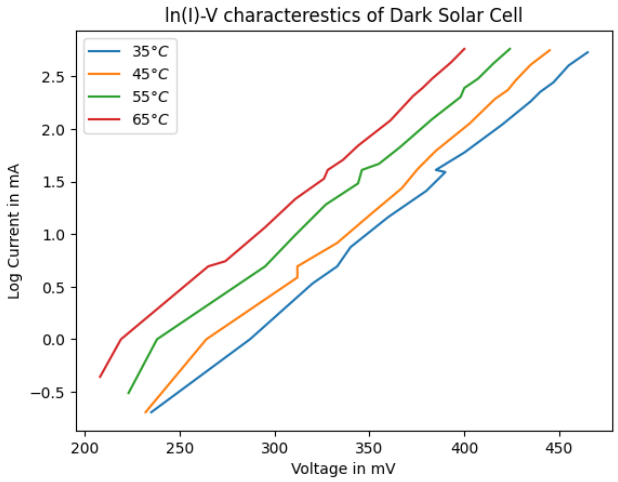


Figure 1: Circuit diagram for dark I/V characteristics

2.2 Plots





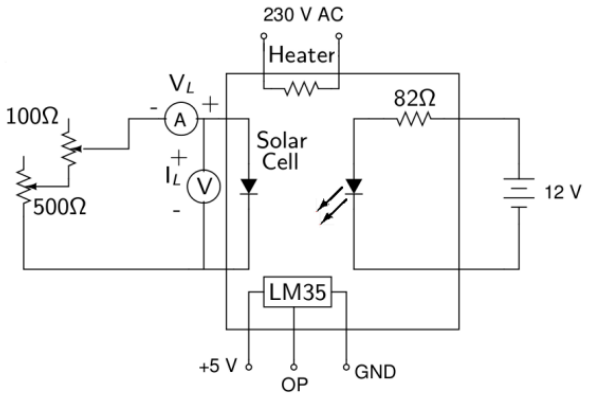
2.3 Observation Table

Temperature (C)	Vd (Voltage Drop)			η(Efficiency)	
	Id = 1 mA	Id = 2 mA	Id = 5 mA	Low Forward Bias	High Forward Bias
35	287	333	385	1.23	2.413
45	264	312	375	1.067	2.268
55	238	295	346	0.833	2.205
65	219	265	328	0.762	1.95

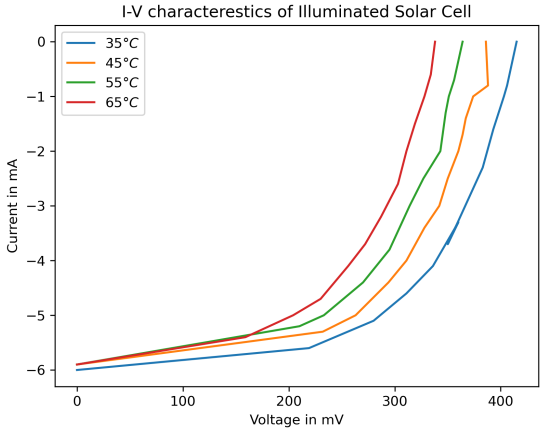
Table 1: Voltage Drop and Efficiency at Different Temperatures

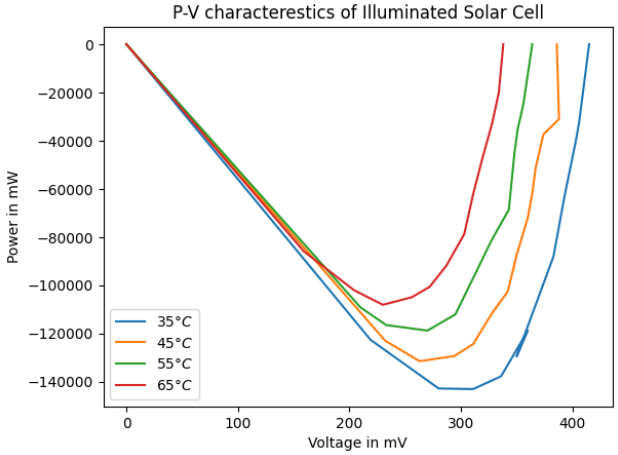
3 Part 2

3.1 Circuit Design



3.2 Plots



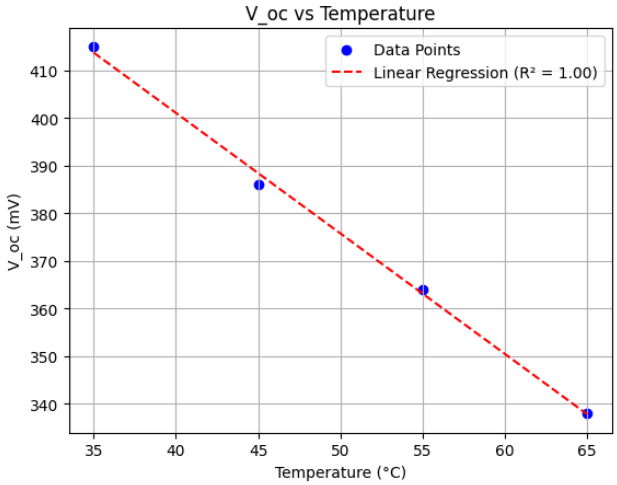


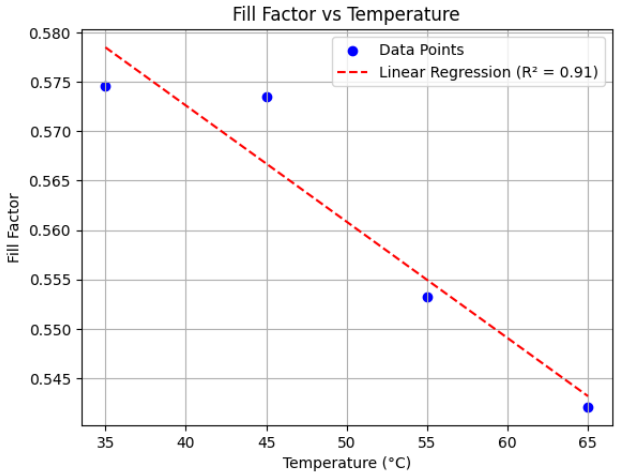
3.3 Values

Table 2: Solar Cell Parameters at Different Temperatures

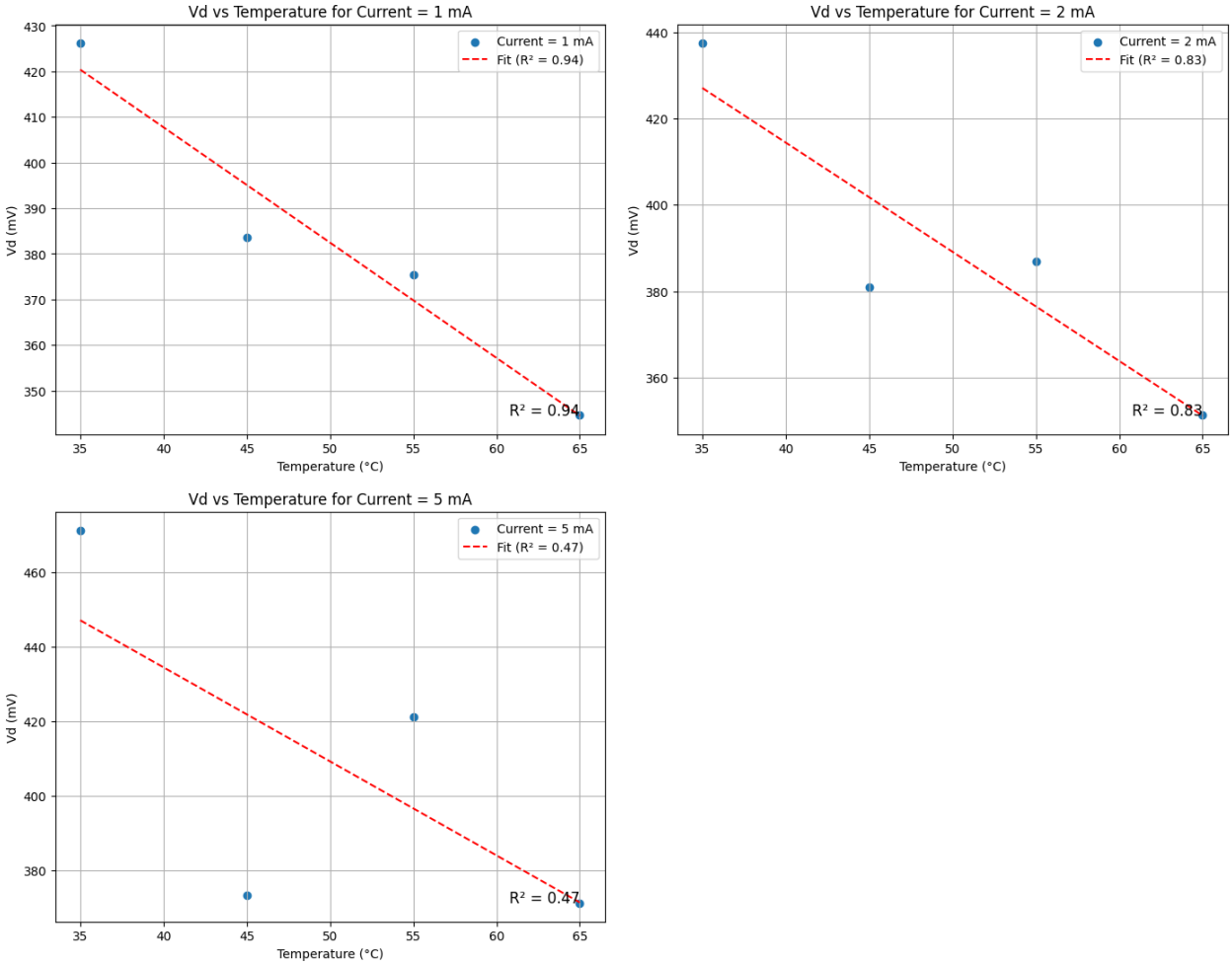
Temperature (°C)	V_{oc} (mV)	I_{sc} (mA)	V_{mp} (mV)	I_{mp} (mA)	Fill Factor (FF)
35	415	-6.0	311	-4.6	0.57454
45	386	-5.9	263	-5.0	0.57741
55	364	-5.9	270	-4.4	0.55318
65	338	-5.9	230	-4.7	0.54207

3.4 FF and V_oc Plots





3.5 V_d Plots



3.6 Comments

1. **Fill Factor (FF)**: It is observed that FF decreases with temperature because of increase in resistive loss and decrease in VOC

2. **Open-Circuit Voltage (V_OC)**: Decreases with temperature because increased thermal energy reduces the bandgap of the semiconductor, which lowers the voltage generated by the cell.

3. **Short-Circuit Current (I_SC)**: Increases with temperature because higher temperatures increase the intrinsic carrier concentration in the semiconductor, leading to more current being generated under short-circuit conditions.