Registration No:

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Total Number of Pages: 02

B.Tech/ Integrated Dual Degree (B.Tech and M.Tech) RBL2B002

2nd Semester Reg. / Back Examination: 2022-2023

Basic Electronics Engineering

AERO, AE, AUTO, BIOTECH, CHEM, CIVIL, CST, CSEAI, CSEDS, CSE, CSIT, CSEAIME, ELECTRICAL & C.E, EEE, ELECTRICAL, ECE, ETC, EIE, MANUTECH, MECH, MME, METTA, MINERAL, MINING, PLASTIC, IT

Time: 3 Hour Max Marks: 100 Q.Code: M383

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-III and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Answer the following questions: (2×10) a) Draw the equivalent circuit diagram of a diode. b) Draw V-I characteristics of the ideal zener diode. Write the applications of CE, CB, CC configuration of transistors. c) d) Define slew rate. Distinguish between BJT and FET. e) Draw the circuit diagram of an Op Amp differentiator. f) Write 4 applications of closed loop Op amp circuits. g) Draw logic gate symbols for NOR & X-OR gates. h)

i) Draw the OR gate using NAND gates.

j) $(127)_{10} = (?)_8$ and $(110110)_2 = (?)_{16}$

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 × 8)

a) Draw the VI characteristics of a diode and explain about its current equation.

b) Explain the principle of operation of a pnp transistor.

- c) What is a zener diode? Explain about its constructional details with applications.
- d) Explain the operation of a digital inverter.
- e) Explain about MOSFET and its characteristics.
- f) Explain the principle of operation of a JFET.
- g) Design a circuit which produces the output voltage $V_0 = 2V_1 6V_2 + 9V_3$ using Op-amp with minimum resistance value $50k\Omega$.
- h) Write the ideal characteristics of Op-amp, with its physical interpretation.
- i) Derive the output voltage of a differentiator circuit using Op-amp.

2(46)

- j) k) Design a full adder using NOR gates only.

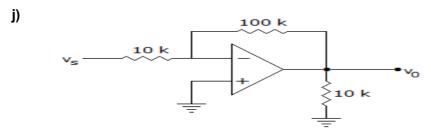
 Design a X-OR gate using minimum number of NOR gates.
- Explain about number systems and its conversion details. 1)

Part-III

Q3	Only Long Answer Type Questions (Answer Any Two out of Four) Explain various types of transistors, its constructional details and input output characteristics.	(16)
Q4	Explain in detail about CMOS, its constructional details, merits and applications.	(16)
Q5	What is an op-amp, its equivalent circuit, applications with neat circuits.	(16)
Q6	Design a half adder, full adder, full substractor with NAND gates only.	(16)
	314.40/06/20/3-10	
	14-19/08/2023-10	

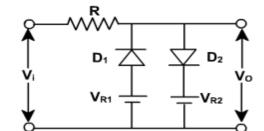
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15l 1 st Semester Back Examination 2017-18														BE2101
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BRANCH: AERO, CHEM, CIVIL, CSE, ECE, EEE, ELECTRICAL, ETC, IT, MECH, PE, PLASTIC, TEXTILE Time: 3 Hours														
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		111	e figure	S III UI	ie rigi	nt nai	nu ma	argii	1 1110	licate	e ma	rks.		
Q1		Answer the	following	g ques	tions:	multi	ple ty	pe o	r das	sh fill	l up t	ype		(2 x 10)
	a)	The thermal					amplifie	er ca	n be	preve	ented	by biasi	ng	
		the transistor						_ \/	(2	٩/ /	/ -0			
	b)	a) V _{CE} > V _{CC} /2 A diode is sa	,	V _{CE} < \ Iseful to								ts ß is		
	ω,	a) Less that		ioorar t			betwe					10 p 10		
		c) between				,	> 50							
	,										0/			
	d) e)	The maximum The frequence												
	f)	An Instrumer								casc	113		.	
	g)	Which of the	following	is not						on				
		a) junction c	•		_									
		b)charge stor c) depletion (е									
		d) channel le			1									
	h)	9's complem	ent of 68	is										
		The decimal	•											
	i)	What is mean a) Maximum					ran h	ne an	nlied	acro	ee a (diode wit	hout	
		breakdown	ieveise i	лаз ро	termai	WITICIT	Carro	с ар	pileu	acio	33 a (aloue wit	ilout	
		b) Maximum	forward I	oias po	tential	which	can b	е ар	plied	acro	ss a	diode wit	hout	
		breakdown	44:-1		حييالم	مائم مام	4			4:	-4-4-			
		c) Minimum p d) Maximum					to rea	acn c	onau	iction	state			
	j)	SR Flip flop					lip-flop	if						
00		A	6 - 11		4	04		4						(0 40)
Q2	a)	Answer the Define CMRI				Snor	t ansv	ver ty	ype					(2 x 10)
	b)	Difference be				wn an	d aval	anch	e bre	eakdo	wn.			
	c)	Derive the re												
	d)	Prove Demo					-	.	<i>(</i> 0=					
	e)	Draw the IEE Define Bark I	•	•		J, NO	ı, NOI	K & >	KUR	gates	S.			
	f) g)	Give the rela				I _{CEO} .								
	h)	Define the th												
	i)	What is com						?						

(5)



What is input impedance of op-amp circuit in the above figure?

Q3 a) With neat circuit diagram and waveforms, explain the working of a full wave bridge rectifier. Also discuss the PIV for center tapped Transformer.



Discuss the above circuit with sinusoidal input of peek to peek voltage 10 V, V_{R1} = 2V, V_{R2} = 1V, R= 1 Ω , and the diode are silicon diodes

Q4 a) The i/p to the Full wave rectifier is $v(t) = 200 \sin 50t$. If RL is 1kΩ and forward resistance of diode is 50Ω, find:

D.C current through the circuit

The A.C (rms)value of current through the circuit

The D.C output voltage

The A.C power input

b)

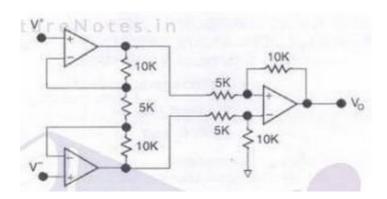
The D.C power output

Rectifier efficiency.

- b) Explain zener diode voltage regulator circuit with no load and with load. (5)
- Q5 a) With a neat circuit diagram, explain the Voltage Divider Bias circuit using approximate analysis. Also derive the equation of stability (S) for Voltage Divider Bias circuit.
 - b) What is a DC load line? Explain Base biased method with necessary equations. (5)
- Q6 a) Design a single stage common source amplifier for following specification. A_v = (10) 25, V_0 = 2.5 V
 - b) Derive the expression of 3 input summing amplifier. (5)
- **Q7** a) Convert $(1101101)_2 = ()_{10}$ and $(69)_{10} = ()_2$ (10) Convert $(1010111011110101)_2 = ()_{16}$ and $(FA876)_{16} = ()_2$
 - b) Write notes on Universal Gates. Also realize NOR using NAND gates only. (5)
- Q8 a) Factories the following Boolean equations $Y_1=AB'+AB$ $Y_2=(B+CA)+(C+A'B)$ Write a note on Full Adder. (10)
 - b) What is a RS Flip-Flop? Explain using its circuit diagram, logic symbol and truth table. (5)
- Q9 a) Write the principle and working of CRO with proper block diagram. (10)
 b) Write notes on Virtual ground
 Clamper circuit

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Regis	stratio	on No:													
Tota	l Nu	mber of P	ages	: 02											B.Tech BE2101
C	1 st Semester Back Examination 2017-18 BASIC ELECTRONICS BRANCH: AUTO, CHEM, CIVIL, CSE, ECE, EEE, EIE, ELECTRICAL, ETC, IT, MECH, MME, PE, PLASTIC, TEXTILE Time: 3 Hours Max Marks: 70 Q.CODE: B1202 Answer Question No.1 which is compulsory and any five from the rest. The figures in the right hand margin indicate marks.														XTILE
Q1	Answer the following questions: a) What will happen at the screen of CRO when time base voltage is given to Y-plate and a pulse is given to X-plate?														(2 x 10)
	b)	b) Define Slew rate and CMRR of an op-amp.													
	c) Establish the relation between α and β of a BJT.														
	d) Determine the DC resistance of a diode at V_D = -20V if its reverse saturation currents 1 μ A. (Take V_T =25 m V at room temperature)													uration	
	e)	Convert the decimal number -32 to its equivalent 1's complement and 2's complement form.													
	f) g)	Implement the logic function using NAND gate only: X=A' +BC. Define Ripple Factor. What is the value of ripple factor of half wave and full wave rectifier respectively?													
	h)	What is the	•			_			•						
	i) j)	Write down What is E counter de	3inary	Cou		•			•	•					
Q2	a)	Draw the feet explain the				erse b	ias c	harac	teristi	cs of	a p-n	junc	tion dio	de and	(5)
	b)	A transisto open circu emitter vol	uited.	Calc	ulate	the	uncti	on vo	ltage	V _C a	and \	/ _E , th	e colle		(5)
Q3	a) b)	Write the to Draw the expression	circui	ts of	integ	rator							_		(5) (5)
Q4	a)	a) Draw the circuit of an emitter follower. Derive the expression for an input										n input	(5)		
	b)	impendend What is N					-	•						g 4X1	(5)
		MUX		ļ	F= A'I	B'C' +	-ABC	+AB'C	C+A'E	C'.					
Q5	a)	What is the oscillation											•	•	(5)

b) Derive the expression for the output voltage and then find the magnitude of the output voltage of the op-amp circuits shown below:



- Q6 (a) A CE amplifier has mid frequency gain of 200. The upper and lower 3dB frequency of the amplifier is 10KHz and 100KHz respectively. A negative feedback of 10% is incorporated in the amplifier circuit. Find the new gain and new bandwidth after feedback?
 - (b) With suitable diagram explain the working principle of CRO. (5)
- Q7 Explain the operation of half wave and full wave rectifier with input and output waveform. Find the ripple factor in both cases. (10)
- Q8 Write short answer on any TWO:

 (5×2)

- a) ROM and RAM
- b) Voltage Divider Circuit
- c) Class-B Amplifier
- d) Small Signal Analysis

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Answer Ques	tion No.1	which	s com	ipulsoi	y and	l any	FIVE	from th	e rest.	
The	figures i	in the riç	ght ha	nd mai	gin ir	ndicat	te ma	rks.		

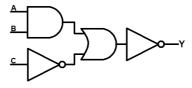
Q1 Answer the following questions: (2 x 10)

- Define PIV of a Diode.
- What do you mean by universal gates? Name two universal gates used.
- c) Perform the following subtraction using 2's complement method. $(47)_{16}$ - $(68)_{10}$
- d) Construct an AND gate using NOR gate.
- Write the difference between flip flop and latch.
- State Barkhausen Criterion of oscillation.
- g) How an ideal diode acts as a bistable switch?
- **h)** Convert (25.625)₁₀ into equivalent Binary.
- Prove the Boolean Identity, (A+B) (A+C)=A +BC
- How a BJT can be used as a Switch?
- Q2 a) With neat sketches explain the operation of a center tapped full wave rectifier. (5)
 - With suitable diagram illustrate the basic operation of a CRO.
- (5)

(5)

(5)

- Q3 a) Convert the given expression into canonical POS form Y=(A+B)(B+C)(A+C)
 - **b)** A negative feedback of gain β =2.5X10⁻³ is applied to an amplifier of open loop (5) gain 1000. Calculate the change in overall gain of the feedback amplifier if the open loop gain of the amplifier is reduced by 25%.
- Q4 a) Write the Boolean expression for this logic below?

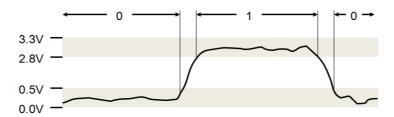


b) Determine I, V_1 , V_2 and V_0 for the following circuit.

(5)

(5)

Q5 a) Define logic 1 and logic 0? In a particular digital system we are getting some output voltages like 0.2V,0.35V,0.45V,1.2 V,2.3V,2.9V,3.2V. Specify which one is logic 1 and logic 0.(follow the diagram for your reference.)



- **b)** Why CE configuration is most popular in amplifier circuits?
- th **(10)**

(5)

- Q6 Discuss the current amplification factor in different configuration of BJT with circuit diagram. Compare their relationship with one another.
- Q7 A 50Ω load resistance is connected across a half wave rectifier. The input supply voltage is 230V (rms) at 50Hz. Determine the dc output voltage, peak-to-peak ripple in the output voltage and output ripple frequency. Also find out the PIV of the diode used. (10)
- Q8 Write short answer on any TWO: (5 x 2)
 - a) Zener and Avalanche breakdown
 - **b)** Positive Clamper circuit
 - c) Full adder circuit.

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B.Tech RBL1B002

1st Semester Regular/Back Examination 2019-20 BASIC ELECTRONICS ENGINEERING

BRANCH: AEIE, AERO, AG, AUTO, BIOMED, BIOTECH, CHEM, CIVIL, CSE, CST, ECE, EEE, EIE, ELECTRICAL, ELECTRICAL & C.E, ELECTRONICS & C.E, ENV, ETC, FASHION, FAT, IEE, IT, ITE, MANUFAC, MANUTECH, MARINE, MECH, METTA, METTAMIN, MINERAL, MINING, MME, PE, PLASTIC, PT, TEXTILE

Max Marks: 100 Time: 3 Hours Q.CODE: HRB713

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Only Short Answer Type Questions (Answer All-10)

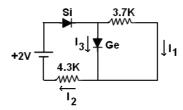
(2 x 10)

- a) Determine the dc resistance of a diode at V_D =-20V if its reverse saturation current is $1\mu A$ (The V_T =25 mv at room temperature)
- b) Give at least two examples of semiconductor materials which are used for LED.
- c) Why BJT is called current controlled device?
- d) Why collector is made larger than emitter and base?
- e) Take a typical open loop differential configuration and derive the output for the mentioned two inputs.
- f) What is the main constructional difference between D-type and E-type MOSFET?
- g) The reverse gate voltage of JFET when changes from 4.4V to 4.2V, the drain current changes from 2.2 mA to 2.6 mA. Find out the value of transconductance of the transistor.
- **h)** What is positive and negative logic?
- i) State the two Demorgan's theorem.
- j) What is virtual Ground?

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- a) Derive the relation between trans-conductance (g_m) and Drain current I_D and plot the curve between them.
- b) Develop the basic Diode equation. Using the same find the percentage increase in reverse saturation current of a PN junction diode if the temperature is increased from 25°C to 50°C.
- c) A diode is operated at room temperature with I_S =10⁻¹⁰ A and η =2. i)What is the diode current I_D , if the voltage across the diode is V_D =0.65 V? ii)What voltage V_D is required for a diode current of 200 μ A.
- d) Compare the Si diode and Ge diode?
- e) Determine l_1 , l_2 and l_3 for the circuit shown in the following figure.



- f) What is pinch off voltage in JFET? Define pinch off voltage with respect to different characteristics of an n-channel JFET. Is the drain current affected by V_P? Justify your answer.
- **g)** Explain the basic operation of a full adder using Truth table. Implement the full adder using half adder.
- h) $Y = \overline{A}B + C$, Implement it using NOR gates only.?
- i) Derive the gain equation with feedback by taking an inverting opamp closed loop configuration.
- j) Prove that $\overline{AB} + \overline{BC} + \overline{CA} = \overline{A} \, \overline{B} + \overline{B} \, \overline{C} + \overline{A} \, \overline{C}$
- **k)** Explain with neat sketch , how transistor can be used as a switch?
- I) Explain the construction and operation of a CMOS Inverter.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- A silicon diode having 20 Ω internal resistance is used as half wave rectifier. If the applied input voltage is 50 sin100πt and load resistance is 800 Ω , then find
 - a) Im, Idc and Irms
 - b) Output frequency and ripple factor
 - c) AC input and output power
 - d) efficiency
- Q4 Prove that voltage divider bias is the best type of biasing than all other types of biasing. (16)
- Discuss the various ideal characteristics of opamp? Determine the output voltage of an op-amp for input voltages of V_{i1} =150 μV and V_{i2} =140 μV . The amplifier has a differential gain of **Ad**=4000 and the value of CMRR is 10⁵

Q6 F=xy'z+x'y'z+w'xy+wx'y+wxy

(16)

- a). Obtain the truth table table of F.
- b).Draw the logic diagram, using original Boolean expression.
- c). Use Boolean algebra to simplify the function to a minimum number of literals.
- d)..Draw the logic diagram, from the simplified expression

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B.Tech 15BE2101

1st Semester Back Examination 2019-20 BASICS OF ELECTRONICS

BRANCH: AEIE, AERO, AUTO, BIOMED, BIOTECH, CHEM, CIVIL, CSE, ECE, EEE, EIE, ELECTRICAL, ENV, ETC, FASHION, FAT, IEE, IT, ITE, MANUFAC, MANUTECH, MARINE, MECH, METTA, METTAMIN, MINERAL, MINING, MME, PE, PLASTIC, TEXTILE

Max Marks: 100 Time: 3 Hours Q.CODE: HB928

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part- I

Q1 Only Short Answer Type Questions (Answer All-10)

(2 x 10)

- a) FET is Current or Voltage control device. Justify.
- b) Is JFET is more advantageous than the BJT? Justify
- c) Differentiate zener and avalanche breakdown.
- d) What is transducer? Mention any four characteristics of a transducer.
- e) Define CMRR and Slew rate for Op-Amp.
- f) State the difference between Latch and Flip-flop.
- g) Convert a decimal number 197.72 to binary.
- h) Find the compliment of A+BC.
- i) Draw a binary adder using logic gates.
- j) Draw only the block diagram of Analog communication.

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- a) Draw and explain the V-I characteristics of silicon diode.
- **b)** What is the need for capacitor filter? For a half-wave rectifier explain the operation of C-filter.
- c) Sketch the transistor input and output characteristics of CE configuration and briefly explain the three regions of operation.
- **d)** Design a voltage regulator using zener diode to meet the following specification; Unregulated voltage=20V, V₀=10V, load current is 0-20mA, I_{2min}=10mA, I_{2max}=100mA
- e) Draw the PNP transistor circuit in CB configuration. Sketch the output characteristics. Indicate active, saturation and cut off regions. Briefly explain the nature of these curves.
- f) How JFET has been constructed? Explain the principle of operation of JFET at different values of V_{GS} and V_{DS} .
- g) A half wave rectifier from a supply 230V, 50Hz with step down transformer ratio 3:1 to a resistive load of $10K\Omega$. The diode forward resistance is 75Ω and transformer secondary is 10Ω . Calculate DC current, DC voltage, efficiency and ripple factor.
- h) Subtract (1000.01)₂ from (1011.10)₂ using 1's and 2's compliment method.
- i) Explain the working of clocked R-S flip flop with a suitable circuit, symbol, truth table, input-output wave forms considering positive edge triggered R-S flip flop.
- i) Implement EX-OR gate using NAND gates and NOR gates.
- **k)** Explain the construction and principle operation of LVDT.
- I) Explain the frequency modulation with necessary waveforms. Bring out the difference between AM and FM.

Part-III

Q3	a) b)	Only Long Answer Type Questions (Answer Any Two out of Four) State and prove Demorgan's theorem. Show that: a. $A\overline{B}C + B + D\overline{B} + AB\overline{D} + \overline{A}C = B + C$	(7) (3 × 3)
		b. $\underline{AB + A(B + C)} + B(B + C) = B + AC$ c. $\overline{\overline{AB} + \overline{A} + AB} = 0$	
Q4	a) b)	What is modulation? What is need of modulation? Design a adder circuit using Op-Amp to obtain an output expression $V_0 = -(0.1V_1 + 0.5V_2 + 20V_3)$. Where $V_1, V_2 \& V_3$ are the inputs. Select $R_f = 10K\Omega$	(4) (6)
	c)	Find out the expression for the rms voltage and PIV for the full wave bridge rectifier.	(6)
Q5	a) b)	Write principle of CRO and working of CRO with proper block diagram. What is a clamper circuit? Explain a positive clamper circuit with neat diagram.	(10) (6)
Q6	a) b)	Write the note on : Digital Multimeter AD converter	(8) (8)

(5)

(5)

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BASIC ELECTRONICS BRANCH: AEIE, AERO, AUTO, BIOMED, BIOTECH, CHEM, CIVIL, CSE, ECE, EEE, EIE, ELECTRICAL, ENV, ETC, FASHION, FAT, IEE, IT, ITE, MANUFAC, MANUTECH, MARINE, MECH, METTA, METTAMIN, MINERAL, MINING, MME, PE, PLASTIC, TEXTILE Time: 3 Hours Max Marks: 70 Q.CODE: C1179 Answer Question No.1 which is compulsory and any five from the rest. The figures in the right hand margin indicate marks. Answer all parts of a question at a place.															
Q1	a) b) c) d) e) f) g) h) i)	Answer the What is the i Write down to Derive the e The gain of a Write down to Realize a No Convert the How BJT ac State the cha	meanii he ad xpress a certa he fou DR ga decim ts as a	ng of vantagion for amount of the front of t	CMRI ges of procoll polifie lication NA nber ch?	R of a need of a	an Opegative curre DdB. Ef a dictate. Dits of the dictate of the dictate of the dictate of the dictate of the dictate.	e feed ont for Expre ode.	dback a CE ss it n	trans iumer	sistor. rically	'.	nent for	m.	(2 x 10)
Q2	a) b)	Explain the of Explain the output wave	operat	ion o	•	•								nput-	(5) (5)
Q3	a) b)	Draw circuit Derive the e Draw the blo	xpress	ion fo	r the	gain	of an	inver	ing a	mplifi	er.			·amp.	(7) (3)
Q4	a) b)	What are th oscillation ar What is the voltmeter.	nd also	the o	condi	tion o	f osci	llatior	in a	RC pl	hase	shift o	scillato	or.	(5) (5)

The open loop gain of an amplifier changes by 5%. If 10dB negative feedback

What is active, saturation and cut-off region of a transistor? Explain with

is applied, calculate percentage change of the closed loop gain?

Q5 a)

b)

necessary diagram.

Q6	a)	Implement the following function using NOR gate only F(A, B, C, D)= (A+C) (B+D).	(7)
	b)	Draw the physical structure, drain characteristics, transfer characteristics and circuit symbol of an n-channel depletion type MOSFET.	(3)
Q7		A crystal diode having an internal resistance r_i =10 Ω is used for center tapped full wave rectification. If the applied voltage is V=50 sin(π t) and the load resistance is R _L = 1K Ω , determine the followings i) Draw the input and output voltage and current waveforms ii) The efficiency of the circuit. iii) The ripple factor.	(10)
Q8		Write short answer on any TWO :	(5 x 2)
	a)	CRT	
	b)	SR Flip-Flop	
	c)	Zener diode as voltage regulator	
	d)	Static and Dynamic Memories	

(5)

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	2 nd Semester Back Examination 2018-19 BASIC ELECTRONICS BRANCH: CHEM, CIVIL, CSE, ECE, EEE, ELECTRICAL, IT, MECH Time: 3 Hours Max Marks: 70 Q.CODE: F112 Answer Question No.1 which is compulsory and any FIVE from the res The figures in the right hand margin indicate marks.														
Q1	Answer the following questions: a) What do you mean by break region of a diode?														
	•	What do you Why the gate frequency?		•	U					high	and	very	low		
	-	State and ex	•										10		
	a) e)	What is the difference between combinational and sequential circuit? Why common collector configuration is called an emitter follower circuit? Comment.													
	f)	Write down the relationship between I_{CO} and I_{CEO} .													
	g)	Compare th and bridge t		_			lvanta	ages	betw	/een	cente	er- ta	pped		
	h)	What is the frequency?	relation	nship	betwe	en t	he p	eriod	of a	a wa	vefor	m an	d its		
	i)	What do you digital logic i		, .	ital lo	gic ir	verto	ors? N	Menti	ion tv	vo IC	s use	ed as		
	j)	Define CMR	R and S	lew ra	te of a	an Op	o-Am	р. Ме	entior	n its s	signifi	cance	Э.		
Q2	a)	What is Lissignal? Staroscilloscope	te and	explai	n the	fun	ction	of t	he s	weep	sig	nal i	n an	(5)	
	b)	•	tal contro							•	_	•	•	(5)	
Q3	a)	Draw and transistor.	explain	a sm	all si	gnal	high	frec	quend	су С	E m	odel	of a	(5)	
	b)	Explain the output wave	•	n of a	a full y	wave	brid	ge re	ectifie	er wit	h its	input	and	(5)	
Q4	a)	What do y advantages system is us	of actu	al and	Hex	adec			-					(5)	

b) How the transistor can be used as an amplifier in CE configuration?

Explain with proper diagram.

Q5	a)	What is a signal generator? Explain the operation of a signal generator with a neat block diagram.	(5)
	b)	Differentiate between static and dynamic RAM.	(5)
Q6		Implement a full adder circuit using two 4:1 multiplexers.	(10)
Q7		Draw and explain the circuit of a basic differentiator. What are the limitation of this circuit and how these are overcome in practical differentiator circuit?	(10)
Q8	a) b) c)	Write short answer on any TWO: Small signal analysis. Feedback amplifier. AF signal generator.	(5 x 2)

Registration No :					

B.Tech RBL2B002

2nd Semester Regular / Back Examination 2018-19
BASIC ELECTRONICS ENGINEERING
BRANCH: AEIE, AERO, AG, AUTO, BIOTECH, CIVIL,
CSE, ECE, EEE, ELECTRICAL, ENV, ETC, IT, MANUTECH, MECH,
METTA, METTAMIN, MINERAL, MINING, MME, PLASTIC

Max Marks: 100 Time: 3 Hours Q.CODE: F358

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Only Short Answer Type Questions (Answer All-10)

(2 x 10)

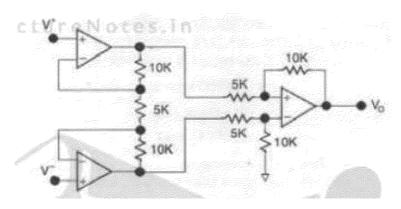
- a) What is Avalnche break down?
- b) Define slew rate and PSRR of op-amp.
- c) Determine the DC resistance of a diode at V_D = 20V if its reverse saturation current is 1 Micro-amp. (Take V_T = 25 milli-amp at room temperature)
- d) What do you mean by three state gate? What is its importance in combinational circuit?
- e) Write down the advantages of negative feedback.
- f) Write down the excitation equation of S-R flip-flops. What is its limitation?
- g) State the relation between I_{CO} and I_{CEO} .
- h) Differentiate between combinational logic and sequential logic circuit.
- i) What is counter? How many flip-flops are required to design a decade counter?
- i) What is the significance gain bandwidth product?

Part- II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of (6 x 8) Twelve)

- a) Explain the operation of P-N junction diode with V-I characteristics.
- b) A crystal diode having an internal resistance ri= 20 ohms is used for full wave rectification. If the applied voltage is V=50sin 2t and the load resistance is RL= 800ohms, determine the following
 - i) I_m , I_{dc} I_{rms} of output
 - ii) a.c power input and dc power output
 - iii) Ripple factor
- c) Draw the circuit of an emitter follower. Derive the expression for input impedance. Mention at least two applications of an emitter follower.
- d) What is Dc load line? Explain base biased method with necessary equation.

e)



Derive the expression for the output voltage and the find the magnitude of the o/p voltage of the op-amp shown above.

- f) What is CRO? Draw the block diagram of CRO and explain its operation.
- g) In RC coupled amplifier, the output voltage is 5V for a sinusoidal input of 5mV. Determine the voltage gain at mid band frequency and at half power frequencies.
- h) Write Short notes on Universal Gate. Also realize NOR using NAND gate only.
- i) What is Flip-Flop? Name the types of Flip-Flop. Explain J-K flip- flop using circuit diagram, truth table and excitation equation.
- j) Explain the ideal characteristics of electronic instrument.
- k) Explain the principle of oscillator circuit. Mention two conditions that must be fulfilled by oscillator circuit.
- I) What is POS and SOP of Boolean expressions? Simplify the following expression using Boolean identity $F(A,B,C,D) = \sum_{m} (4,5,6,7,12,13,14)$.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3 Explain the operation of half wave and full wave rectifier with its input and output (16) waveform. Find the ripple factor in both cases.
- How does the construction feature of MOSFET differs from JFET?

 A JFET operates in the linear region with a constant drain voltage of 1V. When the gate voltage is 2V, a drain current of 10 m amp. Flows, but when the gate voltage is changed to 1 V, the drain current becomes 22.8 m amp. Find the pinch off voltage of the device, the channel resistance for the gate voltage of 0 V.
- With a neat circuit diagram, explain the voltage divider bias circuit. Also derive the equation of stability (S) for voltage divider and self-bias circuit.
- Q6 Derive the of 3-input summing amplifier. Design a single stage common source (16) amplifier for following specification Av= -25 Vo= 2.5V.

B.Tech **RBL2B002**

2nd Semester Regular / Back Examination: 2021-22 BASIC ELECTRONICS ENGINEERING BRANCH(S): AEIE, AERO, AME, BIOTECH, CIVIL, CSE,

CSEAI, CSEAIME, ECE, EEE, ELECTRICAL, ELECTRICAL & C.E, ELECTRONICS & C.E, ENV. ETC. IT, MANUTECH, MECH, METTA,

MINERAL, MINING, MME, PLASTIC, PT

Time: 3 Hour

Max Marks: 100

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-III and any two

The figures in the right hand margin indicate marks.

Q1 Answer the following questions: Part-i

Draw V-I characteristics of the ideal diode (i.e., $V_v=0$ V, $R_f=0$ Ω). (2 ×10)

Draw circuit symbol for Zener diode and pnp transistor.

Write the diode equation and based on it explain how the diode acts as a

(d) Distinguish between JFET and MOSFET

Draw the circuit diagram of an integrator.

Write any four characteristics of the ideal op-amp.

Draw the circuit of a full adder circuit.

 $(127)_{10} = (?)_2$ and $(10110)_2 = (?)_{10}$

Draw logic gate symbols for NCR & X-NOR gates.

Part-II Only Focused-Short Answer Type Questions- (Answer Any Eight out of Q2

a) Explain the principle of operation of a pn junction diode.

Explain about the output characteristics of a CE transistor.

Draw the VI characteristics of Zener diode and explain about it.

Distinguish between BJT and JFET.

Explain the principle of operation of a MOSFET.

Explain the operation of a digital inverter.

Design a circuit which produces the output voltage V₀= 2V₁+8V₂+4V₃ using Op-amp with minimum resistance value 100KΩ.

Derive the output voltage of an integrator circuit using op-amp.

What is open loop and closed loop op-amp, explain in detail.

What is a combinational logic circuit, explain with example. Design a NAND gate using diodes. I) Part-III Only Long Answer Type Questions (Answer Any Two cut of Four) Explain various types of diodes, its constructional details and V-I (16)Q3 characteristics. Explain various types of field effect transistors, its constructional details and (16)Q4 applications. What is an op-amp, explain about its practical applications with near (16)Q5 çir suits. Design a half adder and full adder with NOR gates only. $\{16\}$

j) Design a X-NOR gate using minimum number of NAND gates.

	Registration No :											
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B.Tech. 15BE2101

2nd Semester Back Examination 2017-18 BASICS OF ELECTRONICS BRANCH: AEIE, AERO, AUTO,

BIOMED, BIOTECH, CHEM, CIVIL, CSE, ECE, EEE, EIE, ELECTRICAL, ENV, ETC, FASHION, FAT, IEE, IT, ITE, MANUFAC, MANUTECH, MARINE, MECH, METTA, METTAMIN, MINERAL, MINING, MME, PE, PLASTIC, TEXTILE

Time: 3 Hours Max Marks: 100 Q.CODE: C920

Answer Part-A which is compulsory and any four from Part-B.
The figures in the right hand margin indicate marks.
Answer all parts of a question at a place.

	Answer all parts of a question at a place.													
		Part – A (An	swei	r all the questions)										
Q1		Answer the following questions:			(2 x 10)									
	a)	In a BJT with β = 100, α equals												
		(a) 0.99	(b)	99										
		(c) 1	(d)	1.01										
	b)	Avalanche breakdown results basic	cally	due to										
		(a) impact ionisation												
		(b) strong electric field across the	junct	tion										
		(c) emission of electrons												
		(d) rise in temperature												
	c)	For an Op-amp with negative feedly	oack,	, the output is										
		(a) equal to the input	(b)	increased										
		(c) fed back to the inverting input (d) fed back to the noninverting input												
	d)	d) Which number system has a bas	se of	16										
		(a) Decimal	(b)	Octal										
		(c) Hexadecimal	(d)	Binary										
	e)	e)gates are known	as ı	universal gate.										
	f)			current of 300 mA to a load of 1 Kohm.										
		When the Load is changed to 100												
		(a) 3 Amp	٠,	300 mAmp										
		(c) 30 mAmp	(d)	600 mAmp										
	g)	The Op-amp can amplify												
				d.c. signals only										
		(c) both a.c. and d.c. signals												
	h)	, ,												
		• •		Negative										
		(c) Neither positive nor negative	٠,											
	i)	The forward voltage drop across a												
		(a) 1.2V	٠,	0.3V										
		(c) 0.7V	` '	1.0V										
	j)	The doping level in a zener diode is												
		(a) the same as	٠,	less than										
		(c) more than	(d)	none of the above										

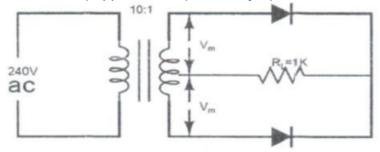
Q2 Answer the following questions: short answer types:

(2 x 10)

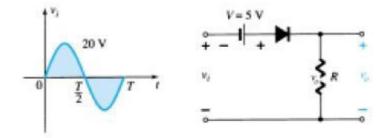
- a) Give the load line of a BJT amplifier if $v_{cc} = +9v$ and $R_c = 1.8K\Omega$.
- b) Explain Early effect of BJT.
- c) Differentiate between zener breakdown and avalanche breakdown.
- d) What is Bark Hausen criteria?
- e) Difference between Practical Op-amp and Ideal Op-amp.
- f) Draw the V-I characteristic of Zener diode.
- g) Implement Half Adder using AND and OR gate.
- h) State De-Morgan's theorem.
- i) What is the relationship between period of waveform and frequency?
- j) What will appear on the screen of CRO when time base voltage is given to Y-plate and pulse is given to X-plate?justify?

Part - B (Answer any four questions)

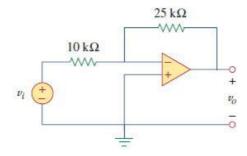
- Q3 a) With neat circuit diagram explain the working principle of Full wave center-tapped transformer rectifier and derive the expression for its efficiency. (10)
 - b) In the center tap fullwave rectifier shown below, find i)peak, average, rms value of load current ii) ripple factor iii) efficiency iv)PIV



- Q4 a) With neat diagram explain the formation of a potential barrier in a p-n junction and show the polarity of the Barrier potential and draw the V-I characteristic of p-n junction diode. (10)
 - b) Determine the output waveform of the circuit given below. Assume ideal (5)



- Q5 a) Realize Op-amp as adder, subtractor, buffer, integrator and differentiator (10) circuit.
 - **b)** In the fig. given below if $v_i = 0.5V$, calculate the output voltage v_o and the current in $10K\Omega$ resistor.



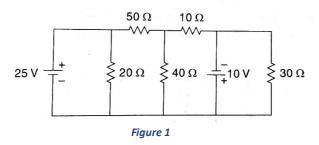
- Q6 a) With a neat diagram explain the basic operation of bipolar junction transistor. (10) Draw its input and output caracteristic and briefly explain why biasing is needed?
 - **b)** Explain how BJT is converted to hybrid-π model and why modeling is needed? (5)
- Q7 a) With a neat block diagram explain the operation of cathode ray tube(CRT), and how phase measurement can be done using an Oscilloscope through the Lissajous metod?
 - b) Write down a short note on Wien-Bridge Oscillator. (5)
- **Q8** a) Realize Full adder using NAND Gate, NOR Gate and Multiplexer. (10) b) Perform the following conversion: i) $(142.623)_{10} = (\)_2$ ii) $(BPUT.2018)_{16} = (\)_8$ iii) $(BPUT.2018)_{16} = (\)_{10}$ iv) $(100100111001.1001)_2 = (\)_{16}$
- Q9 a) State De-Morgan's theorem. Convert the Boolean function $Y = A\overline{B} + BC + \overline{AC}$ into canonical forms. (10)
 - b) Apply De-Morgan's law and minimize the expressions: i) \overline{ABCD} ii) $\overline{A+B+C+D}$ iii) $\overline{\overline{ABCD}}$ iv) $\overline{A+B+\overline{C}}+D(\overline{E+F})$

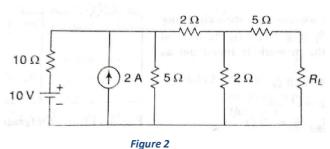
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Q1		Answer the f	برمالت			A (Ans						tha	hlanka:	(2 x 10)
QI	a)	The resistance												(2 X 10)
	uj	length. The n					COIIII	1. 1111	3 WIIC	, 13 31	Cloric	o to	its double	
		(i) RΩ		RΩ		, (iii) 2l	R Ω	(i	v) R/2	2 Ω				
	b)	The average									nplete	e cycl	e is	
	-	$(i)E_{rms}I_{rms}$	(ii) z			(iii)E _m			v) (E _n			-		
	c)	Binary repres												
		(i) 10001	` '	1001		(iii)11			v)101	10				
	d)	The current g		BJI					,	f	thaaa			
	e)	(i) α The rms value	(ii)β	00 V		γ (iii)		(i						
	f)	The rms value The ripple fac	tor of	บบ v half เ	Nave	uppiy rectifi	or is		aı	nd for	full w	/ave i	rectifier is	
	g)	The mobility of												
	h)	A three Phase											metrical	
	-	three phase 4												
		leads 60 degr	ee ah	nead o	of the	corre	spon	ding p	hase	volta	ge. T	hen li	ine current	
		will be	_				. 450	_				-	- 0	
	i)	A two pole DO												
		pole is 1mWb connected an								uilig i	s		_ 101 Iap	
	j)	According to								0 =				
	3/	7 toooraning to	.00.0	arr ia		•		_						
Q2		Answer the f	ollow	ing c	quest	ions:	Shor	t ans	wer t	ype:				(2 x 10)
	a)	Three resistor												
		star network,	conve	ert it i	nto de	elta ne	etworl	k and	find c	out its	equi	ivaler	nt delta	
	1. \	resistance.												
	b)	Define Unilate						a	رز) در درزار در	04.05	/;;\ 1	10 10	2404	
	c) d)	Convert follow Draw the circ								04.00	3 (11) 1	10.10	J 10 1 ₂	
	e)	State De mor		_		iii wa	vc icc	Junci.						
	f)	Calculate the				capa	citor c	of 1 µl	in s	eries	with a	a 1M :	Ω resistance	9
	,	to be charged												
	g)	What is appar	rent p	ower	, activ	e pov	ver ar		ctive	powe	r?			
	h)	What is P and	d N ty	pe se	micor	nducto	or?							

- A zener diode acts as a voltage regulator. Explain the meaning of the statement.
- j) What is the working principle of DC machines?

Part – B (Answer any four questions)

Q3 a) Find the current through 40 Ω resistor using superposition theorem for the circuit shown in figure 1. (5)





- b) State the maximum power transfer theorem and obtain the maximum power transferred to R_L in the circuit shown in Figure 2. And also find the value of R_L
- **Q4** a) Explain the principle of operation of a transformer in detail and Derive the Emf equation of single phase transformer. (5)
 - b) Draw the phase voltage and line voltage phasor diagram for 3-phase star connected balanced system. A 3-phase 230 V load has power factor of 0.7.
 Two wattmeter are connected to measure the power which shows the input to be 10 kW. Find the readings of each wattmeter.
- Q5 a) Explain the operation of a full wave bridge rectifier with relevant waveforms. (5)
 - b) Explain the V-I characteristics of a P-N junction diode when it is connected in forward bias and reverse bias. A PN junction diode gives a current of 50 mA at a room temperature of 20 dergee C when the forward bias voltage is 200mV. Determine (a) the saturation current with a negative bias (b) the diode current when room temperature is 30 degree C, and (c) diode current at a forward bias voltage.
- Q6 a) Explain the full adder circuit with its expression and truth table.
 b) List out all the basic logic gates and universal gateswith its logic symbols and truth table. And generate AND function, OR function and NOT function using any one Universal gate.

- Q7 a) A series circuit has R= 5 Ω, L= 13 mH and C=140 μF and is supplied with 230 v, 50 Hz single phase. Find (i) Impedance (ii) current (iii) power (iv) power factor of the circuit.
 - b) An iron ring made up of three parts, $I_1=12$ cm, $a_1=6$ cm², $I_2=10$ cm, $a_2=5$ cm², $I_3=8$ cm and $I_3=4$ cm². It is surrounded by a coil of 200 turns. Determine the exciting current required to create a flux of 0.5 mwb in the iron ring .[Given μ 1=2670, μ 2= 1055, μ 3= 680]
- Q8 a) Simplify the function $Y = (A+B)(\overline{A} + C)(B+C)$ and design the circuit for simplified function using basic logic gates. (8)
 - $\begin{array}{ll} \textbf{b)} & \text{Determine (i) } I_{\text{C(sat)}}(\text{ii) } I_{\text{C}} \\ & \text{(iii) } V_{\text{C}}(\text{iv})V_{\text{E}} \text{ and } \text{ (v)}V_{\text{CE}} \text{ for the circuit shown in figure 3} \,. \end{array}$

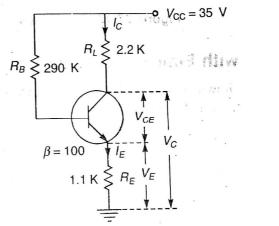


Figure 3

Q9 Write a short note on any THREE:

 (5×3)

(7)

- a) Magnetic material and B-H curve
- **b)** Different methods of transistor biasing.
- c) Generation and distribution of AC Power
- d) Transients in RL circuit with DC excitation
- e) circuit elements and their characteristics

Registration No :										
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B.Tech PEN2B101

2nd Semester Back Examination 2018-19 ELECTRICAL & ELECTRONICS ENGINEERING

BRANCH: AEIE, AERO, AUTO, BIOTECH, CHEM, CIVIL, CSE, ECE, EEE, EIE, ELECTRICAL, ETC, IT, MANUTECH, MECH, METTA, MINERAL, MINING, MME, PE, PLASTIC, PT, TEXTILE

Max Marks: 100 Time: 3 Hours Q.CODE: F1012

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right-hand margin indicate marks.

Part- I

Q1 Only Short Answer Type Questions (Answer All-10)

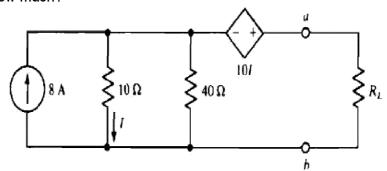
(2 x 10)

- a) What are the internal resistances of an ideal (i)10v voltage source and (ii) 7.5A current source?
- b) What is duality principle? Give two examples.
- c) What is the relation between the line voltage and phase voltage of a 3-phase delta connection circuit?
- d) How diode can be used as a linear element in a circuit?
- e) What is slew rate of an op-amp?
- f) Draw the energy band diagram of a n-type semiconductor
- g) What do you mean by 'ratio correction factor' in an Instrument Transformer?
- h) Find the percentage of error for a reading of 25 mA of an ammeter provided the ammeter range is 0-50mA has an error 0f 2%.
- i) Find the resolution of a voltmeter for a voltage measurement of $4\frac{1}{2}$ digits.
- j) What is the semiconductor material used for the LED and how the different colors are obtained?

Part- II

Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

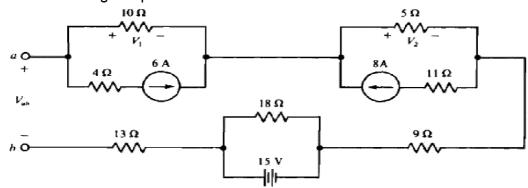
a) For the circuit given below what is the value of R_L for which maximum power transfer will be there and how much?



b) Draw the simplified hybrid π model of a common emitter configuration of BJT and find out the different h-parameters.

Q2

c) Determine the voltage drop across terminals a and b

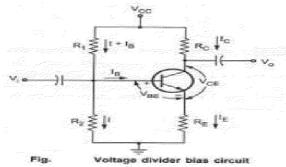


- d) A PMMC instrument has a coil of dimension 10mm X 8mm. The flux density in airgap is 1x10⁻³wb/m² and spring constant is 0.3x10⁻¹⁶N-m/rad. Determine the number of turns required to produce angular deflection of 45⁰ when 4A current is flowing through the coil.
- e) Prove that (i) A+AB=A (ii) A+ \overline{A} B =A+B
- f) Minimize the following expression using Boolean Algebra $F(A,B,C,D)=\sum (1,3,4,6,7,10,11,12,14)$
- g) What is the working principle of a current transformer? Draw and explain its phasor diagram.
- h) Realize a full adder using half adders with truth table.
- i) Explain the working of Single-phase transformer.
- j) Discuss briefly about the Magnetic materials and B-H curves.
- k) How the 3-phase power is measured by 3 wattmeter method?
- I) Draw the diagram of Instrumentation amplifier and explain its working.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

For the circuit given below R_1 =39KΩ, R_2 =6.8KΩ, R_C =5.6KΩ, R_E =1.2KΩ, VCC=12V, β =120. (16) Find the I_{BQ} , I_{CQ} , I_{EQ} , V_{CEQ} , V_{BQ} , V_{CQ} , and V_{BC} .



Draw the phase voltage and line voltage phasor diagram of a 3-phase delta connected balanced system. A 3 phase 230V load with a power factor of 0.5. Two wattmeters are connected to measure the power showing the input to be 7KW. Find the rating of each wattmeter.

Q5 Discuss the special diodes. (16)

Q6 Derive the expression for the impulse response and step response of a second order (16) circuit.