

Project Report

Project Code : B2

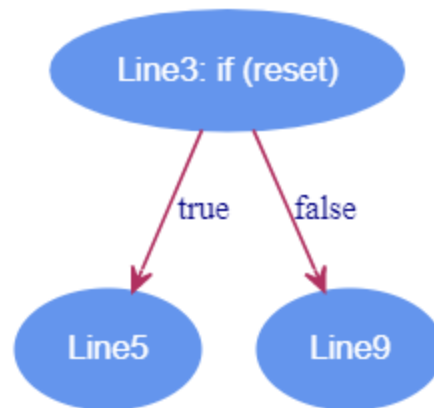
Goal:- Deriving complete Control flow graphs (CFG) of processor modules

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To solve this problem we have broken the problem into smaller parts. In verilog code, we have to handle many loops/control blocks.

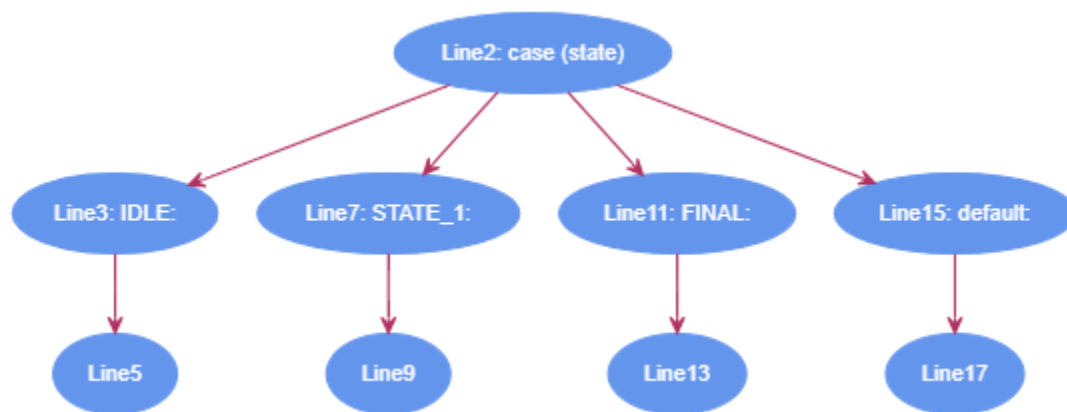
1. If , else if, else statement

```
always @(posedge clk or posedge reset)
begin
  if (reset)
  begin
    q <= 1'b0;
  end
  else
  begin
    q <= d;
  end
end
endmodule
```



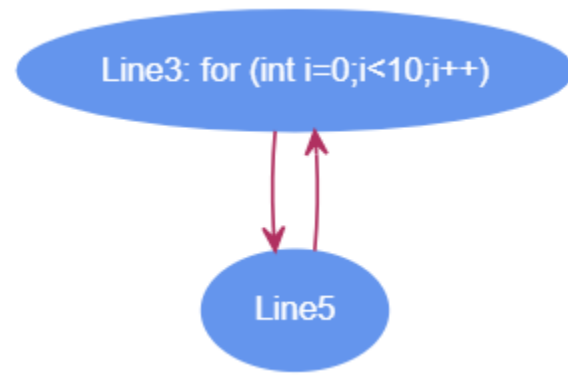
2. switch case statement

```
always @(posedge clk) begin
  case (state)
    IDLE:
      begin
        state <= IDLE;
      end
    STATE_1:
      begin
        state <= FINAL;
      end
    FINAL:
      begin
        state <= ACCESS;
      end
    default:
      begin
        state <= SETUP;
      end
  endcase
end
```



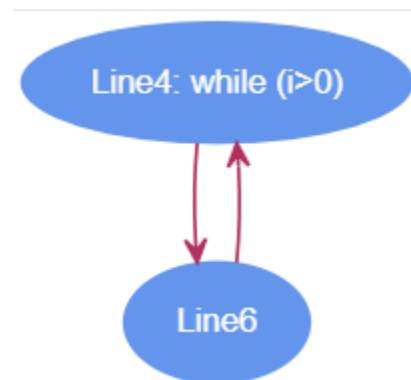
3. for loop

```
module tb;
  initial begin
    for (int i=0;i<10;i++)
      begin
        $display ("iteration [%0d]", i);
      end
  end
endmodule
```



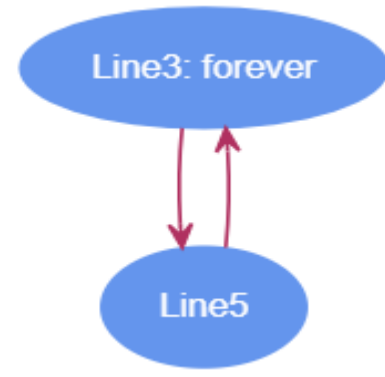
4. While loop

```
module mydesign;
  integer i = 5;
  initial begin
    while (i>0)
      begin
        $display ("Iteration#%0d", i);
        i = i-1;
      end
  end
endmodule
```



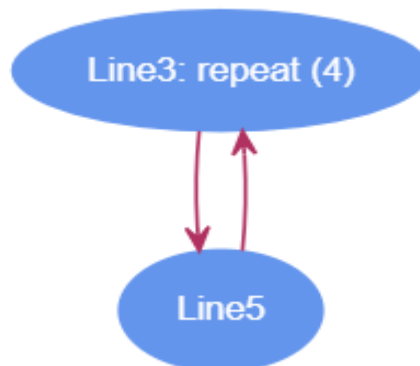
5. forever loop

```
module mydesign:
  initial begin
    forever
    begin
      $display("This will be printed")
    end
  end
endmodule
```



6. repeat loop

```
module mydesign:
  initial begin
    repeat (4)
    begin
      $display("there is a system");
    end
  end
endmodule
```

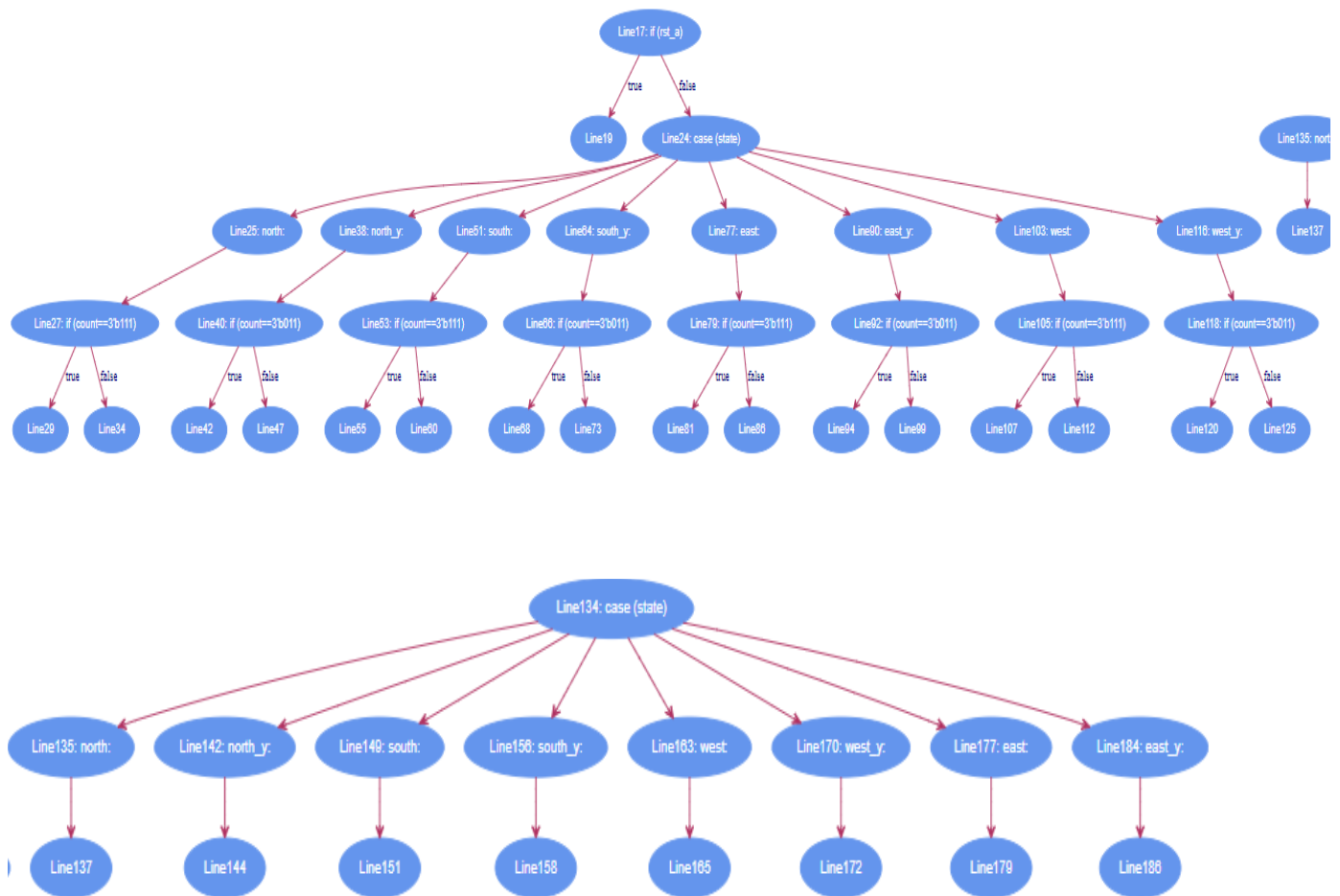


Control flow diagram for large input files

As the input file is large, we provide .txt files of verilog code in the zip files.

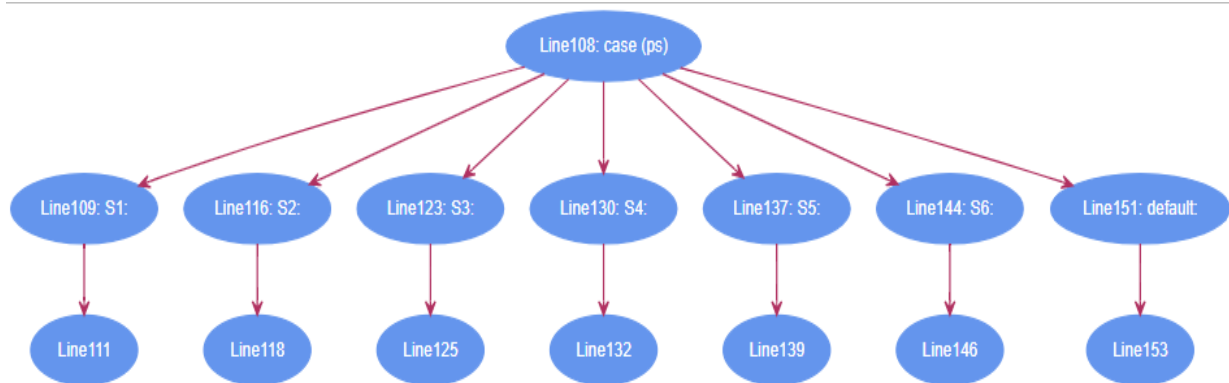
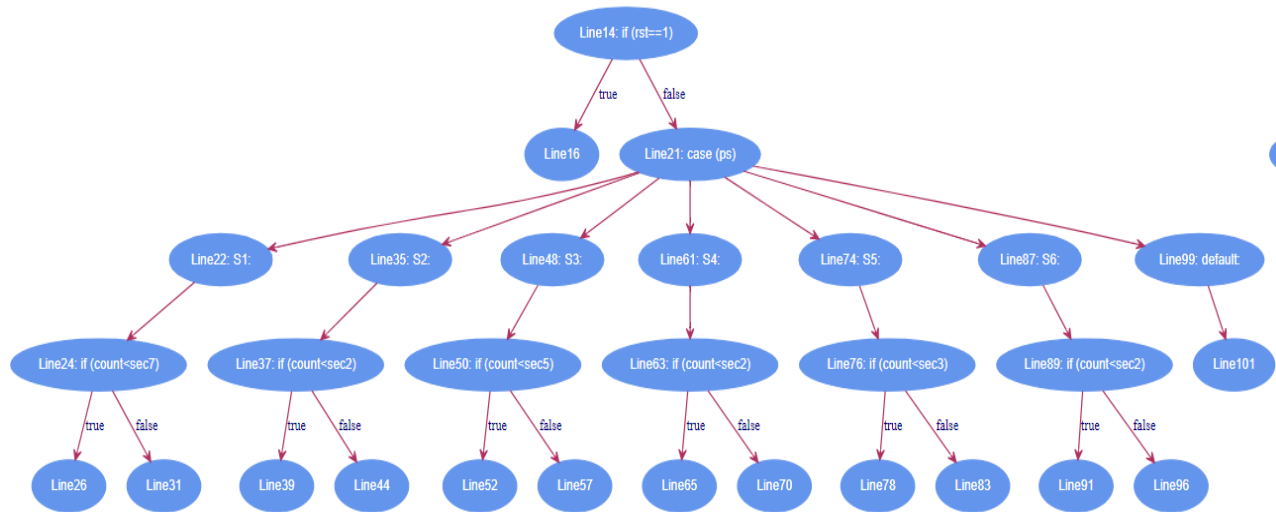
1. Traffic_light_controller verilog code

Control flow diagram:



2. Case_1 verilog code

Control flow diagram:



3. Tic_Tae_Toe_Game Verilog code

Control flow diagram:

