1.   Refer to the datasheet for 74C00.
      (https://pdf1.alldatasheet.com/datasheet-pdf/view/351452/ONSEMI/74HC00.html)

      i)   Under normal conditions what is the largest LOW-state voltage that should appear at the
            output of this gate where V_{CC}=6 V?

      ii)   What is the ESD voltage for the Human Body Model (HBM)?

2   In a digital system define the following parameters:
      a)   Propagation delay time -

      b)   Power consumption -

      c)   noise immunity -

3.   Two different logic circuits have the following characteristics:

	Circuit A	Circuit B
V_{supply}	6 V	10 V
V_{IH}	1.6 V	1.8 V
V_{IL}	0.9 V	0.7 V
V_{OH}	2.2 V	2.5 V
V_{OL}	0.4 V	0.3 V
t_{PLH}	10 ns	18 ns
t_{PHL}	8 ns	14 ns
P_D	16 mW	10 mW

      a)   Which circuit has the best LOW-state dc noise immunity?
      b)   Which circuit has the best HIGH-state dc noise immunity?
      c)   Which circuit operates at the higher frequency?
      d)   Which circuit has the lower power consumption?

4.   List any 3 characteristics of the CMOS ICs.

5.   Give a comparison of CMOS ICs to that of TTL ICs with reference to the following:

Parameters		CMOS	TTL
1	Speed		
2	Power		
3	Noise Immunity		
4	Voltage Range		
5	ESD tolerance		

6.   The greater the noise margin, the greater is the noise immunity. True/False

7.   List any two common Electrostatic Sensitive Device (ESD).

8.   Explain what is Electrostatic Discharge?

9.   List four precautions how should an ESD device be handled?

10.   Explain why an unused input of CMOS chips must not be left unattended?
      With an aid of a diagram, show how an unused input of a AND gate should be handled.

Formula for Q3

Noise margin calculation:	VNH = VOH(max) -VIH(min)	VNL = VIL(min) -VOL(max)
Propagation delay, Pd Frequency , f	Pd= tpLH + tpHL /2	f = 1/Pd