Indian Institute of Technology, Goa

Lab-7 report

(Latches and Flip-Flops)

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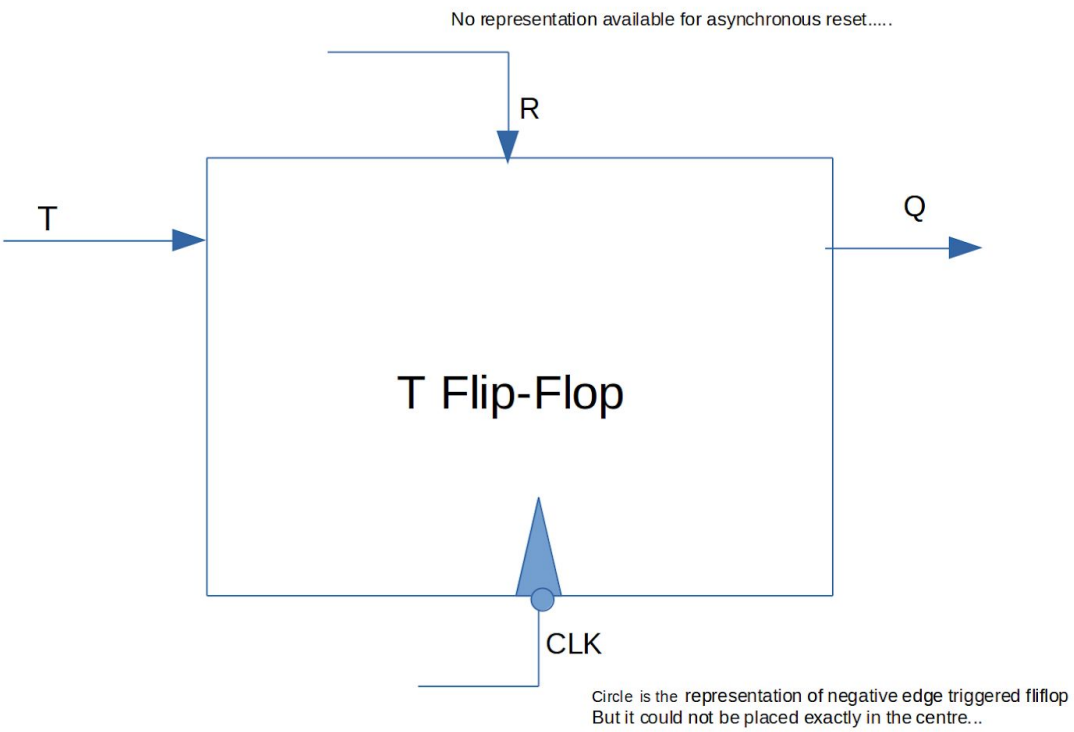
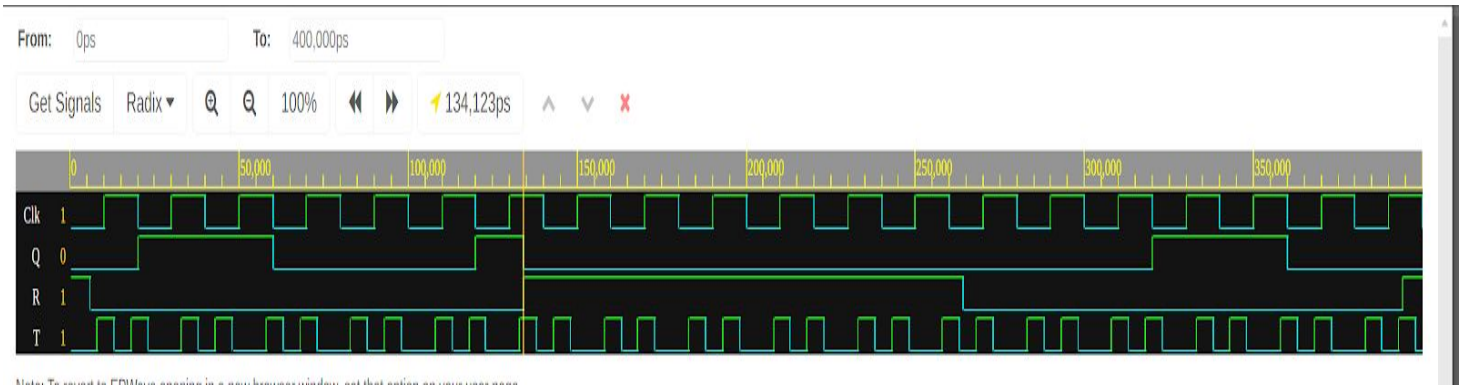
Abstract : This Report explains the architecture of T Flip-Flop vhdl code .It also presents the simulation waveform obtained by the simulation of the VHDL code in EDA playground,as well as the interface diagram of Negative Edge-triggered T Flip-Flop with an Asynchronous Reset.

Interface Diagram of Negative Edge-triggered T Flip-Flop with an Asynchronous Reset



Simulation Waveform



Explanation of the waveform *:-*

Time(ns)	Behaviour of waveform
0-8	Reset=’1’ ,thus output Q=’0’.
At 20	There is a negative edge of the clock;Also T=’1’ and R=’0’; Thus Q toggles from ‘0’ to ‘1’.
At 60	There is a negative edge of the clock;Also T=’1’ and R=’0’; Thus Q toggles from ‘1’ to ‘0’.
At 120	There is a negative edge of the clock;Also T=’1’ and R=’0’; Thus Q toggles from ‘0’ to ‘1’.
134-264	Reset=’1’ ,thus output Q=’0’.(Although at t=160ns,210ns T=’1’ and clock has a negative edge but Q didn't toggle)
At 320	There is a negative edge of the clock;Also T=’1’ and R=’0’; Thus Q toggles from ‘0’ to ‘1’.
	AND THE PROCESS CONTINUES…..

Architecture of T Flip-Flop

```
13 architecture Behav1 of TFF is
14 begin
15     proc: process(Clk,R) is
16     begin
17     if R='1' then
18         Q<='0';
19     else
20         if Clk'event and Clk='0' then
21             if T='0' then
22                 Q<=Q;
23             else
24                 Q<=not(Q);
25             end if;
26         end if;
27     end if;
28     end process proc;
29 end Behav1;
```

Some notable Features of this architecture are :-

1. Process Block is sensitive to both clock and reset as we wanted to represent an asynchronous reset.
2. When R=’1’ , Q=’0’.
3. Clk=’0’ represents negative edge triggered Flip-Flop.
4. T=’0’ keeps output the same,whereas T=’1’ toggles it.

--------**THE END**--------