Design a CMOS Differential Amplifier with Current Mirror Load.

A Presentation by
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Introduction:

A Differential Amplifier is a two-input circuit that amplifies only the difference between its two inputs. . In the ever-evolving landscape of electronic devices, there is a need for amplifiers that can provide high gain, exceptional common-mode rejection, and improved power efficiency concurrently.

To enhance the performance of differential amplifiers, we can integrate a Current Mirror load, which employs a current mirror circuit as the load for active devices. This addition offers advantages like improved biasing stability, enhanced output swing, and reduced sensitivity to process variations.

Application

1. Analog-to-Digital Converters (ADCs)
2. Communication Systems
3. Biomedical Applications.
4. Audio Amplification
5. High Speed Data Communication

Literature Survey

1. An investigation and literature survey to design the CMOS Differential Amplifier.

2. A differential amplifier that amplifies two input signals and determines their differences.

3. To gain fundamental knowledge about CMOS differential amplifiers.

4. Advance Design System (ADS) is used to simulate NMOS and PMOS and display the amplifier design.

5. To construct an amplifier array with neural recording that is ultra-power and low noise.

6.To amplify two input signals and determine the difference.

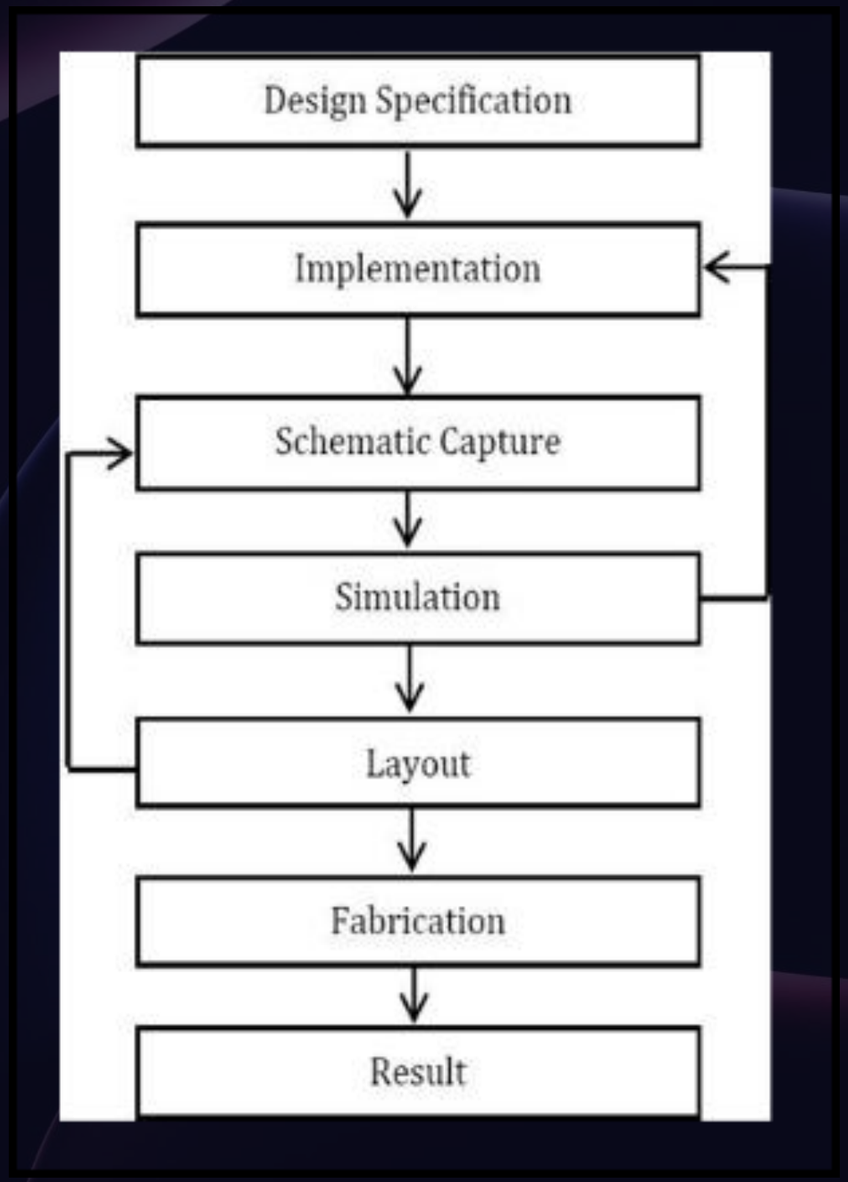
7.To use NMOS current meter loads from several topologies to achieve the circuit's specifications and purpose.

Objectives:-

The Purpose of the Differential Amplifier is to increase the amplitude of a signal to a level where it can be converted into a digital form.

The project aims to design and analyze a differential amplifier circuit with a current mirror load for enhanced performance in terms of gain, CMRR and power efficiency. The impact of variations in key parameters will be investigated, and strategies to optimize the design for a specific application will be explored. The focus is on reducing the amplifier size while maintaining low noise and power consumption.

Planning and Approach



Design Analysis

Small-signal gain *A*v $A_v = g_{m1}R_{\text{out}}$

Frequency response for a given load capacitance, ω-3 dB $\omega_{-3\text{ dB}} = \frac{1}{R_{\text{out}}C_L}$

Input common-mode range (ICMR) or maximum and minimum input common-mode voltage [*VIC* (max) and *VIC*(min)]

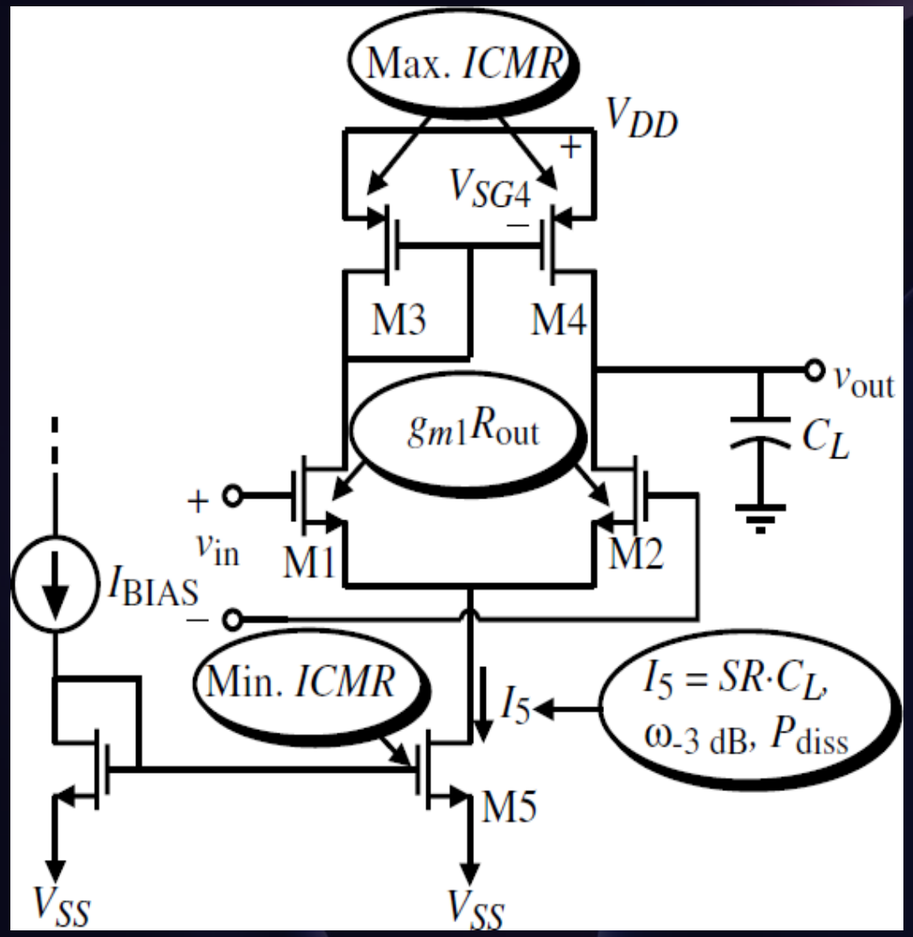
$$V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}$$

$$V_{IC}(\min) = V_{DS5}(\text{sat}) + V_{GS1} = V_{DS5}(\text{sat}) + V_{GS2}$$

Slew rate for a given load capacitance, *SR*:- $SR = I_5/C_L$

Power dissipation P_{diss} $P_{\text{diss}} = (V_{DD} + |V_{SS}|)(I_5) = (V_{DD} + |V_{SS}|)(I_3 + I_4)$

Circuit Schematic and Procedure



This circuit diagram illustrates the relationships that are typically used to design the various parameters of the current-mirror load differential amplifier.

This design procedure assumes that the small-signal differential voltage gain, Av; the -3 dB frequency, ω-3 dB; the maximum input common mode voltage, VIC (max); the minimum common mode voltage, VIC (min); the slew rate, SR; and the power dissipation, Pdiss, are given.

1.Choose I5 to satisfy the slew rate knowing CL or the power dissipation, Pdiss

2.Check to see if R out will satisfy the frequency response and if not, change I5 or modify thecircuit (choose a different topology).

3.Design W3/L3 (W4/L4) to satisfy the upper ICMR.

4.Design W1/L1 (W2/L2) to satisfy the small-signal differential voltage gain, Av.

5.Design W5/L5 to satisfy the lower ICMR.

6.Iterate where necessary.

Reference

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THANK YOU