ORGANISASI & ARSITEKTUR KOMPUTER

SEMESTER 2

PERTEMUAN KE-1

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ORGANISASI & ARSITEKTUR

- **Organisasi** → Bagaimana suatu perangkat diimplementasikan
  - Sinyal kontrol, interface dan memori
  - Contoh:
    - penambahan hardware baru atau penambahan hardware secara berulang.
    - Apakah instruksi perkalian diimplementasikan secara hardware, ataukah dikerjakan dengan penambahan secara berulang?
- **Arsitektur** → Atribut yang berhubungan dengan programmer
  - Kumpulan bit, jumlah bit yang digunakan untuk representasi data, mekanisme I/O, teknik pengalamatan
  - Contoh: apakah tersedia instruksi untuk perkalian?

ORGANISASI & ARSITEKTUR

- Arsitektur sama, organisasi dapat berbeda
- Arsitektur bertahan lama, organisasi menyesuaikan perkembangan teknologi
  - Semua keluarga Intel x86 mempunyai dasar arsitektur yang sama
  - Semua keluarga IBM system/370 mempunyai dasar arsitektur yang sama
  - Memberikan kompatibilitas kode
  - Organisasi berbeda jika versi berbeda

FUNGSI DAN STRUKTUR

- Fungsi merupakan operasi dari masing-masing komponen sebagai bagian dari struktur
- Struktur adalah bagaimana masing-masing komponen saling berhubungan satu sama lain

FUNGSI

- Semua komputer berfungsi untuk:
  - Pengolahan data (Data processing)

Data dapat memiliki berbagai bentuk, dan berbagai persyaratan pemrosesan. Namun hanya ada beberapa metode dasar atau jenis pemrosesan data.

  - Penyimpanan data (Data storage)

Komputer sedang memproses data dengan cepat (mis data masuk dan diproses, dan hasilnya segera keluar), dalam sementara waktu komputer harus menyimpan setidaknya potongan data yang sedang dikerjakan setiap saat.

  - Pemindahan data (Data movement)

Lingkungan pengoperasian komputer terdiri dari beberapa perangkat yang berfungsi sebagai sumber atau tujuan data.

  - Control

Unit kontrol mengelola computer sumber daya dan mengatur kinerja bagian fungsionalnya sebagai respons untuk instruksi.

FUNGSI KOMPUTER

Komputer dilihat dari sudut pandang fungsi

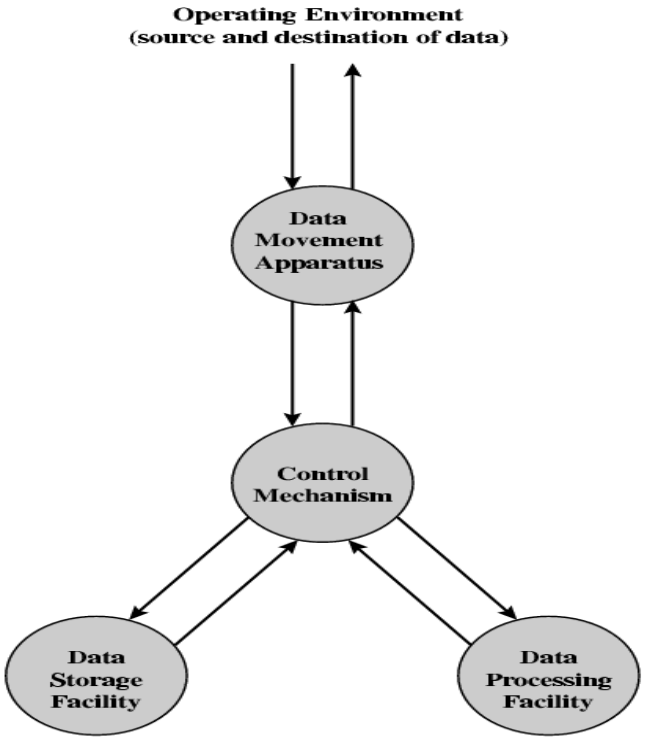
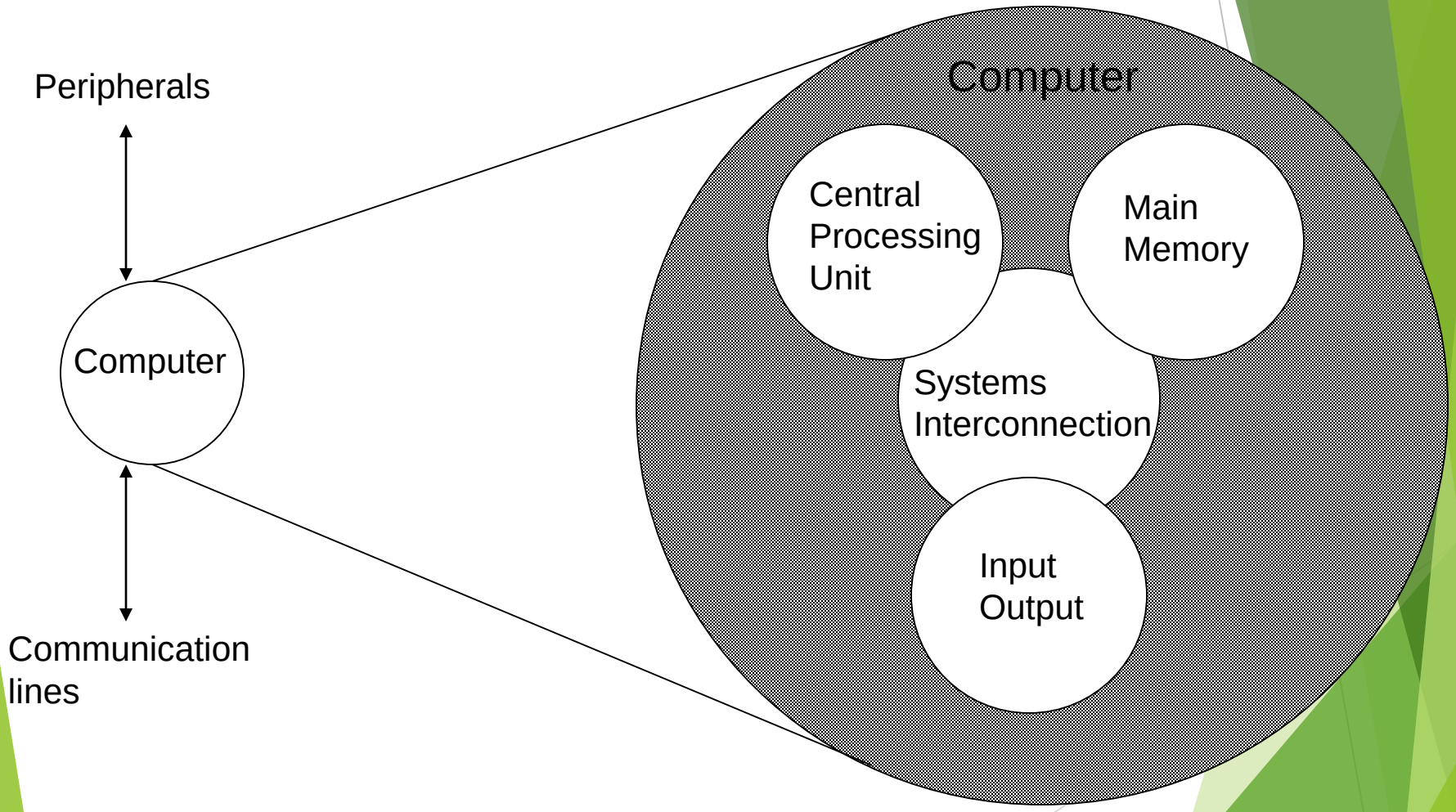
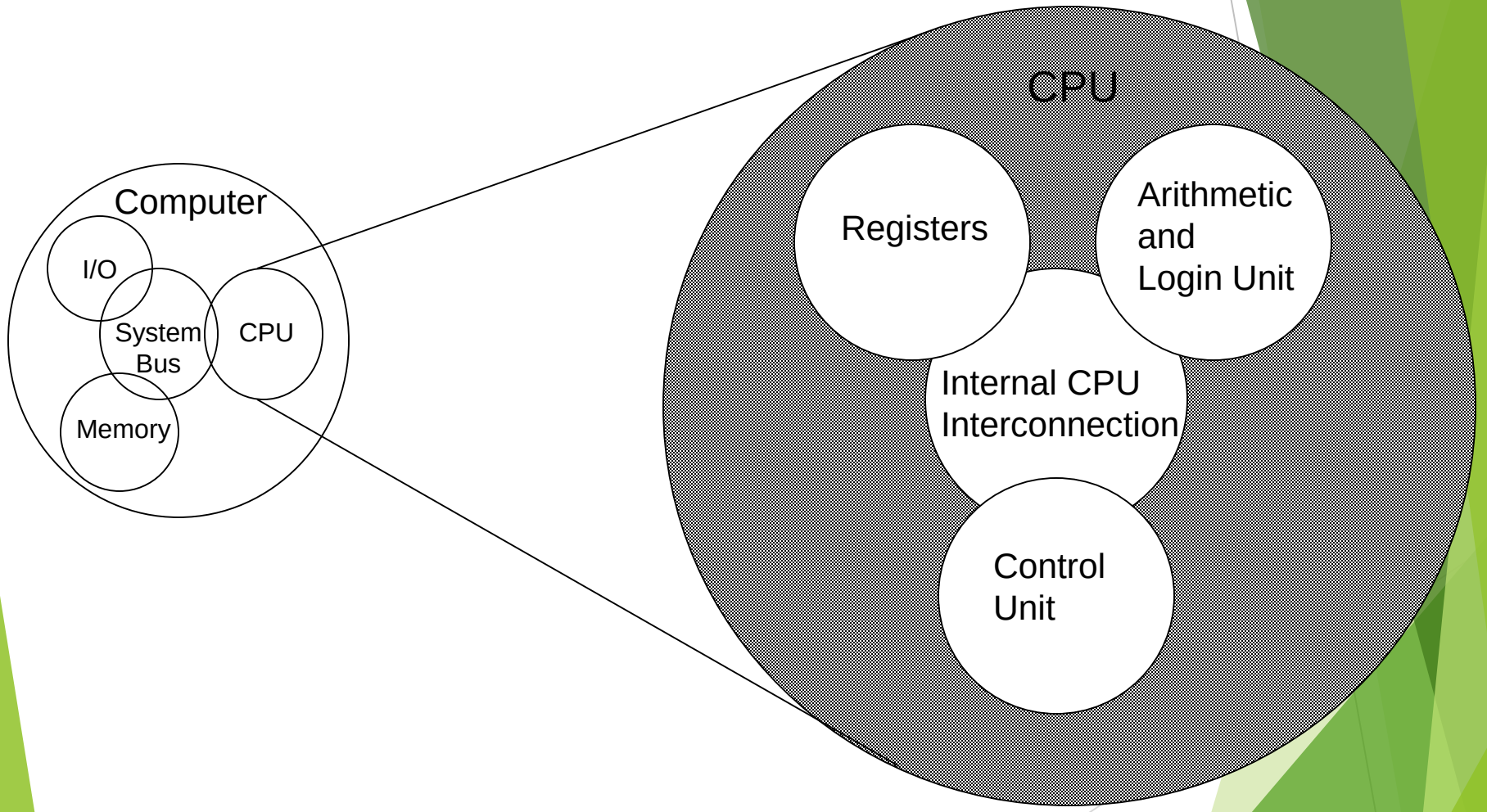


Figure 1.1 A Functional View of the Computer

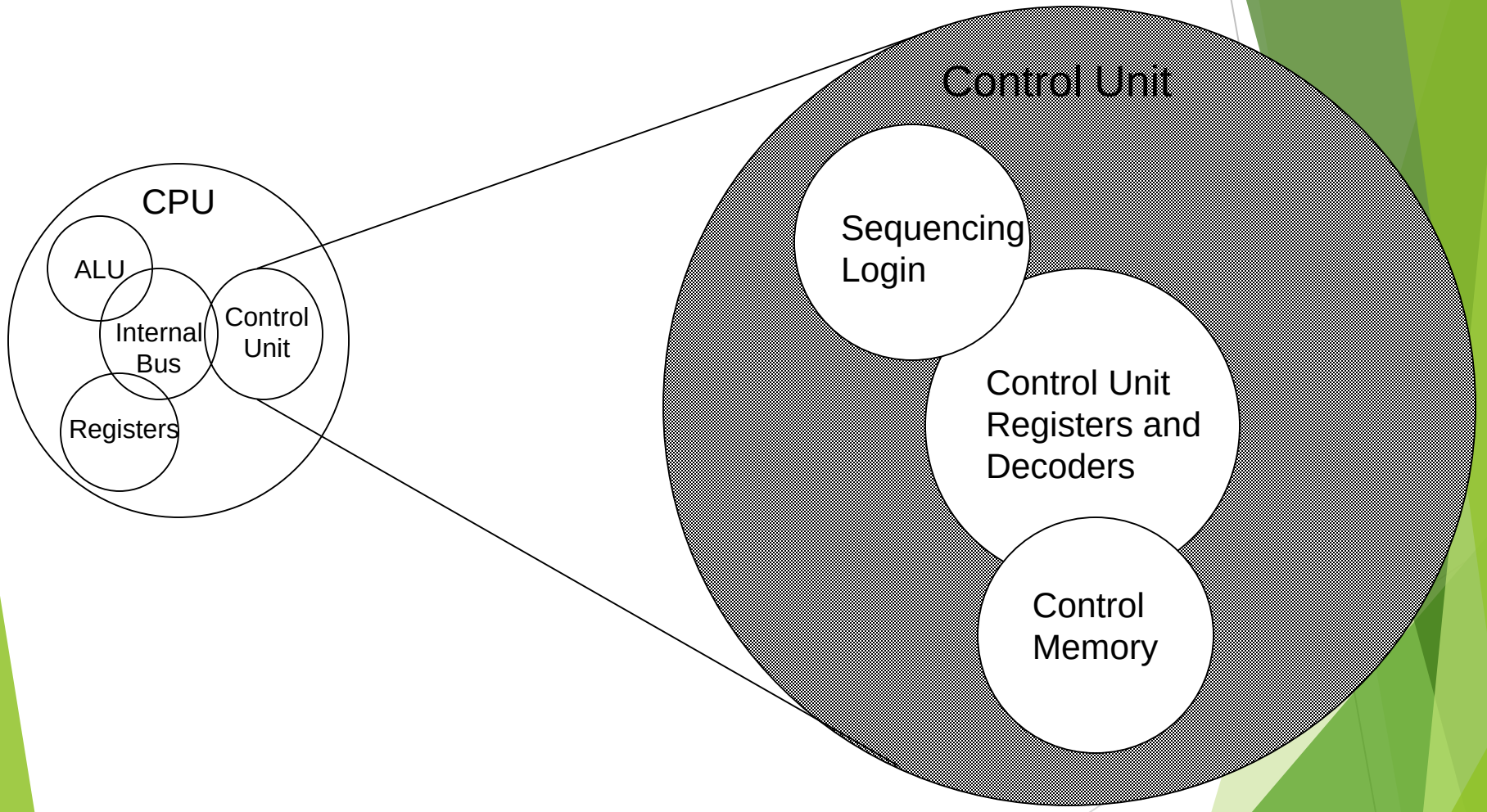
STRUKTUR – TOP LEVEL



STRUKTUR - CPU



STRUKTUR – KONTROL UNIT



Struktur Komputer

- Penjelasan setiap bagian dari computer satu prosesor dan multicore ada pada halaman 4, 5, dan 6. (Buku Wajib)

Misal penjelasanya:

- Central processing unit (CPU): Mengontrol operasi komputer dan melakukan fungsi pemrosesan data; sering disebut **prosesor.**
- Core (Inti) - multicore: Unit pemrosesan individual pada chip prosesor. Inti setara fungsinya dengan CPU pada sistem CPU tunggal. Unit pemrosesan khusus lainnya, misal yang dioptimalkan untuk operasi vektor dan matriks, disebut juga core.
- Dst … baca bagian **printed circuit board (PCB)** untuk multicore!

View prosesor multi-core

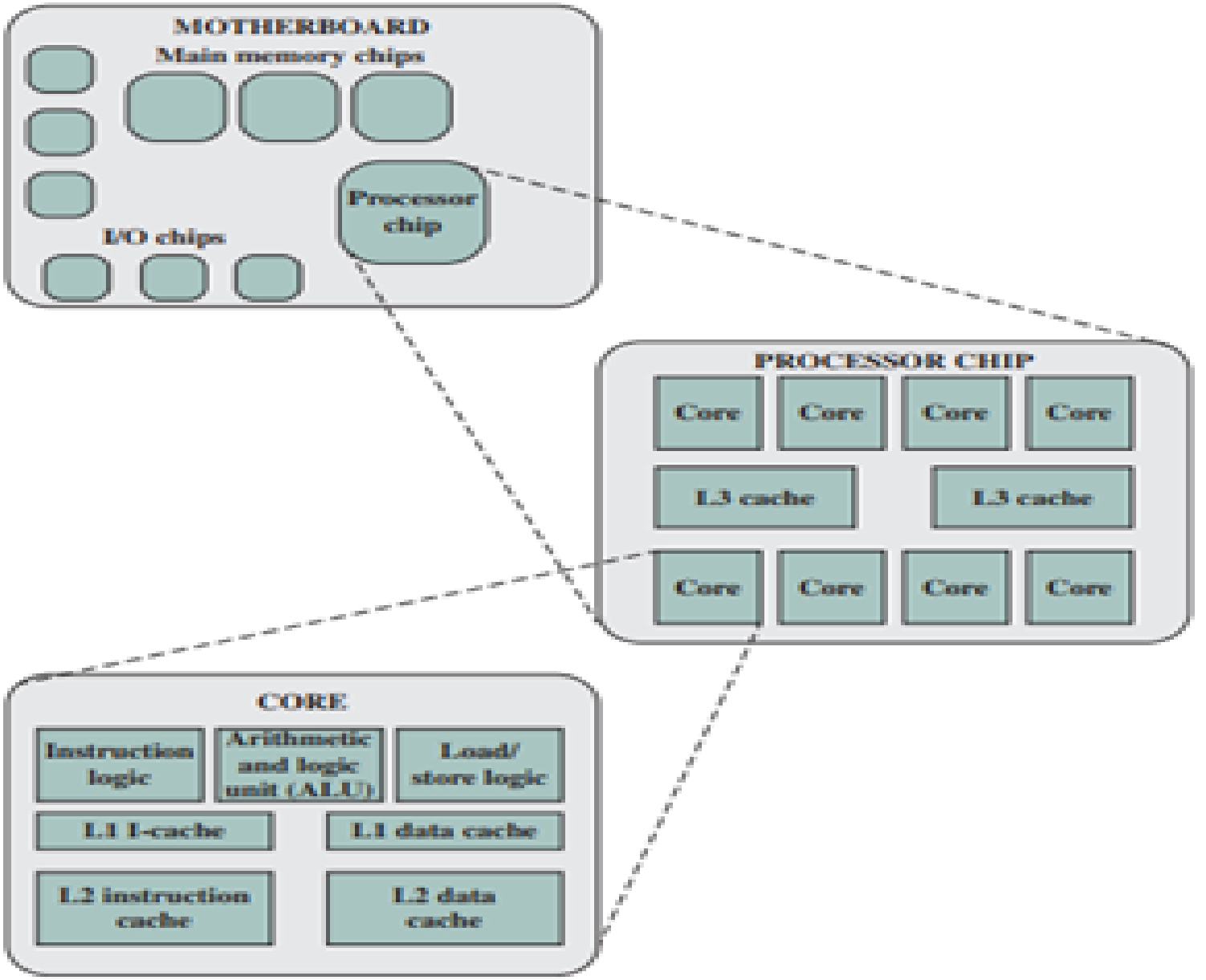


Figure 1.2 Simplified View of Major Elements of a Multicore Computer

Contoh kasus:

- Akan sangat berguna melihat beberapa contoh dunia nyata yang menggambarkan struktur hierarkis komputer. **Gambar 1.3** Foto dari motherboard untuk komputer dengan dua prosesor Intel Quad-Core Xeon. Banyak elemen yang dilabeli yang akan dibahas. Bagian paling penting, selain prosesor adalah soket:
- ■ Slot PCI-Express untuk adaptor tampilan kelas atas dan untuk periferal tambahan.
- ■ Pengontrol Ethernet dan port Ethernet untuk koneksi jaringan.
- ■ Soket USB untuk perangkat peripheral, dst ….

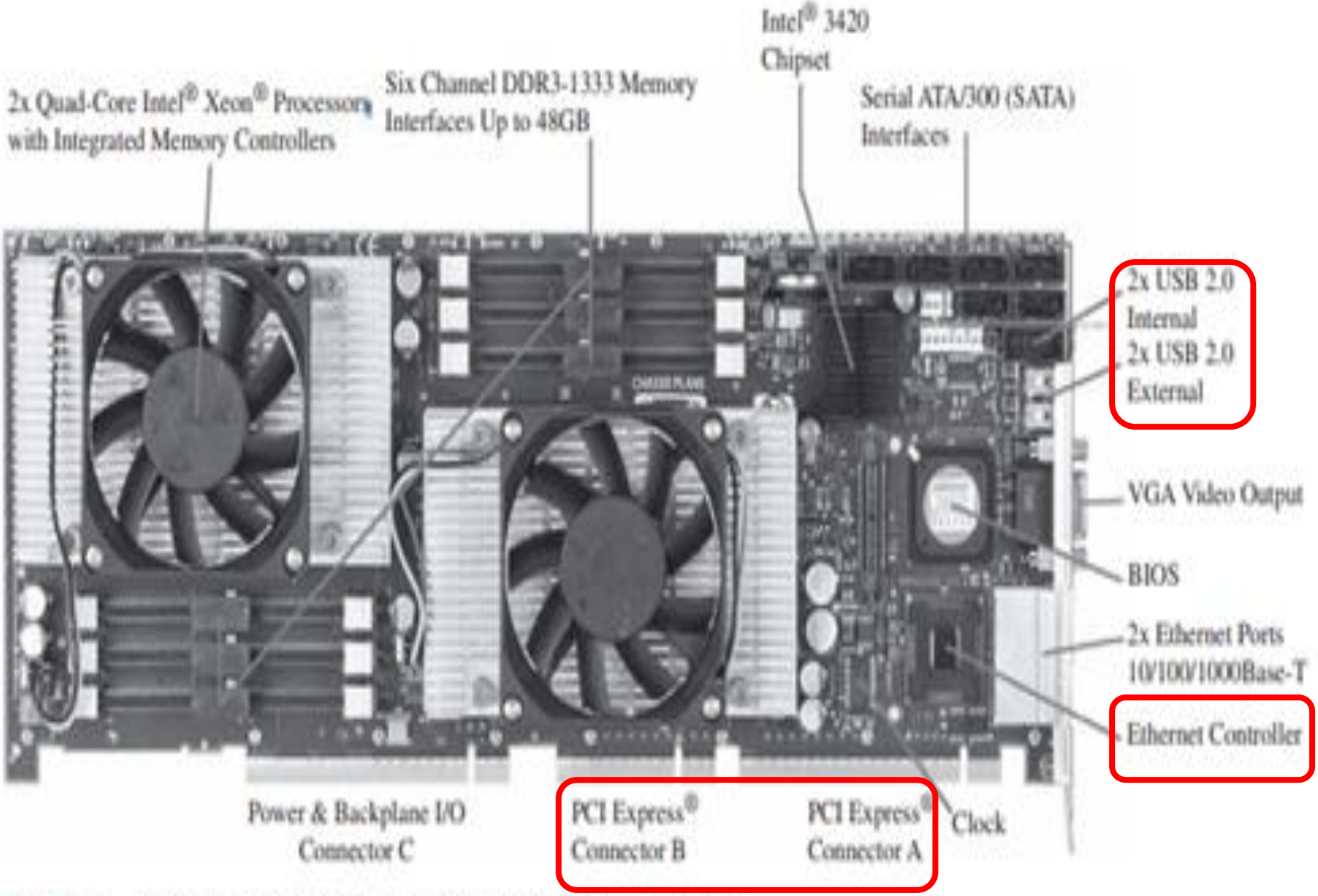


Figure 1.3 Motherboard with Two Intel Quad-Core Xeon Processors

Source: Chassis Plans, www.chassis-plans.com

Here, we mention the most important, in addition to the processor sockets:

- PCI-Express slots for a high-end display adapter and for additional peripherals (Section 3.6 describes PCIe).
- Ethernet controller and Ethernet ports for network connections.
- USB sockets for peripheral devices.

Serial ATA (SATA) sockets for connection to disk memory (Section 7.7 discusses Ethernet, USB, and SATA).

- Interfaces for DDR (double data rate) main memory chips (Section 5.3 discusses DDR).
- Intel 3420 chipset is an I/O controller for direct memory access operations between peripheral devices and main memory (Section 7.5 discusses DDR).

Nama subarea prosesor zEnterprise EC12

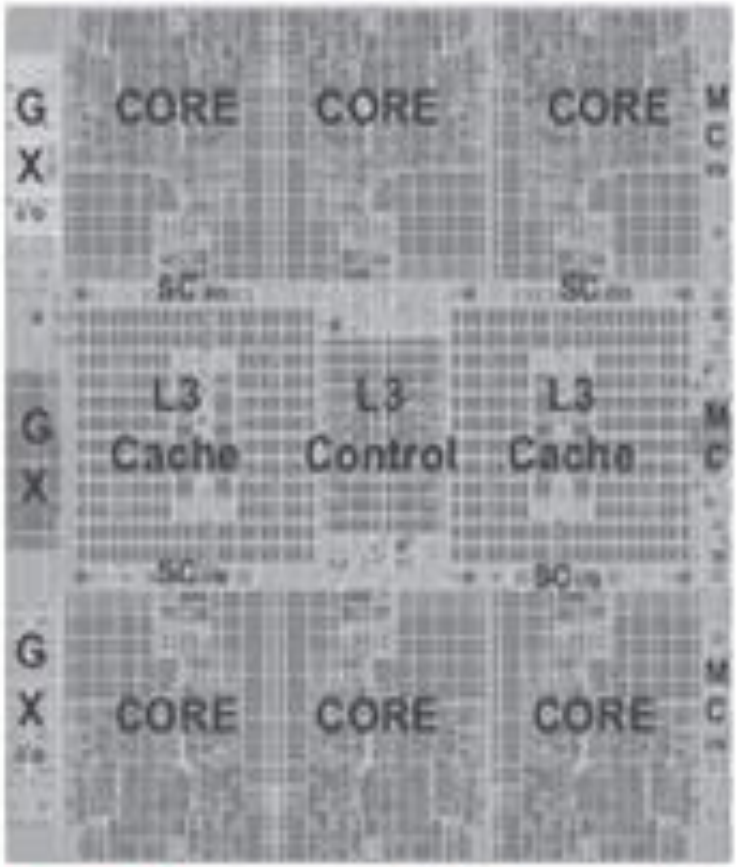


Figure 1.4 zEnterprise EC12 Processor Unit (PU) chip diagram
Source: IBM zEnterprise EC12 Technical Guide, December 2013, SG24-8049-01. IBM, Reprinted by Permission

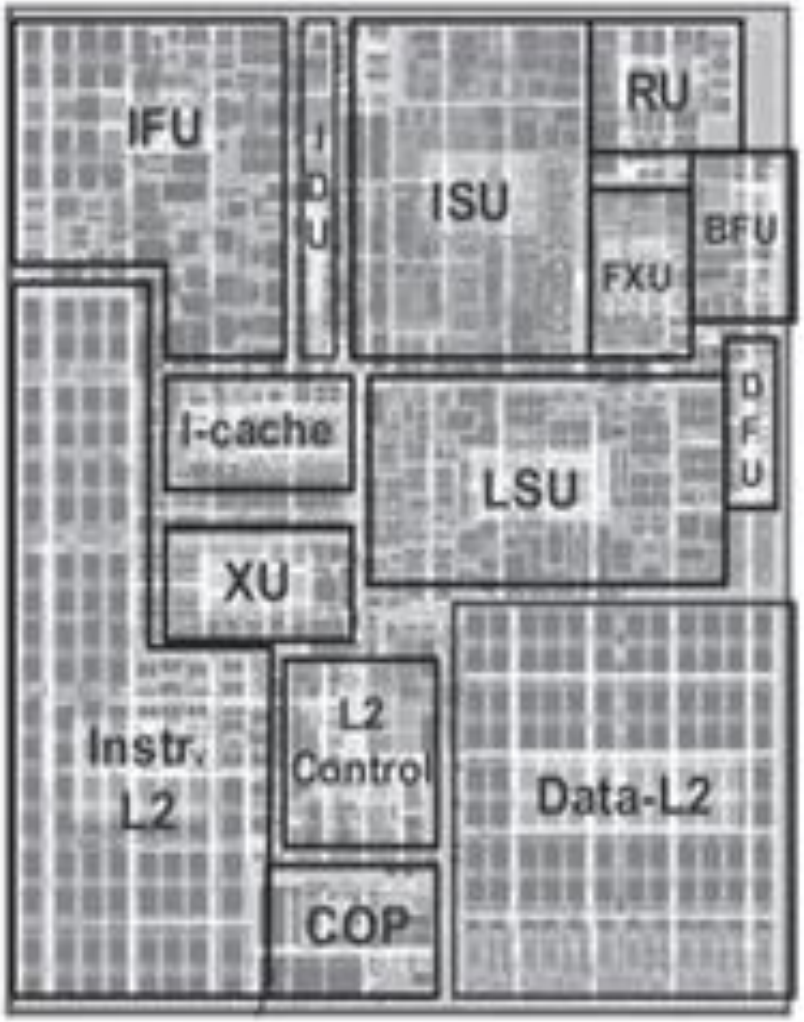


Figure 1.5 zEnterprise EC12 Core layout
Source: IBM zEnterprise EC12 Technical Guide, December 2013, SG24-8049-01. IBM, Reprinted by Permission

The main sub- areas within this core area are the following:

■ ISU (instruction sequence unit): Determines the sequence in which instructions are executed in what is referred to as a superscalar architecture (Chapter 16).

■ IFU (instruction fetch unit): Logic for fetching instructions.

■ IDU (instruction decode unit): The IDU is fed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.

■ LSU (load-store unit): The LSU contains the 96-kB L1 data cache,1 and manages data traffic between the L2 data cache and the functional execution units. It is responsible for handling all types of operand accesses of all lengths, modes, and formats as defined in the z/Architecture.

■ XU (translation unit): This unit translates logical addresses from instructions into physical addresses in main memory. The XU also contains a translation lookaside buffer (TLB) used to speed up memory access. TLBs are discussed in Chapter 8.

■ FXU (fixed-point unit): The FXU executes fixed-point arithmetic operations.

■ BFU (binary floating-point unit): The BFU handles all binary and hexadecimal floating-point operations, as well as fixed-point multiplication operations.

■ DFU (decimal floating- point unit): The DFU handles both fixed- point and floating-point operations on numbers that are stored as decimal digits.

■ RU (recovery unit): The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault signals, and manages the hardware recovery actions.

■ COP (dedicated co-processor): The COP is responsible for data compression and encryption functions for each core.

■ I- cache: This is a 64-kB L1 instruction cache, allowing the IFU to prefetch instructions before they are needed.

■ L2 control: This is the control logic that manages the traffic through the two L2 caches.

■ Data-L2: A 1-MB L2 data cache for all memory traffic other than instructions.

■ Instr-L2: A 1-MB L2 instruction cache.

The First Generation: Vacuum Tubes

- Komputer IAS dikenal sebagai komputer *stored-program concept* juga dikenal sebagai konsep dari **John von Neumann**.
- all of today's computers have this same general structure and function and are thus referred to as von Neumann machines.
- Struktur IAS terdapat:
  1) Main memory, menyimpad data dan instruksi
  2) Arithmetic and logic unit (ALU) operasi data dalam biner
  3) Kontrol unit, yang menginterpretasikan instruksi untuk dieksekusi
  4) Unit Input–output (I/O)

GAMBAR BERIKUT (Fig. 1.6 IAS Computer)

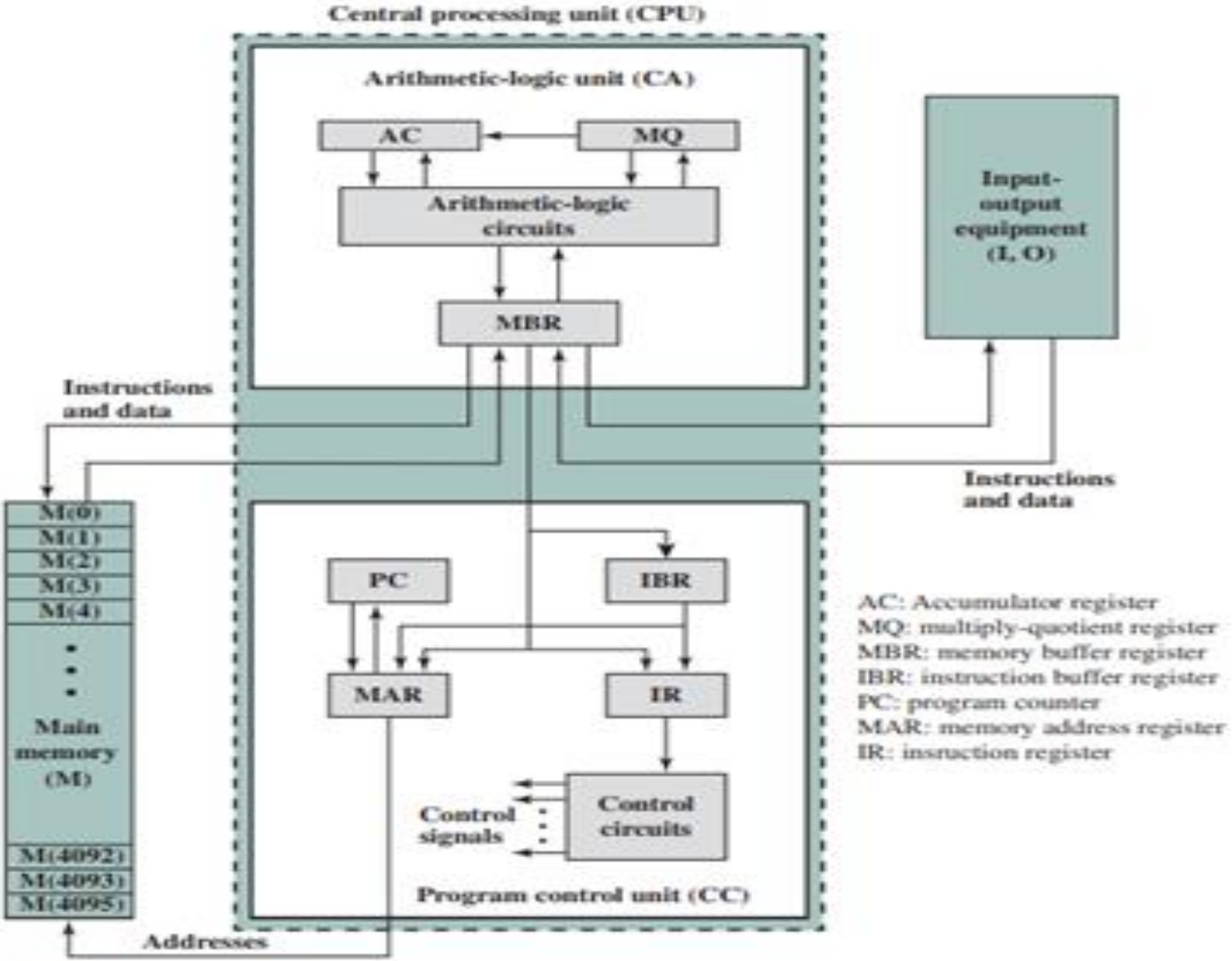
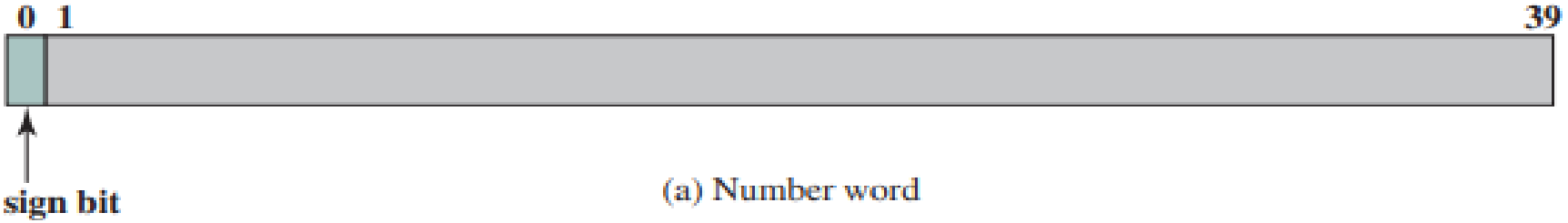
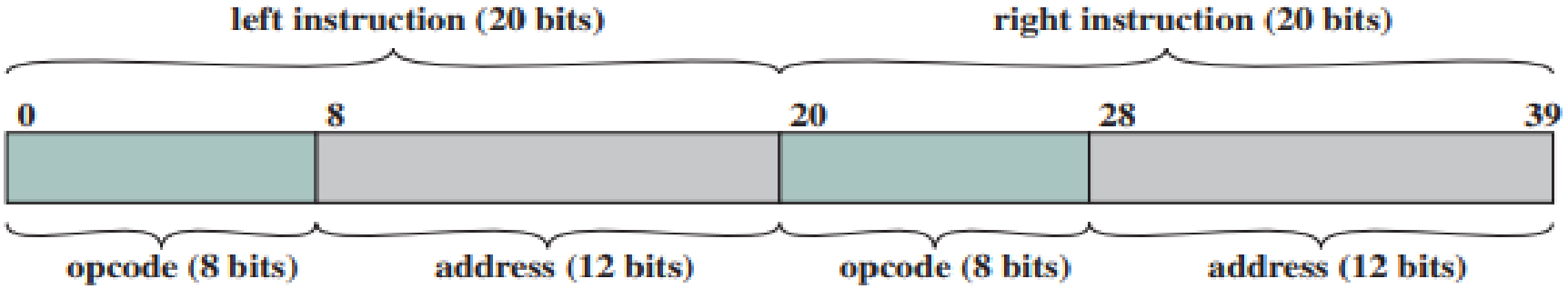


Figure 1.6 IAS Structure

Format Memori IAS



(a) Number word



(b) Instruction word

Figure 1.7 IAS Memory Formats

Table 1.1 The IAS Instruction Set

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD –M(X)	Transfer –M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD –|M(X)|	Transfer –|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP + M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP + M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; that is, shift left one bit position

Table 1.2 Computer Generations

Generation	Approximate Dates	Technology	Typical Speed (operations per second)
1	1946–1957	Vacuum tube	40,000
2	1957–1964	Transistor	200,000
3	1965–1971	Small- and medium-scale integration	1,000,000
4	1972–1977	Large scale integration	10,000,000
5	1978–1991	Very large scale integration	100,000,000
6	1991–	Ultra large scale integration	>1,000,000,000

Table 1.3 Evolution of Intel Microprocessors (hal. 26 – 27 dan penjelasanya).

DAFTAR PUSTAKA

- **Stallings, W.,** (2016), *Computer Organization and Architecture*, 10th edition, Prentice Hall
- http://williamstallings.com/ComputerOrganization/index.html