Hardware Assignment 2

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Problem Statement:

1. Design a combinational circuit that accepts a single 4-bit hexadecimal or decimal digit as input from the switches and generates a 7-bit output to drive the seven-segment display of the Basys3 FPGA board.
2. Extend the design to create a timing circuit that controls all four displays, enabling them to display four digits simultaneously.

Approach:

Design Decisions

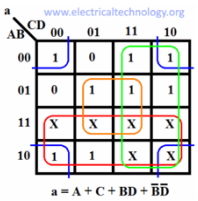
- **Component Breakdown:**
  - Multiplexer (mux4x1): A 4:1 multiplexer was used to select which input number will be displayed at a given time on the 7-segment display.
  - Timing Block: The timing block reduces the 100 MHz clock input and generates the mux_select signal, which controls which 4-bit input is selected by the multiplexer. It also generates anode signals for the display refresh.
  - BCD to 7-segment Decoder: The decoder takes the 4-bit number output from the multiplexer and converts it to a 7-segment display signal.
- **Clock Division:**
  - To control the refresh rate, the clock was divided to generate a suitable clock signal (~1 kHz to avoid flickering).
  - An internal signal new_clk was generated after counting cycles of the main 100 MHz clock.
- **Minimized Combinational Logic:**
  - The design of the BCD to 7-segment decoder involved deriving minimized logic expressions for each segment (a-g). Karnaugh maps were used to optimize the Boolean expressions.

Combinational Circuit:

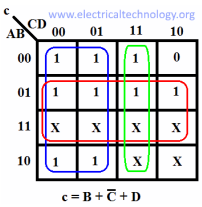
To design the combinational circuit, we first constructed a truth table representing the 4-bit input and the corresponding 7-bit output required for the cathodes of the seven-segment display.

K-Maps:

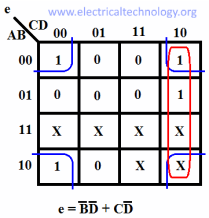
#for a:



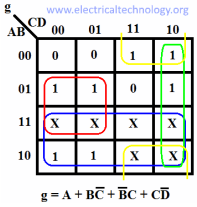
#for c:



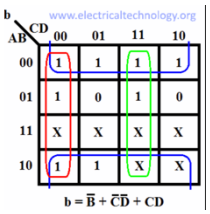
#for e:



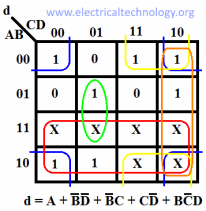
#for g:



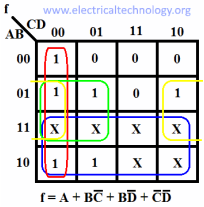
#for b:



#for d:



#for f:

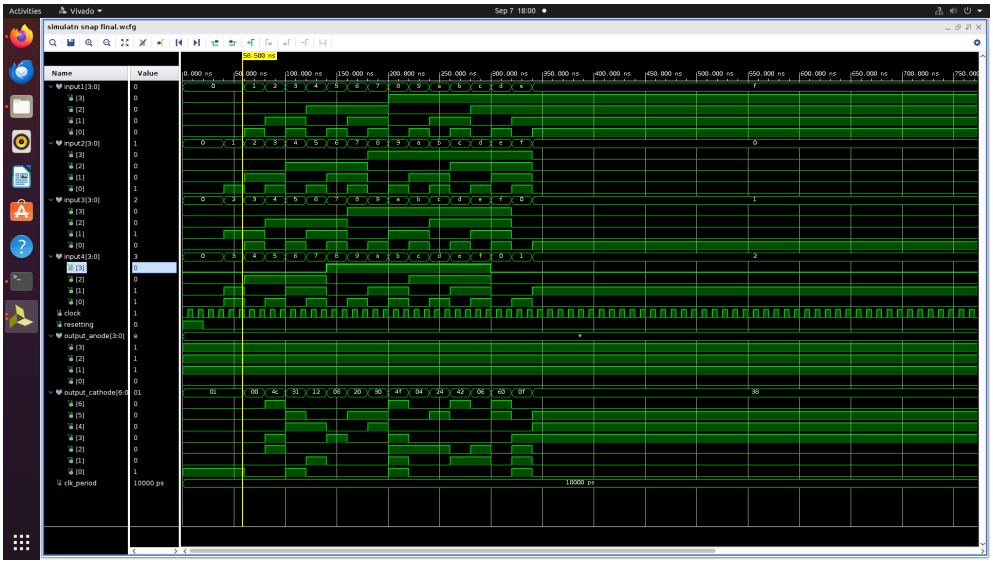


Here is the truth table that defines the relationship between the 4-bit inputs and the 7-segment display outputs:

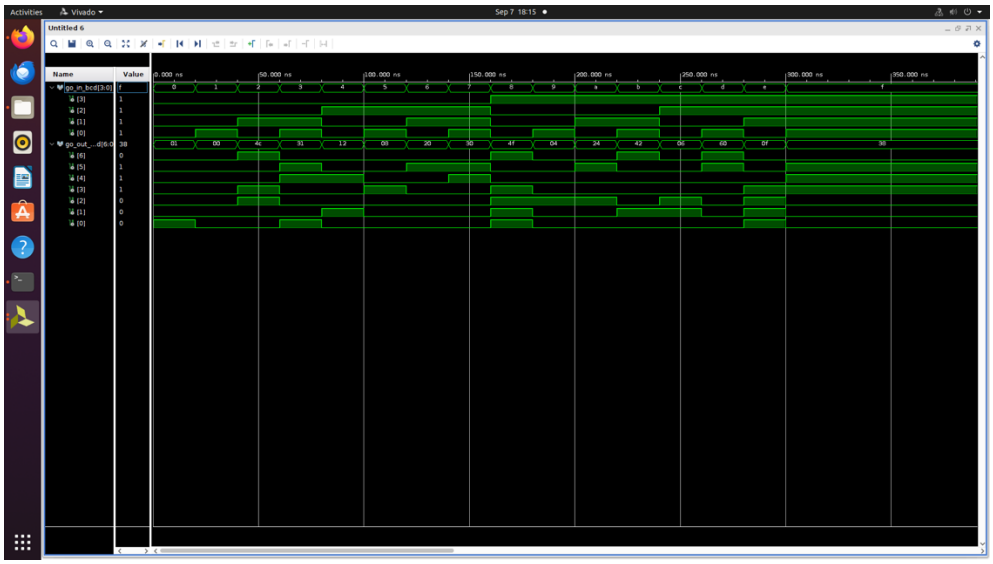
Input	Visual	a	b	c	d	e	f	g
0000		0	0	0	0	0	0	1
0001		1	0	0	1	1	1	1
0010		0	0	1	0	0	1	0
0011		0	0	0	0	1	1	0
0100		1	0	0	1	1	0	0
0101		0	1	0	0	1	0	0
0110		0	1	0	0	0	0	0
0111		0	0	0	1	1	1	1
1000		0	0	0	0	0	0	0
1001		0	0	0	0	1	0	0
1010		0	0	0	0	0	1	0
1011		1	1	0	0	0	0	0
1100		0	1	1	0	0	0	1
1101		1	0	0	0	0	1	0
1110		0	1	1	0	0	0	0
1111		0	1	1	1	0	0	0

Simulation Snapshots:

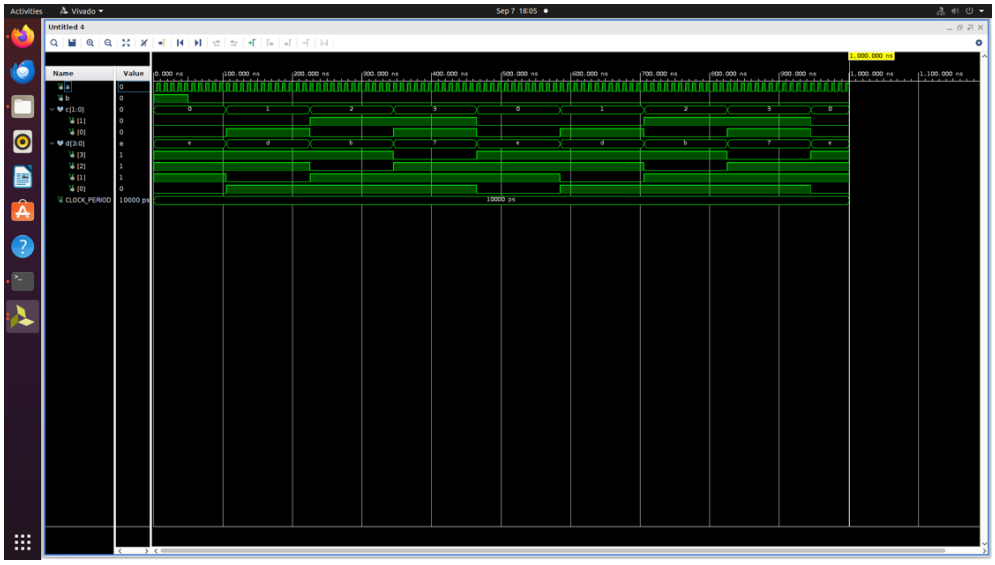
- top_entity simulation



- bcd_7 simulation

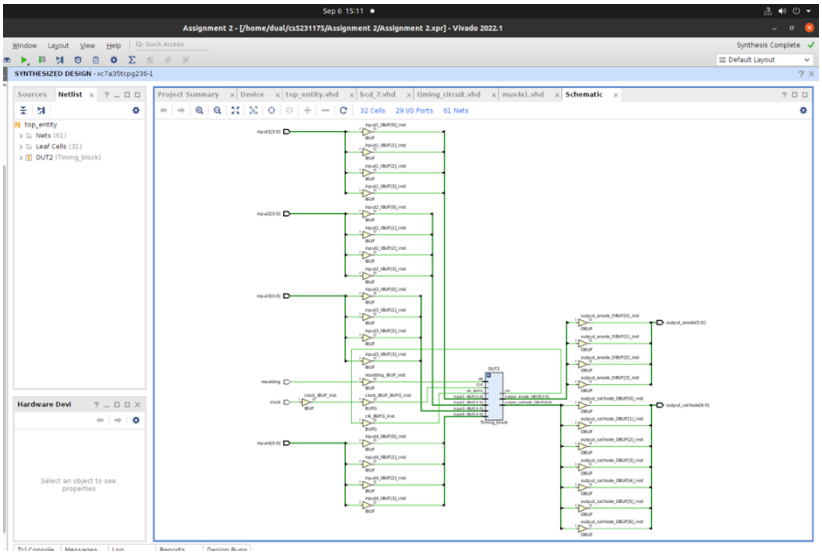


- timing_circuit simulation

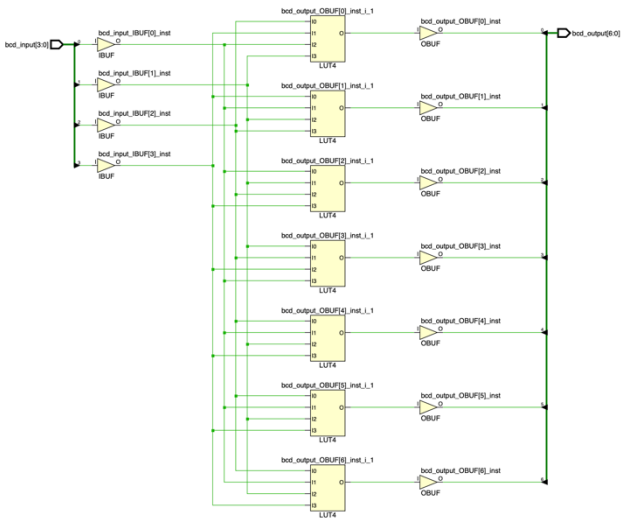


Schematic Snapshots:

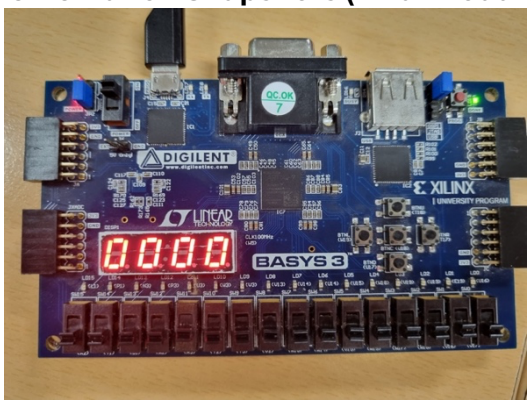
- top_entity schematic

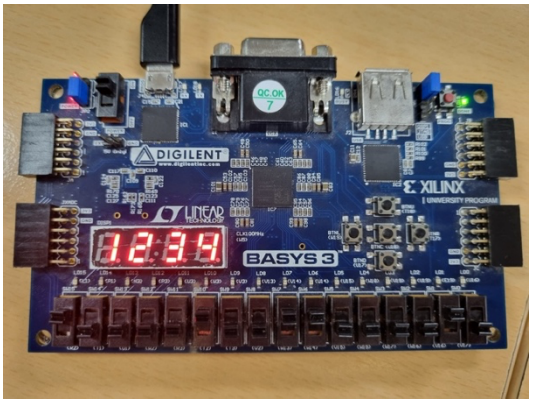


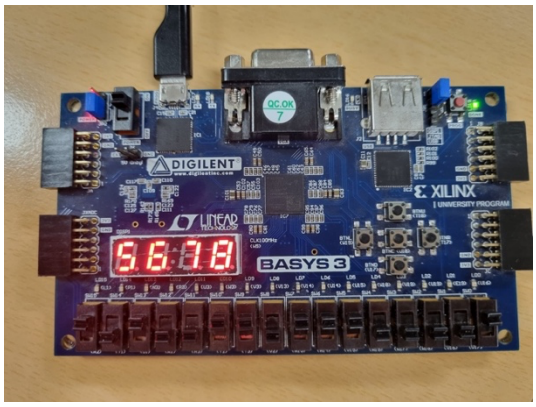
- bcd_7 schematic

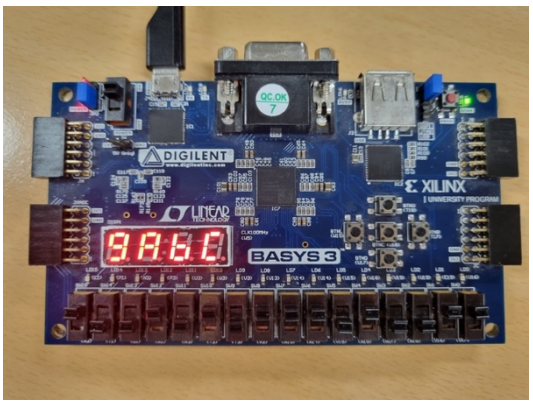


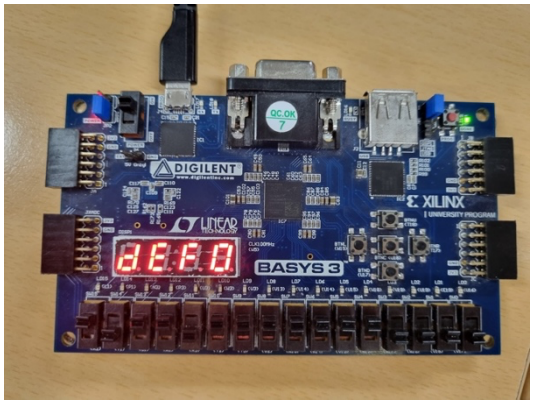
Implementation Snapshots (Final Module):











Timing block util table:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)	BUFGCTRL (32)
Timing_block	113	65	41	113	8	2

Mux4x1 util table:

Name	Slice LUTs (20800)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)
mux4x1	4	1	4	22

Bcd_7 util table:

Name	Slice LUTs (20800)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)
bcd_7	4	1	4	11

Summary of the Provided VHDL Codes

The project involves designing a hardware circuit that drives the 7-segment displays on the Basys 3 FPGA board. The VHDL code includes four key components:

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1. Top-Level Entity (top_entity.vhd)

- Purpose: The top_entity is the main module that connects the multiplexer (mux4x1), timing block (Timing_block), and BCD to 7-segment decoder (bcd_7) to drive the four 7-segment displays.
- Key Features:
  - Inputs:
    - Four 4-bit inputs (input1, input2, input3, input4) that represent the four hexadecimal or decimal digits.
    - A clock signal and a resetting signal.
  - Outputs:
    - output_anode: Controls which 7-segment display is active.
    - output_cathode: The 7-bit signal that drives each segment of the display.
  - Connections:
    - Instantiates the mux4x1, Timing_block, and bcd_7 components, wiring them together to form the complete display system.

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2. Timing Block (Timing_circuit. vhd)

- Purpose: The Timing_block generates the timing signals required to control the multiplexing of the four 7-segment displays. It divides the 100 MHz clock to generate a slower clock for refreshing the displays and outputs the signals for selecting which input is active at any time.
- Key Features:
  - Clock Division:
    - Divides the 100 MHz clock to a 1 kHz clock using a counter.
  - Multiplexer Select Signal (mux_select):
    - A 2-bit signal that cycles through the four inputs at the refresh rate, ensuring each 7-segment display is active one at a time.
  - Anode Signals:
    - Generates the output_anode signal, which is used to control which display is active at any given time.
  - Reset Functionality:
    - Resets the counter and clock signals when the reset signal is active.

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3. Multiplexer (mux4x1.vhd)

- Purpose: The mux4x1 component is a 4:1 multiplexer that selects one of the four 4-bit inputs based on the mux_select signal provided by the timing block.
- Key Features:
  - Inputs:
    - Four 4-bit inputs (i1, i2, i3, i4), representing the digits to be displayed on the 7-segment display.
    - sel: A 2-bit signal generated by the Timing_block, determining which input is currently selected.
  - Output:
    - outputkar: A 4-bit output corresponding to the selected input.
  - Functionality:
    - Based on the value of sel, the multiplexer outputs one of the four inputs.

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4. BCD to 7-Segment Decoder (bcd_7.vhd)

- Purpose: The bcd_7 component converts a 4-bit binary-coded decimal (BCD) input into a 7-bit output that drives the seven-segment display.
- Key Features:
  - Input:
    - bcd_input: A 4-bit BCD input representing a single digit (0-9 or A-F).
  - Output:
    - bcd_output: A 7-bit output that corresponds to the 7 segments (a to g) of the display.
  - Logic:
    - The 7-segment display output is generated using Boolean expressions based on the BCD input, controlling which segments are lit for each digit.
    - The segment outputs are determined for each possible BCD input (0-9), ensuring proper display of digits.

Resource Utilization Table:

After synthesizing the design for the Basys 3 FPGA board, the following resources were used:

Resource Type	Used	Available	Utilization (%)
Slice LUTs	121	20800	0.58
- LUT as Logic	121	20800	0.58
- LUT as Memory	0	9600	0.00
Slice Registers	65	41600	0.16
- Register as Flip-Flop	65	41600	0.16
- Register as Latch	0	41600	0.00
F7 Muxes	0	16300	0.00
F8 Muxes	0	8150	0.00
Block RAM (RAMB36/FIFO)	0	50	0.00
Block RAM (RAMB18)	0	100	0.00
DSP Slices	0	90	0.00
Bonded IOBs	29	106	27.36
BUFGCTRL (Clock Buffers)	2	32	6.25

Timing Circuit:

To manage the four-digit display, we designed a timing circuit using the internal clock of the Basys3 FPGA board. We implemented a counter to count the rising edges of the clock signal. After a set number of cycles (we selected a refresh period of 10 ms), the corresponding anode was activated.

The first two bits of the binary counter value were used to select which of the four displays (anodes) was activated at any given time. A multiplexer (MUX) filtered the input bits according to the active anode. The output from the combinational logic determined the correct signals for the cathodes based on the selected anode.

Test Cases and Results:
We developed a VHDL testbench to simulate and verify the design. After confirming the simulation results, we implemented the design on the Basys3 board. We manually verified the outputs for a few test cases and observed no flicker during the transitions. All test cases showed the correct output. We successfully designed and implemented a 4-digit hexadecimal/decimal display using the Basys 3 board's 7-segment displays.

References

- Basys 3 Reference Manual
- IEEE VHDL Reference Manual
- Online VHDL tutorials for combinational logic design