Experiment-3: DESIGN AND ANALYSIS OF TWO -STAGE DIFFERENTIAL AMPLIFIER

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Objectives:

Design and Analysis of TWO STAGE- Differential Amplifier for the given specifications.

- Vdd = 1.8V
- Av >= 1000, 60dB
- Phase Margin>=60^0
- CL = 2pF
- ICMR (+) = 1.6V
- ICMR (-) = 0.8V
- Slew Rate = 20V/usec
- Power dissipation < 0.3 mW
- GBW >= 30MHz

Tools Used:

Cadence Software: TSMC 180 nm module

Theory:

A two-stage differential amplifier is a type of electronic amplifier that amplifies the difference between two input signals while suppressing any voltage common to both inputs. A two stage amplifier can provide high gain and high output swing. First stage is a Differential Amplifier which is an Analog circuit with two inputs Vin+ and Vin- and one output Vout which is proportional to the difference between the two inputs. The second stage is a Common Source Amplifier.

Two-Stage Configuration:

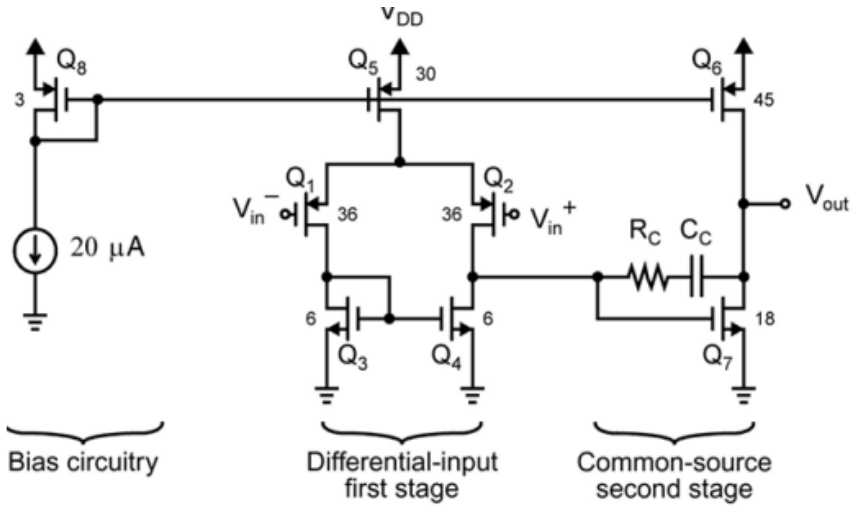
In a two-stage differential amplifier, two operational amplifiers (op-amps) are used in sequence. The first stage is typically a non-inverting amplifier, and the second stage is a differential amplifier. This configuration increases the gain and input resistance of the amplifier.

First Stage: Non-Inverting Amplifier:

The first stage amplifies the input signal without inverting it. The gain of this stage is determined by the feedback resistors used in the circuit. The output of the first stage becomes the input for the second stage.

Second Stage: Differential Amplifier

The second stage amplifies the difference between the two input signals The differential gain of this stage is also determined by the resistors in the circuit. The overall gain of the two-stage differential amplifier is the product of the gains of the individual stages.

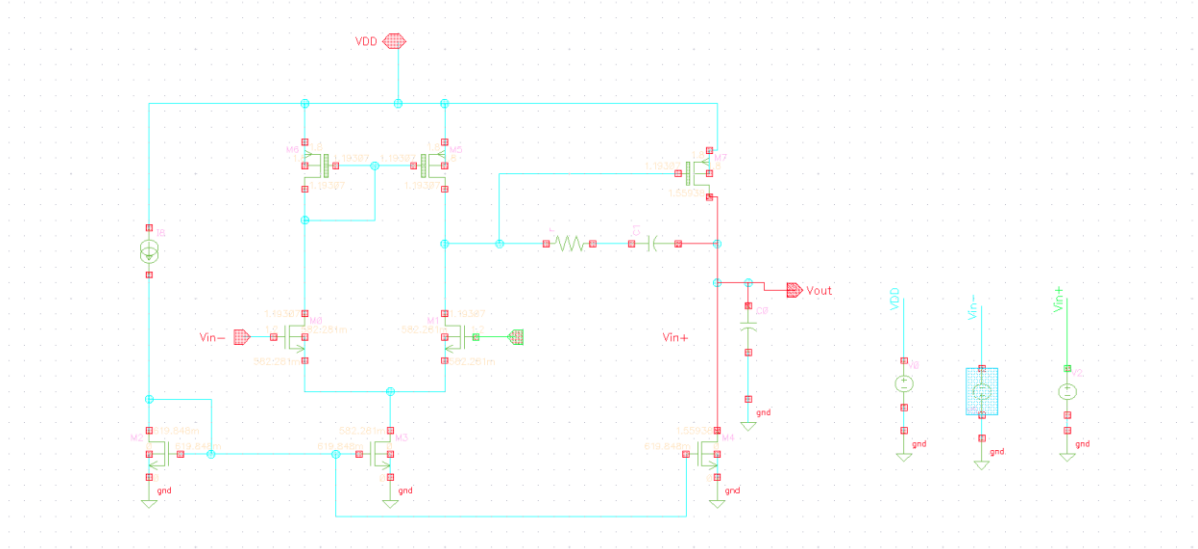


Two - stage Differential Amplifier

Gain of the differential amplifier is the product of transconductance of M1 and Rout Ad = gm1 { rds2 || rds4 }

While that of CS stage is Av = gm7 { rds6 || rds7 }

Circuit Diagram:



Circuit Diagram for Two Stage- Operational Transconductance Amplifier/Two- stage Differential Amplifier

Calculations:

Assuming $L = 400nm$

→ Now we know for phase margin $C_c \geq 0.22 \times 2pF$

$C_c \geq 0.44pF$

Assuming $C_c = 1pF$

→ Slew rate $= \frac{I_5}{C_c}$ → $I_5 = (S.R) \cdot C_c$

$= 20M \times 1 \times 10^{-12}$

$\boxed{I_5 = 20\mu A}$

→ Gain. B.W $= \frac{g_{m1}}{C_c}$

→ $g_{m1} = 30M \times 1P \times 2\pi$

$g_{m1} = 188.495\mu$

→ $g_{m1} = \sqrt{2 I_D (\mu_n C_{ox}) \cdot \left(\frac{W}{L}\right)_1}$

$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{2 I_D k_n} = \frac{(188.495)^2}{2 \times 10\mu \times 290\mu}$

$\boxed{\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{1.225}{0.4}}$

→ $ICMR^+ = V_{DD} - V_{SD3} + V_{tn}$

$1.6 = 1.8 - V_{SD3} + 0.49$

$V_{SD3} = 0.2 + 0.49$

$\boxed{V_{SD3} = 0.69}$

$$I_D = \frac{1}{2} k_p \left(\frac{W}{L}\right) (V_{SG3} - V_{thp})$$

$$\left(\frac{W}{L}\right) = \frac{2 I_D}{k_p (V_{SG3} - V_{thp})} = \frac{2 \times 104}{78.4 \times 4 (0.69 - 0.5)^2}$$

$$\boxed{\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_3 = \frac{2.824}{0.4}}$$

→ $ICMR^- = V_{GS1} + V_{DSAT}$

$$V_{GS1} = \sqrt{\frac{2 I_D}{k_n \left(\frac{W}{L}\right)}} + V_{thn} = \sqrt{\frac{2 \times 104}{290 \mu \times \left(\frac{1.225}{0.4}\right)}} + 0.490.$$

$$V_{GS1} = 0.64$$

$$V_{DSAT} = 0.8 - 0.64 = 0.16$$

Now, $I_{D5} = \frac{1}{2} k_n \left(\frac{W}{L}\right) \cdot (V_{DSAT})^2$

$$\left(\frac{W}{L}\right)_5 = \frac{2 I_{D5}}{k_n (V_{DSAT})^2} = \frac{2 \times 104}{290 \mu \times (0.16)^2}$$

$$\boxed{\left(\frac{W}{L}\right)_5 = \frac{2.155}{0.4}}$$

Given Power $\leq 200\mu W$

$$(1.8) \cdot (I_D + I_5 + I_8) \leq 300\mu$$

$$(I_D + I_5 + I_8) \leq 166.66\mu$$

$$I_D + I_5 + 20\mu \leq 160$$

Assume $I_D = 20\mu$, $I_5 = 20\mu$

$$\Rightarrow I_6 = 100\mu - I_7$$

By current mirror

$$\frac{\left(\frac{W}{L}\right)_7}{I_7} = \frac{\left(\frac{W}{L}\right)_5}{I_5}$$

$$\Rightarrow \left(\frac{W}{L}\right)_7 = 5 \times \left(\frac{2.155}{0.4}\right) = \frac{10.775}{0.14}$$

Now by $I_D \propto \frac{W}{L} \propto g_m$

$$\frac{g_{m6}}{\left(\frac{W}{L}\right)_6} = \frac{g_{m4}}{\left(\frac{W}{L}\right)_4} \Rightarrow g_{m4} = \sqrt{(\mu_p C_{ox}) \cdot \left(\frac{W}{L}\right) \cdot 2 \cdot I_D}$$

$$g_{m4} = \sqrt{(79.057)\mu \cdot \left(\frac{2.424}{0.4}\right) 2 \times 10\mu}$$

$$g_{m4} = 105.252\,\mu S$$

$$\Rightarrow \left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{g_{m4}} \times \left(\frac{W}{L}\right)_4$$

$$\left(\frac{W}{L}\right)_6 = \frac{1900}{105.25} \times \left(\frac{2.424}{0.4}\right)$$

$$\boxed{\left(\frac{W}{L}\right)_6 = \frac{50.978}{0.4}}$$

$$R_C = \frac{1}{g_{m6}}$$

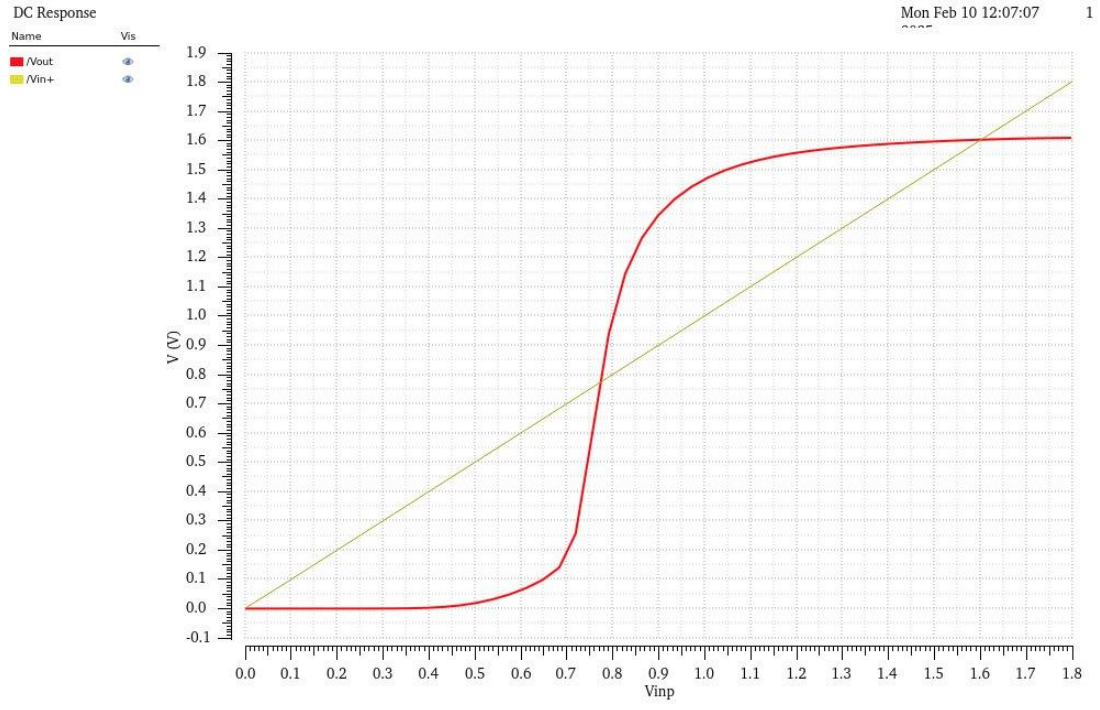
$$\boxed{R_C \approx 2k}$$

Observations:

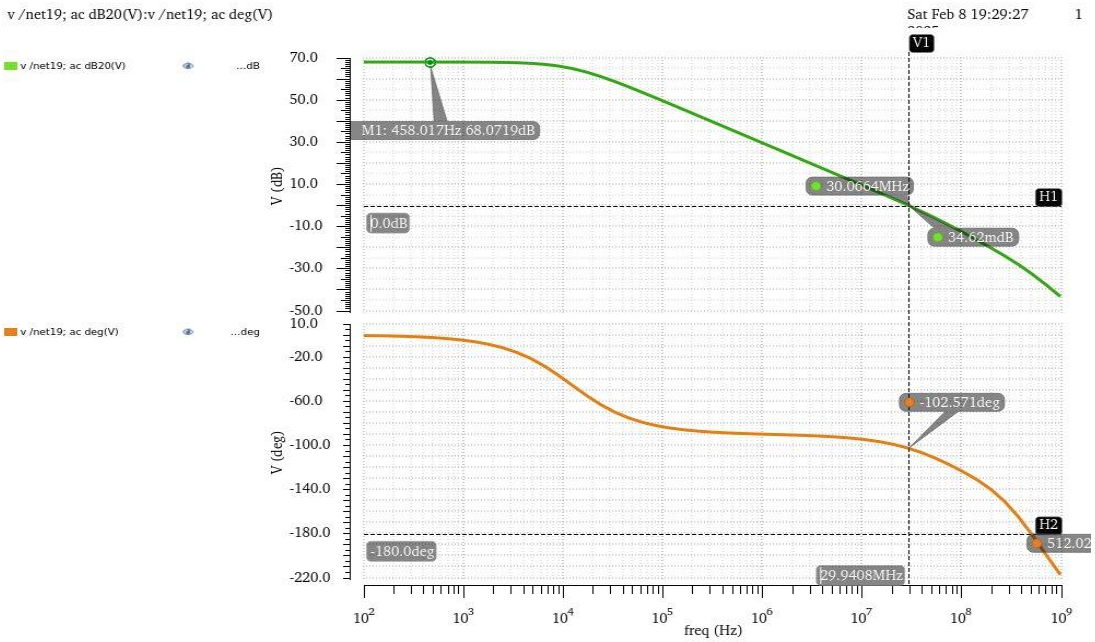
From the circuit diagram, the theoretical and practical values are

Parameter	Theoretical	Practical
(W/L)1	1.225/0.4	1.225/0.4
(W/L)2	1.225/0.4	1.225/0.4
(W/L)3	2.824/0.4	4/0.4
(W/L)4	2.824/0.4	4/0.4
(W/L)5	2.155/0.4	2.155/0.4
(W/L)6	50.978/0.4	50.1/0.4
(W/L)7	10.775/0.4	11/0.4
Rc	2k ohms	2k ohms
Cc	1p F	1p F
I5	20u A	19.929u A
Gm1	188.485u	105.138u
Gm2	105.252u	1.12902u

Results and Discussions:

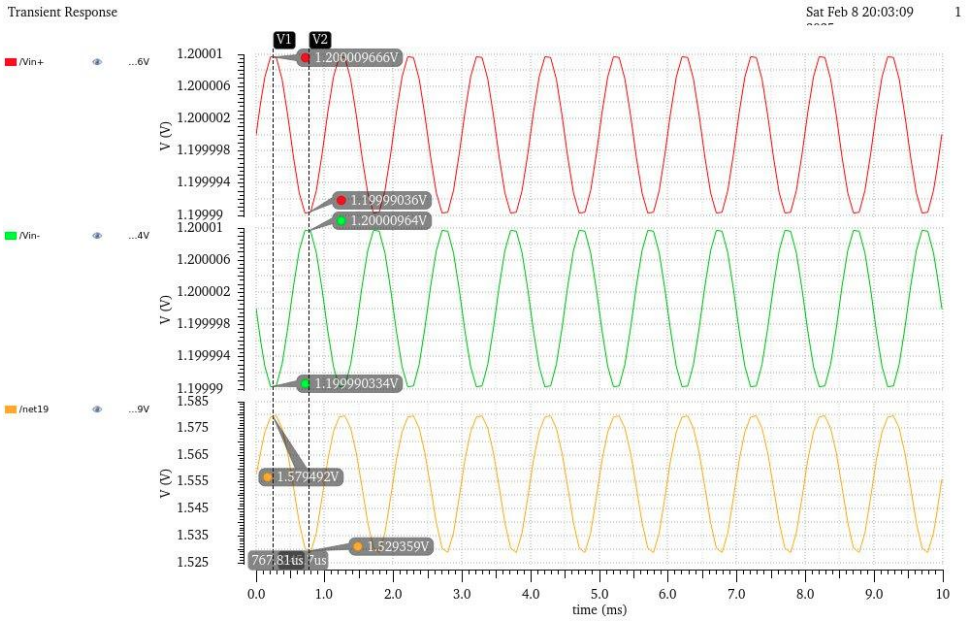


1.DC Response of Two stage Differential Amplifier



2.AC Response of Two- stage Differential Amplifier

Here we observe the Gain (in dB) and the Phase of the Vout . We are getting a gain of about nearly 68dB for 0deg phase shift. We have achieved a GBW of 30.0664MHz.



3.Transient Analysis of Two-stage Differential Amplifier

From here we observe that our Circuit produces an Vout which sweeps between (approx.) 1.52935V to 1.579492V. Because we maintained the output DC operating point so that the output signal could swing without requiring any transistors to enter the triode or cutoff zone of operation, we are able to notice no clipping in the Vout waveform.

The power dissipated by our design. We can observe that our design dissipates about 287.96 uW of power, which is under the design requirement of 300uW. We achieved this by utilising a 1:2 ratio which allowed us to decrease the current requirement thus decreasing the power dissipated.

Conclusion:

We accomplished the experiment's goals and obtained a gain of 68 dB at a power consumption of around 287.96 uW. In order to allow for a bigger VDS drop across them, we controlled for the ICMR range by maintaining a higher aspect ratio of the pmos load and a lower nmos current source. This permits the circuit to operate at saturation for the specified ICMR. we improved the gain and GBW by having a very high aspect ratio since this allowed us to have a high transconductance, which in turn produced a high gain and GBW.