Channel noise reduction of image in FPGA

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1 Aim

The aim of the project is to reduce the noise introduced by channel in image using fpga.

2 Introduction

In the project we have generated a noise reduction filter and placed in fpga for a particular channel.when we pass the image through fpga we get the filtered output.

2.1 FPGA

FPGA is an integrated circuit designed to be configured by a customer or a designer after manufacturing.FPGAs contain an array of programmable logic blocks, and a hierarchy of ”reconfigurable interconnects” that allow the blocks to be ”wired together”, like many logic gates that can be inter-wired in different configurations.

3 Hardware

For this project we used

- 2 arduino boards(to send and receive input and output from FPGA)
- ico board(ico board is a FPGA based IO board for RaspberryPi)
- Rasberrypi

4 process

4.1 Generating filter

To generate the filter we need one noise free image and same image with channel noise.Using 2D-LMS algorithm we generated the filter.First we took a filter with some random values and filtered the image using this random filter and then updated the filter using the error(difference between original image and filtered image.This updating was done till we reach some min error.

calculations involved are: u(i,j) is the input pixel of image, w(t,l) is the filter coefficients, and N1 and N2 specify the order of the FIR filter(we took N1 and N2 as 3 in our project).

$$\mathbf{W}_k(i,j) = \begin{bmatrix} w(0,0) & \cdots & w(0, N_2 - 1) \\ \cdots & \ddots & \cdots \\ w(N_1 - 1, 0) & \cdots & w(N_1 - 1, N_2 - 1) \end{bmatrix}$$

$$\mathbf{U}_k(i,j) = \begin{bmatrix} u(i,j) & \cdots & u(i, j - N_2 + 1) \\ \cdots & \ddots & \cdots \\ u(i - N_1 + 1, j) & \cdots & u(i - N_1 + 1, j - N_2 + 1) \end{bmatrix}$$

- convolve U_k and W_k
- calculate difference of above convolved result with same pixel in noise free image which gives the error.
- $W_{updated} = W_{present} + 2seU_k$
  s-stepsize,e-error

This filter is placed in fpga

4.2 Sending Image to fpga

The image to be filtered is first sent to arduino and there the pixel values are converted to binary and are sent to the ico board through I/O pins.The pixel values are sent from the system to arduino through serial communication.we have set our own clock in arduino which makes the ico board to read only when the input was sent and we have set one reset pin wchich will reset all values in icoboard to zero.

4.3 Process in Ico board

In icoboard we applied the filter to image by convolving it with filter

4.4 output from FPGA

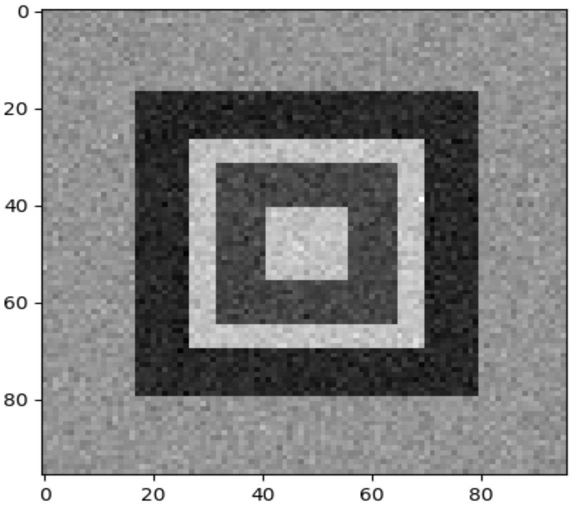
we read the output from FPGA using arduino and we reform the filtered image using python script.In the python script we have taken the output values from arduino through serial communication and converted the to integers.Then these values are reshaped to form the output image.In Fpga we are sending a signal which becomes high when the output calculations are done in fpga.THis signal makes the arduino to read the correct output.

4.5 Codes used

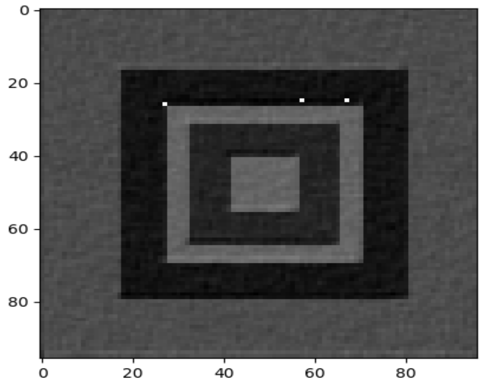
All the codes used in the project are there in this link:
`https://github.com/kesanamani/fpga_project`

4.6 Results

INPUT NOISE IMAGE



DENOISED IMAGE



4.7 Reference

1)https://ieeexplore.ieee.org/document/5941155
2)https://github.com/gadepall/EE5811/tree/master/icoboard_fpga
3)https://www.researchgate.net/publication/288107539_Image_denoising_with_two-dimensional_adaptive_filter_algorithms