Venkata Naga Sai Pranathi Reddy Janapala

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Professional Summary

Design Verification Engineer with 1+ year of ASIC DV experience building UVM testbenches, SystemVerilog Assertions (SVA), and coverage-driven verification for AMBA/DDR-class interfaces. Proven record of owning regression stability, driving coverage closure, and closing protocol/spec compliance gaps by isolating root-cause RTL defects and preventing escape issues through assertion-based and constrained-random verification.

Education

- **M.S. Computer Engineering**, University of North Carolina at Charlotte — Aug 2024 – May 2026
- **B.Tech. Electronics & Communication Engineering**, Sridevi Women's Engineering College — Jul 2019 – Jul 2023

Experience

- **Graduate Assistant – ASIC / RTL Verification** — **Aug 2024 – Present**
  University of North Carolina at Charlotte — *Charlotte, NC*
  - Owned end-to-end verification of a 1×3 packet router; built reusable UVM components (driver, monitor, scoreboard, sequencer) and functional coverage model enabling deterministic debug and signoff readiness.
  - Drove coverage closure by +20% by identifying missing scenarios and adding targeted constrained-random sequences; uncovered 15 critical RTL defects impacting arbitration and FIFO flow control.
  - Reduced debug turnaround time by 30% by building a repeatable failure-triage flow (waveform analysis, assertions, scoreboard mismatches), accelerating regression stabilization.
- **Design Verification Engineer** — **Aug 2023 – Feb 2024**
  Synaptics — *Hyderabad, India*
  - Closed I2C Controller IP compliance gaps by developing SVA checks and constrained-random tests across 100/400 kbps modes, preventing protocol escapes and ensuring spec compliance.
  - Improved regression quality by +35% coverage through parameterized UVM agents (multi-master arbitration, clock stretching) and spec-aligned corner-case scenarios.
  - Unblocked integration by partnering with design to root-cause RTL issues from assertion failures and validating fixes via clean regressions and coverage closure.
- **Design Verification Engineer** — **Feb 2023 – Jul 2023**
  Sumedha IT Solutions — *Hyderabad, India*
  - Owned AMBA AXI3 and AXI-Lite verification plan and execution; implemented burst, ID, ordering, and response checks ensuring protocol correctness prior to subsystem handoff.
  - Reduced debug cycle time by 20% via cross-functional RTL triage (assertions, scoreboard mismatches, waveform analysis), improving regression stability and closure velocity.
  - Achieved 88% functional coverage by adding directed tests for hard-to-hit scenarios and aligning bins to protocol specifications.
- **VLSI Design Trainee** — **Aug 2022 – Jan 2023**
  Semi Design Training Program — *Hyderabad, India*
  - Verified a single-cycle RISC-V processor using directed and random tests; achieved 100% instruction accuracy through systematic waveform debugging and golden-model validation.

Projects

- **DDR3 Controller DV (Behavioral DRAM Model):** Built UVM environment with 4-bank behavioral DRAM; implemented functional coverage and corner-case tests (refresh, timing windows, protocol ordering).
- **Protocol Verification (AXI4 / AHB / APB):** Created 25+ constrained-random sequences and protocol checkers; validated burst handling, backpressure, and response scenarios using assertions and scoreboards.
- **AXI4-Lite Router (1×3):** Designed UVM testbench and coverage model; generated 50+ routing tests validating boundary and negative cases to improve regression robustness.

Technical Skills

Verification: UVM, SystemVerilog, SVA, Coverage-Driven Verification, Constrained-Random Testing, Scoreboards/Monitors, Test Plans, Regression Triage
Languages/Scripting: SystemVerilog, Verilog, C, Python, Tcl, Linux
Tools: Synopsys VCS, Verdi, QuestaSim/ModelSim, JasperGold, Cadence Xcelium, DVE
Protocols: AMBA (AXI/AXI-Lite/AHB/APB), I^2C, SPI, DDR3/DDR4