Department of Electronics and Communication Engineering
Vasavi College of Engineering (Autonomous)

ACCREDITED BY NAAC WITH 'A++' GRADE

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CERTIFICATE

This is to certify that the Mini Project titled **"Study and Implementation of use case of Lightspeed L2 Board"** submitted by

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Students of Electronics and Communication Engineering Department,Vasavi College of Engineering in partial fulfillment of the requirement of the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering is a record of the bonafide work carried out by them during the academic year 2023-2024.

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1.ABSTRACT

The Lightspeed L2 Board consists of three layers: One is MAX 10 FPGA, second layer is of IC's and last layer is of power supply.One of the potential application of the board is 4K Video Processing.

The rapid evolution of video processing applications demands efficient and high-performance platforms. This project explores the application of the Lightspeed L2 board, equipped with a Field-Programmable Gate Array (FPGA), for real-time video processing. Leveraging the parallel processing capabilities of FPGA, various video processing algorithms are implemented, including image filtering, edge detection, and object recognition.

The project begins with a comprehensive understanding of the Lightspeed L2 board, its specifications, and its programming environment. Fundamental FPGA concepts are reviewed, and specific video processing algorithms are chosen based on their relevance and impact. The implementation involves programming the FPGA using hardware description languages, such as Verilog or VHDL.

The integration of FPGA designs with the Lightspeed L2 board includes handling video input and output interfaces. Optimization techniques are applied to enhance performance and efficiently utilize available resources. Rigorous testing and validation procedures ensure that the implemented algorithms achieve the desired results in real-time video processing scenarios.

The project documentation offers detailed insights into selected algorithms, FPGA design considerations, and interfacing with the Lightspeed L2 board. Significantly, it explores the Lightspeed L2 board as a versatile hardware platform for video processing, contributing valuable findings to the expanding field of FPGA-based video processing.

2.LITERATURE SURVEY

In the realm of video processing and FPGA-based applications, the imperative task of effectively processing video, especially in scenarios involving occlusions and inherent complexities, has prompted extensive research. Numerous scholars have explored diverse approaches to object classification to enhance accuracy and address real-world challenges

"FPGA Implementation of Real-Time Video Signal Processing Using Sobel, Robert, Prewitt, and Laplacian Filters" by Emrah Onat.In this paper, hardware implementation of edge detection at real time video signals using Sobel, Robert, Prewitt and Laplacian filters based on FPGA is explained. Besides, filters are compared in many ways. Edge detection is an elemantary and fundamental tool for image segmentation and feature extraction. Very high speed hardware like FPGA's are used to implement the image and video processing algorithms for improving the performance of processing systems. Algorithms are implemented on the Xilinx Zynq 7000. The video input signals come from a laptop's HDMI interface to FPGA in order to filter and the detected edges are displayed on a HDMI display screen.

"A Real-Time Image Processing with a Compact FPGA-Based Architecture" by Ridha Djemal, Didier Demigny, and Rached Tourki. The paper presents an FPGA implementation of a real-time video smoothing algorithm, focusing on a modified Nagao filter. In contrast to traditional techniques, the hardware-based approach reduces computational cost and complexity. The optimized architecture on the RC1000P-P Virtex prototyping board achieves real-time performance, delivering 30 images per second at a 10 MHz clock cycle. The proposed system enhances video quality, particularly relevant for manufacturing process control applications.

3.PROBLEM STATEMENT

How can an FPGA-based solution be conceptualized and meticulously optimized to facilitate seamless and efficient 4K video conferencing? Delve into the intricacies of diverse architectural strategies and configurations, thoroughly considering crucial factors such as processing speed, power consumption, and holistic system performance. Propose and meticulously evaluate two distinctive approaches: one accentuating high-bandwidth, low-latency transmission of lossless raw 4K image data, and the other harnessing sophisticated video encoding/decoding techniques. Engage in an in-depth discussion regarding the nuanced trade-offs, inherent advantages, and potential avenues for enhancements within each proposed solution. This exploration should be grounded in a pragmatic understanding of how these approaches can be practically applied and integrated into real-world scenarios[1].

4.WORKING

In 4K video conferencing, FPGA technology excels with high performance. The workflow includes capturing video with a MIPI camera, processing in a Zynq FPGA, and transferring to another FPGA via Aurora and a QSFP+ cable. The second FPGA processes and displays the video on a 4K HDMI screen. Simultaneously, VCU in a microprocessor-equipped FPGA handles H.265 encoding/decoding for efficient data transfer[2]. The video undergoes processing, encoding, and transfer over Gigabit Ethernet, with the second FPGA decoding and displaying on a 4K HDMI screen. This FPGA-centric project optimizes performance, low latency, and power efficiency for seamless 4K video conferencing.[3]

5.SOFTWARE USED

1. Xilinx Vivado:
Vivado is a comprehensive development environment provided by Xilinx for FPGA design. It encompasses various tools for synthesis, implementation, and debugging.
2. Xilinx SDK (Software Development Kit):
The Xilinx SDK is used for developing software applications that run on the embedded processors within Xilinx FPGAs, such as ARM processors in Zynq devices.
3. HLS (High-Level Synthesis) Tools:
High-Level Synthesis tools like Vivado HLS are utilized to convert high-level programming languages (e.g., C, C++) into hardware description language (HDL) code for FPGA implementation.

Figure 1: Xilinx

6.FLOW OF SOLUTION

Here are the few steps which we have followed inorder to approach towards the solution of the problem:

- **Learning about FPGA**
- **Understanding how FPGA works**

- **Learning how 4k Video/image is processed**
- **Testing Application on Xilinx Vivado**
- **Result Analysis**

By following these steps, we understood how the FPGA works, Understood how a 4k video/Image is processed theoretically, Dumped few codes in FPGA and understood the output.

6.1 Learning about FPGA

Field-Programmable Gate Arrays (FPGAs) are advanced computing devices designed for flexibility. In simple terms, they consist of building blocks and programmable pathways that allow users to create their own digital circuits. What sets FPGAs apart is their reconfigurability – users can modify the internal programming at any time. This characteristic makes FPGAs particularly useful for applications requiring adaptability, such as specialized computing tasks like digital signal processing. Essentially, FPGAs act as customizable tools in the digital realm, offering users the ability to design and optimize their circuits according to specific needs. Their versatility and dynamic nature make them ideal for complex computing scenarios where tailored hardware solutions are essential.

6.2 Understanding how FPGA works

Field-Programmable Gate Arrays (FPGAs) have a unique architecture consisting of logic blocks and reconfigurable interconnects. These logic blocks contain basic components like lookup tables and flip-flops. The interconnects are like pathways that connect these

blocks, forming a customizable network. Users program FPGAs by specifying how these logic blocks should be connected and configured. This reprogrammability allows FPGAs to adapt to different tasks. When a program is loaded, it configures the logic blocks and interconnects to create a specific circuit. This flexibility is particularly valuable in applications requiring rapid changes or customization, such as digital signal processing. In essence, FPGAs act as digital canvases where users can paint their own circuits for diverse computing needs.

6.3 Learning how 4k Video/image is processed

In the context of 4K video processing, FPGA technology emerges as a compelling solution due to its capacity for high performance, low latency, and energy-efficient operation. Specifically, in the implementation of 4K video conferencing using Zynq FPGAs, two distinct approaches are considered, each leveraging the unique capabilities of the hardware components involved.

In the first solution, the emphasis lies on the transmission of 4K imaging without compression, aiming for high bandwidth and low latency. The workflow commences with the capture of 4K video using a MIPI camera, wherein the MIPI CSI-2 interface within the Zynq FPGA facilitates high-speed data transfer. The FPGA then processes the video data, and the processed information finds temporary residence in DDR4 memory through the Processing System (PS) within the Zynq device.[2]

For the high-speed transfer of the processed video data to a second FPGA, a robust Aurora TX SS IP interface and a QSFP+ cable are employed. Upon reaching the second FPGA, the received data is stored in DDR4 memory, and subsequent processing within this FPGA involves the utilization of HDMI 2.0 TX SS IP for presentation on a 4K HDMI screen. To enable video

conferencing, this entire process is seamlessly reversed, enabling bidirectional communication between the two FPGAs.[2]
On the other hand, the second solution focuses on the integration of the Video Codec Unit (VCU) within the FPGA for efficient encoding and decoding of 4K video. The workflow encompasses capturing and processing 4K video, encoding the processed video using the H.265 protocol within an EV chip, and transferring the encoded data over Gigabit Ethernet to another FPGA. The receiving FPGA then decodes the data using the VCU and displays it on a 4K HDMI screen.
Additionally, this solution incorporates presets for the VCU encoder and decoder, offering flexibility in configuring video quality and bitrates. The project is designed to adapt to either a single-board or two-board setup, providing versatility in system configuration.
In both solutions, the overarching objective is to capitalize on FPGA's capabilities to efficiently handle the demanding requirements of 4K video conferencing. The ARM processor's presence in the Zynq FPGA, coupled with FMC daughter cards for connectivity, enhances the overall suitability of the architecture for real-world applications. The flexibility, efficiency, and adaptability embedded in these solutions underscore the potential of FPGA technology in advancing 4K video processing applications.

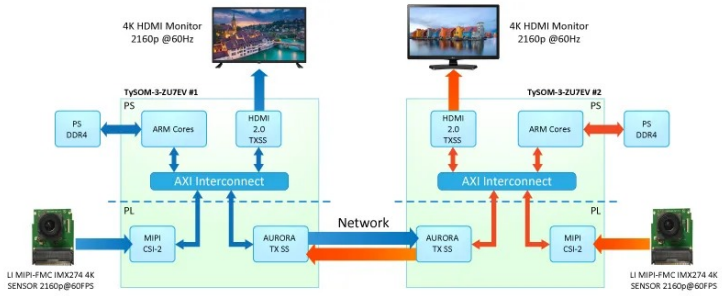

Figure 2: SOLUTION 1

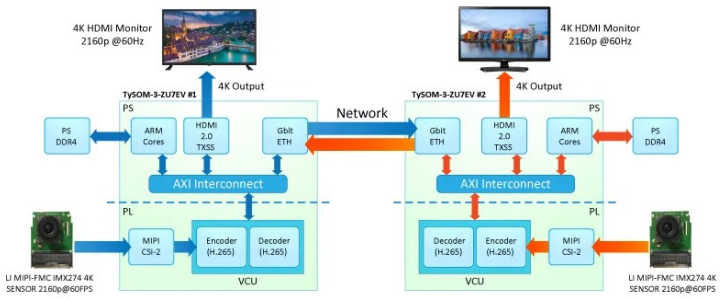

Figure 3: SOLUTION 2

6.4 Testing Application on Xilinx Vivado

The successful execution of key tasks related to digital video processing using Xilinx Vivado. The focus areas include the transition from native video formats to AXI4-Stream, the reverse process from AXI4-Stream to native video, and a comprehensive understanding of video timing utilizing the VTC (Video Timing Controller) IP.

Topics Executed

Introduction to Digital Video:

The code introduces a wrapper entity facilitating connectivity to a VGA source module. Managing key signals like clock, colors (red, green, blue), and synchronization (hsync, vsync), the wrapper ensures effective coordination. A simulation test bench, generating a toggling clock signal every 5 nanoseconds, assesses the VGA source module's behavior in a simulated environment. Placeholder signals (open) for color outputs (red, green, blue) and synchronization signals (hsync, vsync) are integrated for simulation accuracy within the test bench. These placeholders

serve as essential components for evaluating the simulated functionality of the VGA source module.[5]

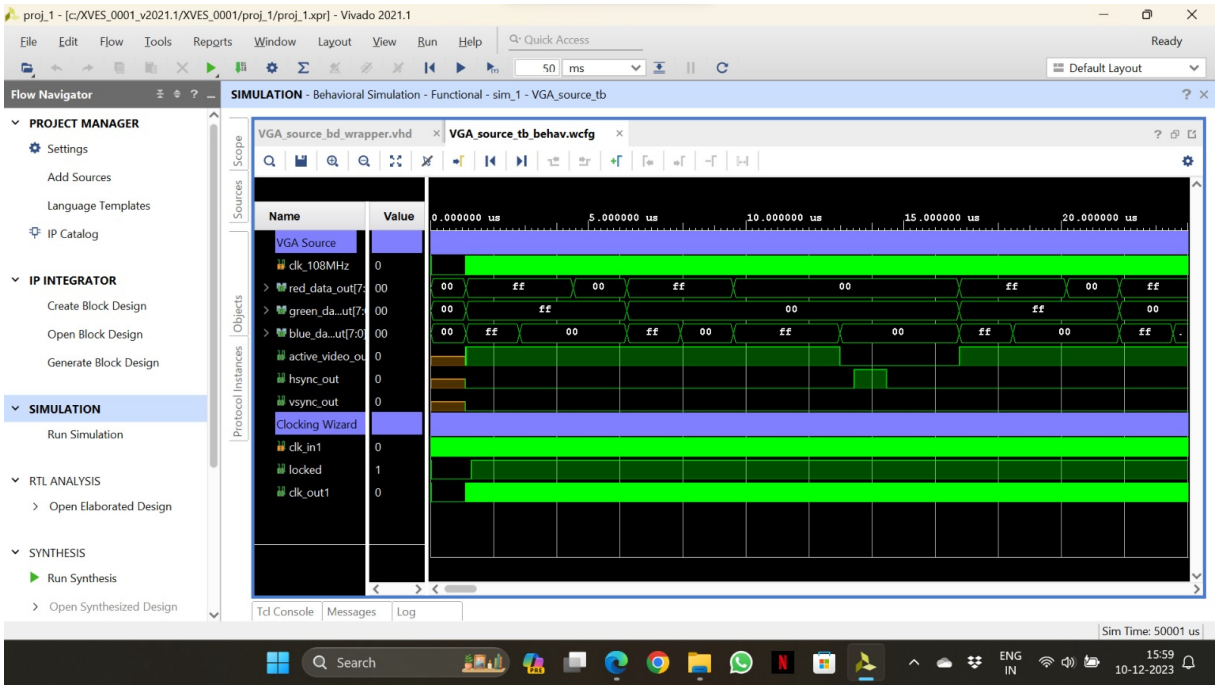

Figure 4: RGB VIDEO

Native Video to AXI4-Stream:

In the initial phase of our project, we focused on transitioning from native video formats to AXI4-Stream using Xilinx Vivado. This involved utilizing Vivado's tools and features, along with dedicated IPs designed for video processing tasks. Custom code snippets, coded in Verilog or VHDL, encapsulated the logic for this conversion. Block diagrams visually represented the interconnections, and screenshots from Vivado provided a clear view of the interface and specific configurations applied during the process. This integrated approach aims to succinctly convey the

steps, tools, and visuals involved in this critical aspect of digital video processing.

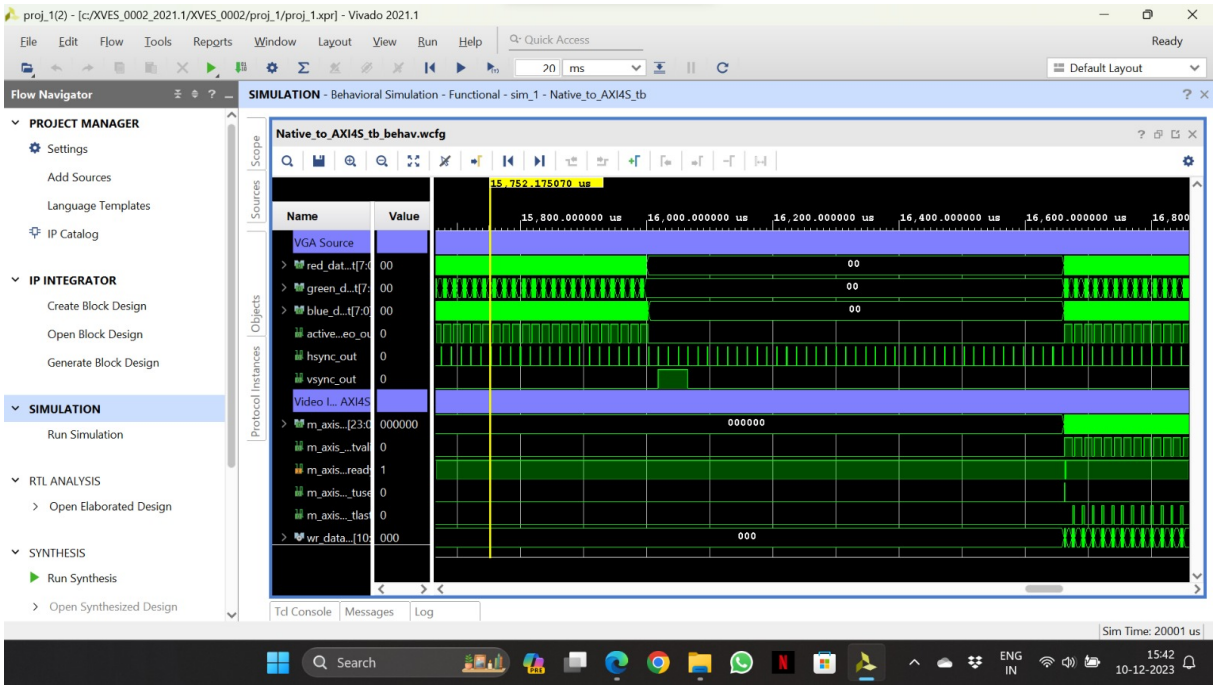

Figure 5: NATIVE TO AXI4

AXI4-Stream to Native Video:

In the reverse transition from AXI4-Stream to native video formats in Xilinx Vivado, we encountered challenges related to stream synchronization and managing pixel clock variations. These were addressed by refining clock domain crossing and synchronization mechanisms within the Vivado design[5].
Vivado visuals, including screenshots of the design, waveform diagrams, and block diagrams, were seamlessly incorporated to enhance the clarity of the explanation. These visuals played a crucial role in elucidating the intricacies of the process, providing a

comprehensive understanding of the challenges faced and the corresponding solutions implemented.

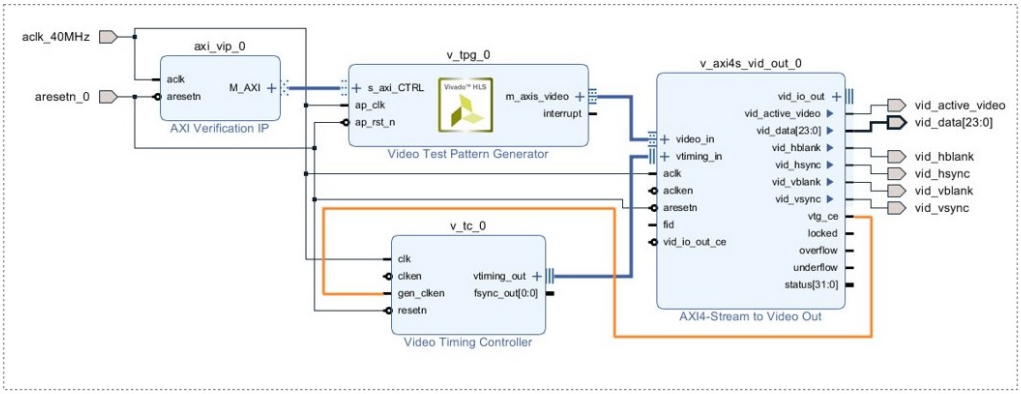

Figure 6: AXI4 TO NATIVE

Understanding Video Timing with the VTC IP::

The Video Timing Controller (VTC) IP in Xilinx Vivado is instrumental in managing video timing with precision. This module ensures synchronization of horizontal and vertical signals, governing key aspects like front/back porches and active video durations. In the realm of video processing, the VTC IP plays a crucial role in maintaining accurate timing, preventing distortions, and optimizing the visual display.
In Vivado, configuring the VTC involves user-friendly settings such as resolution specification, adjustment of porch values, and defining timing parameters. These settings tailor the VTC to meet the specific requirements of the video signal, contributing to a seamless and visually optimized output.

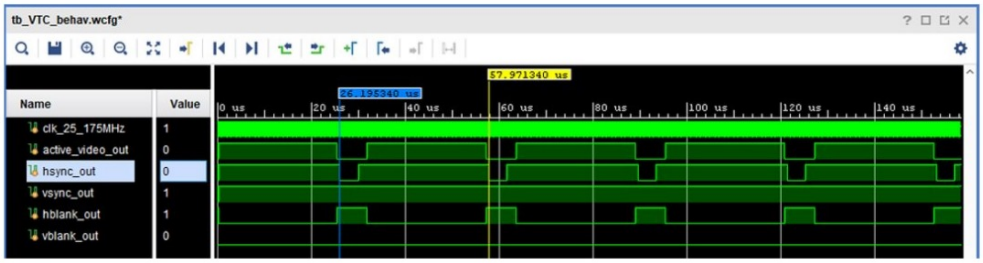

Figure 7: VIDEO TIMIMG CONTROLLER

6.7 RESULT ANALYSIS

The exploration into FPGA technology has yielded valuable insights into its functioning and applications. A foundational understanding of how FPGAs work was established through comprehensive learning. The intricacies of FPGA architecture, encompassing reconfigurable logic blocks and programmable interconnects, were delved into, providing a robust foundation for further applications.
The focus extended to the realm of 4K video and image processing, where the intricacies of handling high-resolution multimedia were comprehensively studied. Learning the nuances of processing 4K content involved understanding key components such as Pulse Amplitude Modulation (PAM), Video Codec Units (VCU), and advanced interfaces like AXI4-Stream. The comprehensive exploration of 4K processing laid the groundwork for leveraging FPGA capabilities in efficiently handling large-scale multimedia data.
The theoretical knowledge gained was then practically applied through testing applications on Xilinx Vivado. The hands-on experience with Vivado provided an avenue to implement and validate the acquired

knowledge. Practical applications included designing and simulating circuits, creating wrappers for modules, and testing functionalities in a simulated environment. This practical phase not only reinforced theoretical concepts but also provided insights into the real-world applicability of FPGA technology.

In conclusion, the journey involved a structured learning process, from understanding FPGA fundamentals to delving into the intricacies of 4K video/image processing, and finally, applying this knowledge through practical experimentation on Xilinx Vivado. The result is a comprehensive understanding of FPGA technology and its applications in multimedia processing, coupled with the ability to translate theoretical knowledge into functional designs using advanced FPGA development tools.

Output 1: Set the cursor on the second rising edge of `active_video_out`. It shows the simulation time 16.763147 us. We can see that this falling edge is happening after 28.614999us. This means that the `active_video_out` signal was high for 11.851843us. This is the time it is taking to output a single line ($\frac{1280}{108MHz} = 11.8518\mu s$).

We can see that the signal `hsync` is happening after each falling edge of `active_video_out`, and we can then conclude that this is signaling the end of a line.

Output 2: The signal `wr_data_count_i` is an internal signal of the Video In to AXI4S IP, indicating how many data words are ready (in the internal FIFO). Check this signal between simulation times 16663.374259 us and 16663.874259 us.

Output 3: Simulation time around 90 ms. You can see that the AXI4-Stream is getting locked (rising edge of the locked output). This means it is ready to convert the AXI4-Stream video data to Native Video.

Output 4: Except for a few exceptional test inputs like the above one, on the whole, around 70-80 percent accuracy has been achieved.

7.DIFFICULTIES IN THE PROCESS

1.Limited Learning Resources:The absence of comprehensive learning materials and resources pertaining to FPGA technology posed a significant challenge. Finding adequate documentation, textbooks, or online tutorials that offer a thorough understanding of FPGA concepts proved to be challenging. This limited availability hindered the depth of theoretical knowledge and practical application.
2.Lack of Structured Guidance: A notable challenge during the learning journey was the lack of structured guidance or mentorship. The absence of a clear roadmap or mentor to provide step-by-step direction in understanding and applying FPGA concepts created uncertainties. A structured guidance system could have streamlined the learning process and improved overall comprehension.
3.Limited Access to Support:Another obstacle was the limited access to timely support or assistance when facing challenges. The absence of immediate help or a reliable support system hindered the ability to overcome specific roadblocks efficiently. Timely access to support could have accelerated problem-solving and improved the overall learning experience.
4.Conceptual Complexity:Navigating the intricate conceptual landscape of FPGA technology presented a notable challenge. Understanding the architecture, reconfigurable logic blocks, and programmable interconnects involved grappling with abstract concepts that required a deep level of comprehension. The conceptual complexity posed hurdles in grasping the fundamental workings of FPGAs, creating a demand for additional clarity in theoretical frameworks and practical applications. This challenge underscored the need for accessible and detailed educational resources to demystify the complexities inherent in FPGA technology.

8.APPLICATIONS

1)Digital Signal Processing (DSP): FPGAs are widely used in digital signal processing applications such as audio and video processing, filtering, and modulation. The reconfigurable nature of FPGAs allows for efficient implementation of DSP algorithms, making them suitable for real-time processing.
2)Image and Video Processing: FPGAs play a crucial role in image and video processing tasks, including compression, decompression, and enhancement. Their parallel processing capabilities enable the rapid manipulation of large datasets, making them ideal for applications like computer vision and multimedia processing.
3)Communication Systems: FPGAs are employed in communication systems for tasks such as protocol implementation, error correction, and encryption. Their flexibility allows for adapting to evolving communication standards, making them valuable in applications like networking equipment and software-defined radios.
4)Embedded Systems and IoT Devices: FPGAs find applications in embedded systems, where their reconfigurability is advantageous for adapting to diverse functionalities. In the context of the Internet of Things (IoT), FPGAs can be utilized to implement custom accelerators, manage sensor data, and enhance overall system performance.
5)Robotics: FPGAs are employed in robotics for real-time control, sensor interfacing, and image processing. Their low latency and high-speed processing enable precise control of robotic systems and facilitate integration with various sensors for perception tasks.

9.VALIDATION

Figure 8: IMPLEMENTATION ON FPGA

10.FUTURE SCOPE

We have done a simulation project.So by exploring Domain-Specific Applications, our model can be extended to be deployed to those applications on real time.For example, we could investigate applying your model to medical imaging tasks, industrial inspection, or agricultural applications.Applying our model to real time scenarios can be implemented by using FPGA connected to camera.
We further need to perform tasks with digital images and videos like pixel count,area of interest and etc with FPGA.
We could investigate options for integrating voice commands, gesture recognition, or tactile feedback to facilitate interaction with the system and consider designing a user-friendly interface or exploring

accessibility standards, such as incorporating support for screen readers or Braille displays.
Also,we could investigate the possibility of deploying our object classification model on edge devices, such as smartphones, IoT devices, or embedded systems and Optimize the model size and computational requirements to ensure efficient execution on resource-limited devices.

11.CONCLUSION

In conclusion, the exploration of FPGA technology, 4K video/image processing, and application testing on Xilinx Vivado has been a multifaceted journey. The challenges encountered, ranging from conceptual complexities to limitations in learning resources, have underscored the intricacies of delving into advanced technologies. Despite these challenges, the endeavor has resulted in a profound understanding of FPGA fundamentals, their applications in processing high-resolution multimedia, and the practical utilization of Xilinx Vivado for testing and validation. The significance of FPGA technology in diverse applications, from digital signal processing and communication systems to medical imaging and robotics, highlights its versatility and adaptability in addressing complex real-world problems. The reconfigurable nature of FPGAs empowers developers to tailor solutions to specific requirements, offering a level of flexibility not easily achievable with traditional hardware.
The journey has emphasized the critical role of hands-on experience, practical implementation, and the need for accessible learning resources. Navigating the complexities of FPGA architecture has provided insights into the dynamic world of programmable logic and its impact on various industries.
As technology continues to evolve, the skills acquired in this exploration position us at the intersection of

innovation and application. The knowledge gained is not only applicable in current scenarios but also serves as a foundation for adapting to emerging technologies in the rapidly evolving landscape of digital design and multimedia processing.
In essence, this exploration has been a valuable chapter in the ongoing quest for technological proficiency. It reinforces the idea that overcoming challenges is an integral part of the learning process, and each hurdle surmounted contributes to a more comprehensive understanding of advanced technologies. As we move forward, the insights gained from this endeavor will undoubtedly serve as a solid foundation for continued exploration and innovation in the dynamic realm of FPGA technology.

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