Project 4 – MOSFET-Based XOR Gate

ELEC 2EI4

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Circuit Schematic

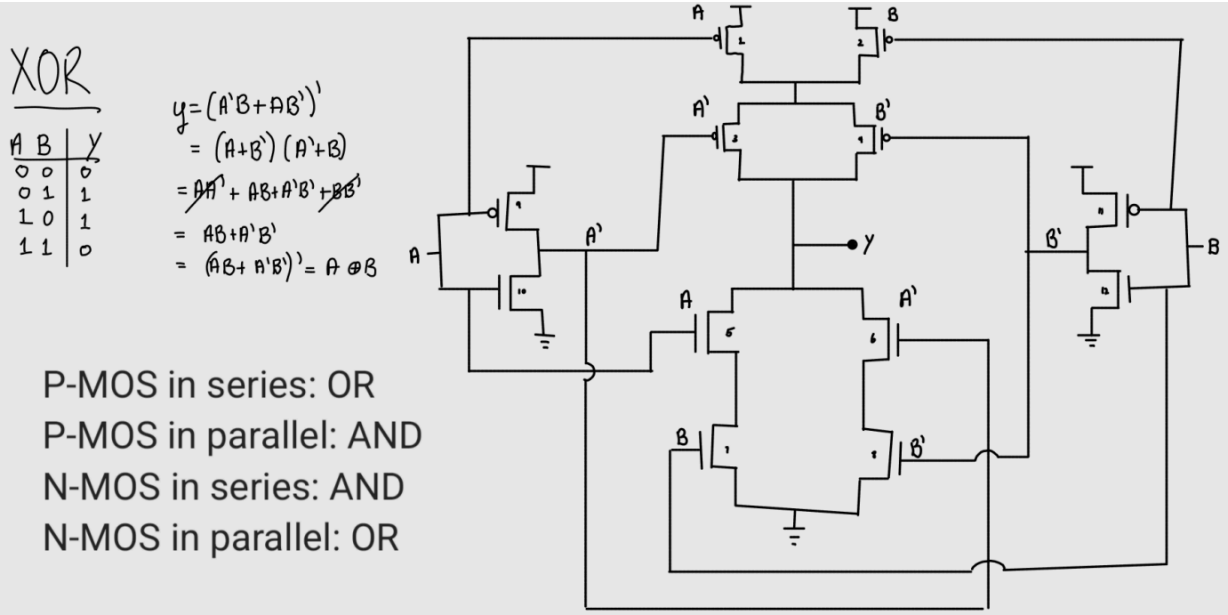

Figure 1: Circuit Schematic and Validation

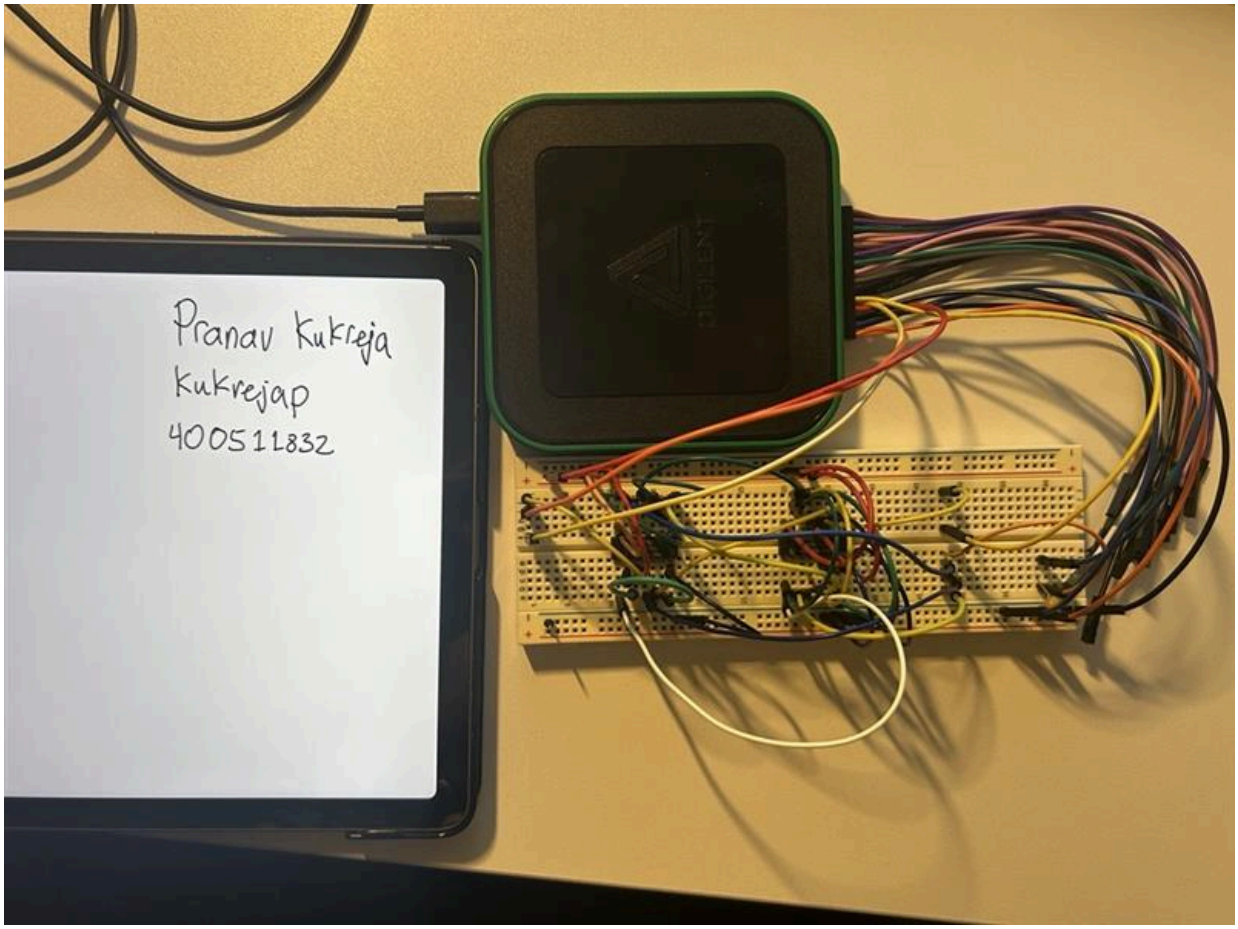

Figure 2: XOR Gate Circuit Implementation

Ideal Sizing

In an ideal XOR gate design, transistor sizing is crucial for balanced performance. Typically, n-type MOSFETs are sized with a 2:1 ratio, while p-type MOSFETs use a 5:1 ratio to compensate for their lower conductivity. This leads to an overall p-type to n-type ratio of 5:2 across the gate. In our implementation, we use two CD4007B ICs that provide six n-type and six p-type transistors, which match the required layout for an XOR gate. Although the CD4007B does not allow for custom transistor sizing, its n-type and p-type devices are fairly well-matched in terms of performance. Because we can match the ideal number of transistors, our circuit approximates the desired sizing ratio quite well. This enables us to accurately implement XOR functionality, even if slight differences in switching characteristics may introduce minor variations in timing.

Functional Testing

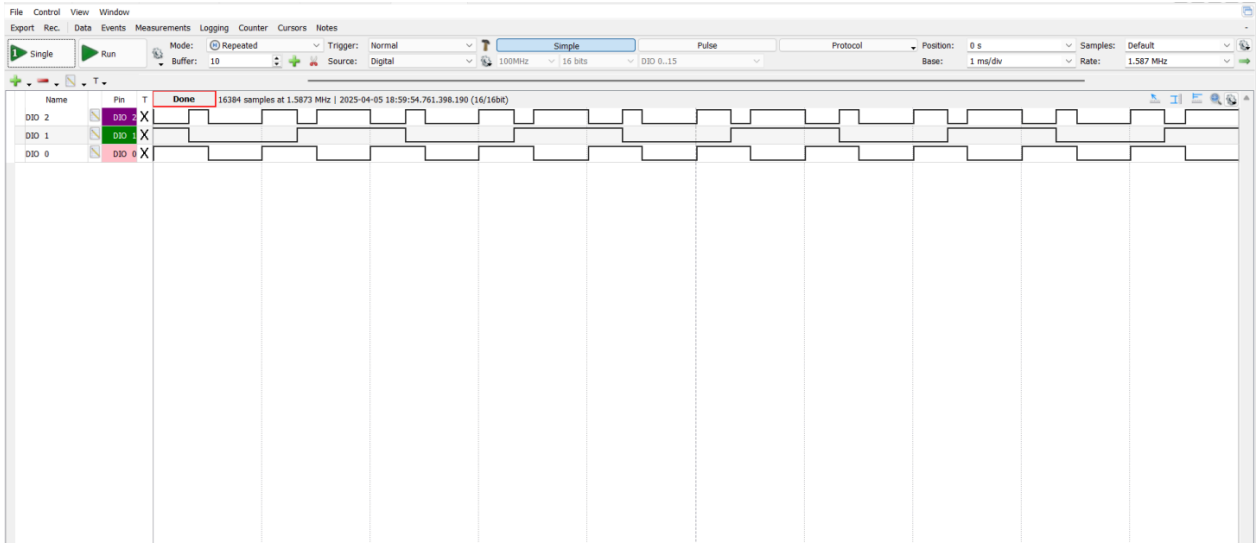

Figure 3: Logic Analyzer Timing Diagram: diode 2 (purple) is output, diode 1 (green) is A, and diode 0 (pink) is B

We verified the functionality of the XOR gate using the digital I/O pins on the AD3. Inputs DIO0 and DIO1 were driven by the wave generator to cycle through all possible input states: 00, 01, 10, and 11. The output, monitored on DIO2, produced a high logic level for input combinations 01 and 10, and remained low for 00 and 11. This output pattern aligns perfectly with the standard XOR truth table shown in Figure 1, confirming that our transistor-based design operates correctly.

Static Level Testing

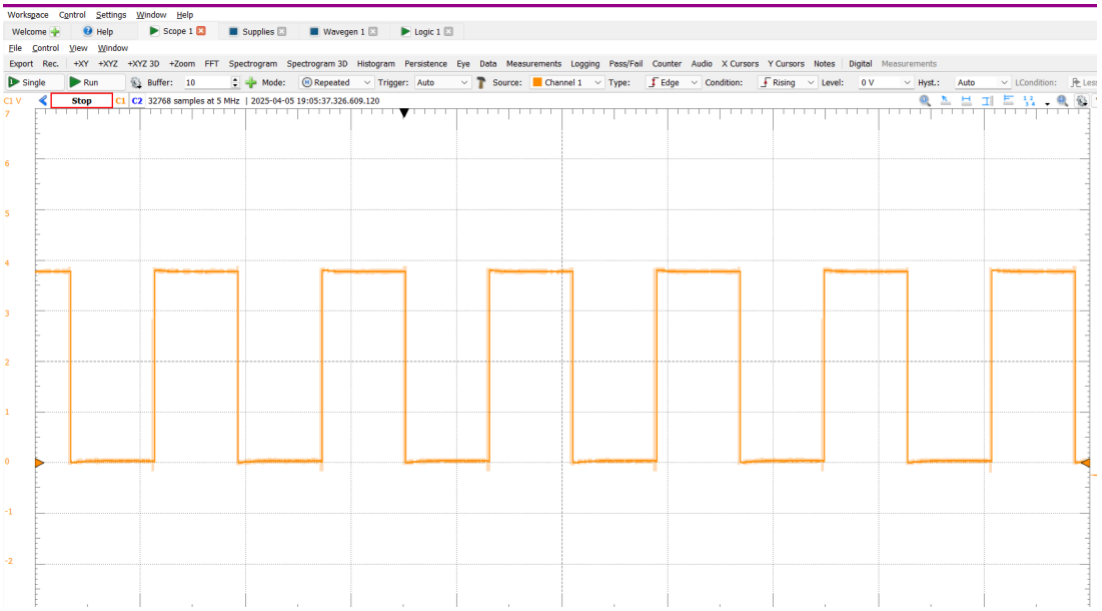

Figure 4: AD3 oscilloscope results for first input as logic-1 and second input as a square wave

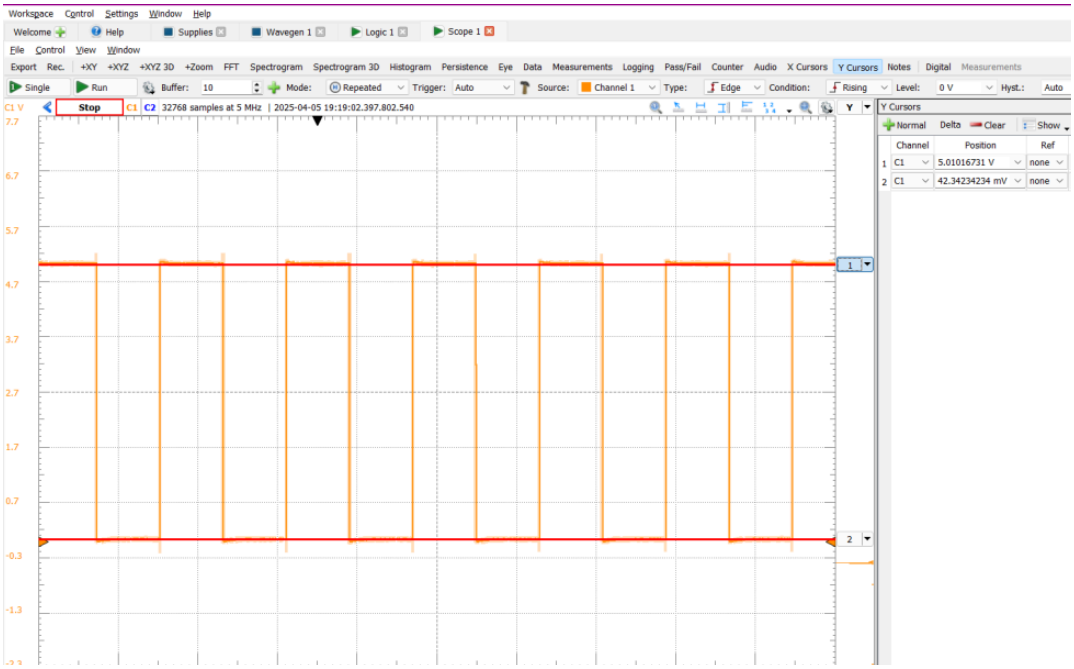

Figure 5: Static Level Testing Waveform with Cursors

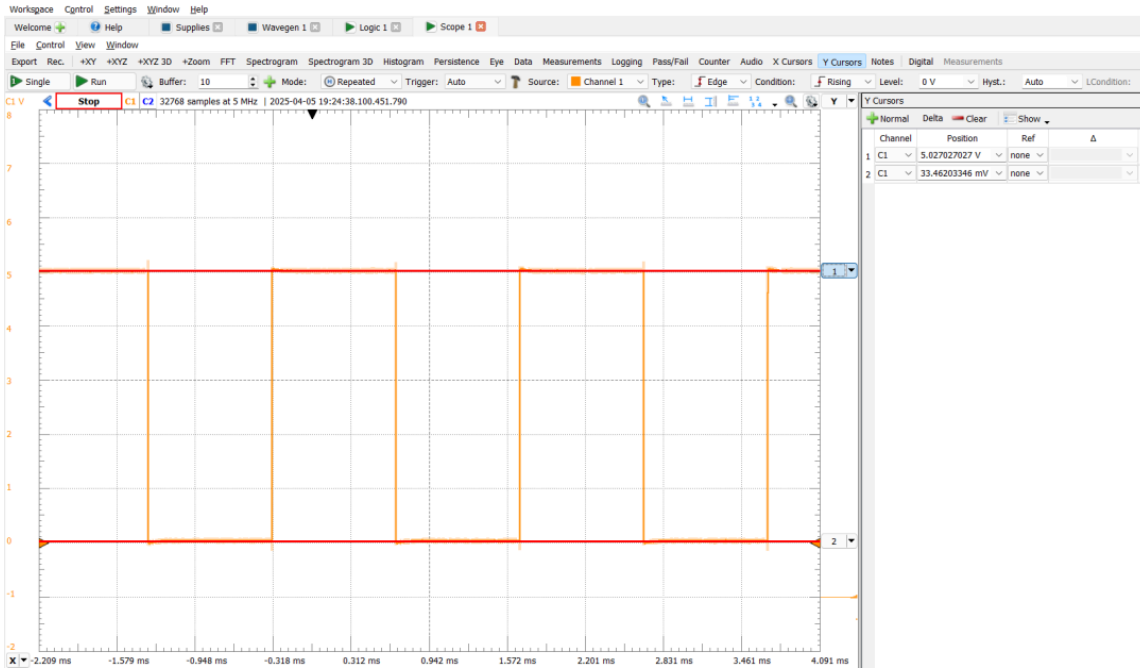

Figure 6: Waveform after swapping logic-1 and square wave inputs

To characterize the logic levels, one input was held at a constant high (5V) while the other received a square wave signal. Under this setup, the output reached a high voltage (VH) of 5.010 V and a low voltage (VL) of 42.34 mV, as shown in Figure 5. These values represent the peak and trough of the output waveform and serve as the baseline logic levels for the circuit.

When the inputs were swapped, the output measured a VH of 5.0270 V and a VL of 33.462 mV, as shown in Figure 6. While both sets of measurements are close, there is still a slight variation, particularly in the VL values. However, the differences are minimal and do not impact the overall logic behavior of the circuit.

Timing

To determine the rise and fall times of the output signal, we measured the duration it takes for the voltage to transition between 10% and 90% of its actual range. Specifically, the rise time corresponds to the interval during which the output voltage increases from 10% to 90% of its observed maximum, while the fall time captures the reverse, when the voltage decreases from 90% down to 10%. These thresholds are calculated based on the measured high and low voltage levels from the waveform. This approach yields a more accurate representation of the circuit's real-world switching performance.

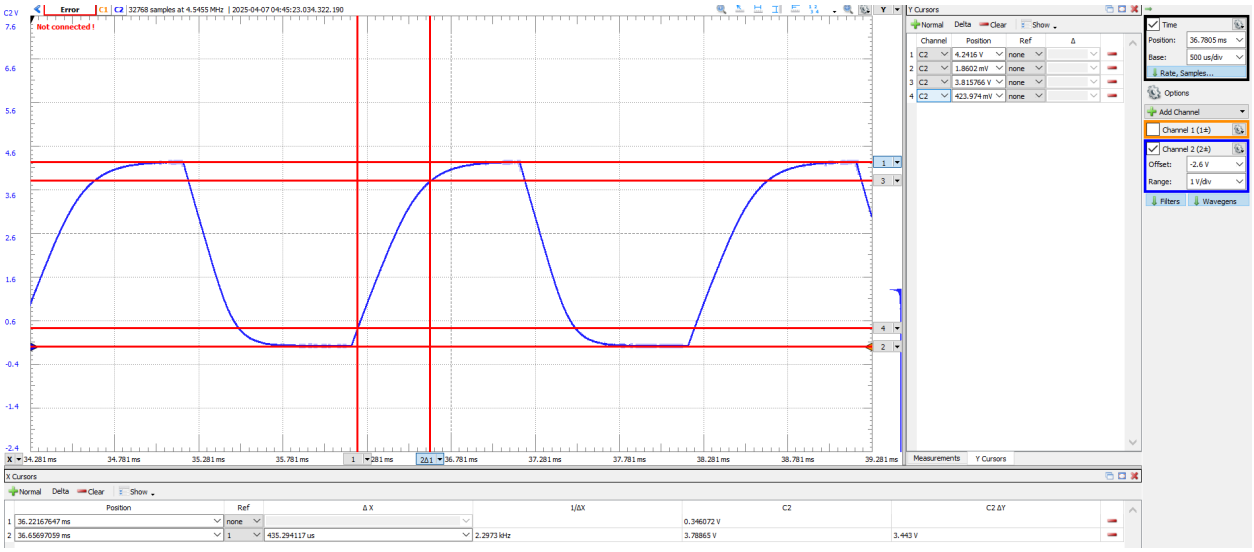

Figure 7: Measuring rise time with capacitor as load

Figure 7 shows the output waveform, where the minimum and maximum voltages were measured at 1.8602 mV and 4.2416 V, respectively, thus allowing us to calculate a voltage swing of 4.2397 V. From this, the 10% and 90% thresholds were calculated to be 0.424 V and 3.8157 V. By placing the oscilloscope cursors at these two points during the rising edge of the waveform, the time it took to transition between them was found to be 435.29 µs. This rise time reflects the effect of the 100 nF capacitor connected to the output, which introduces a noticeable delay.

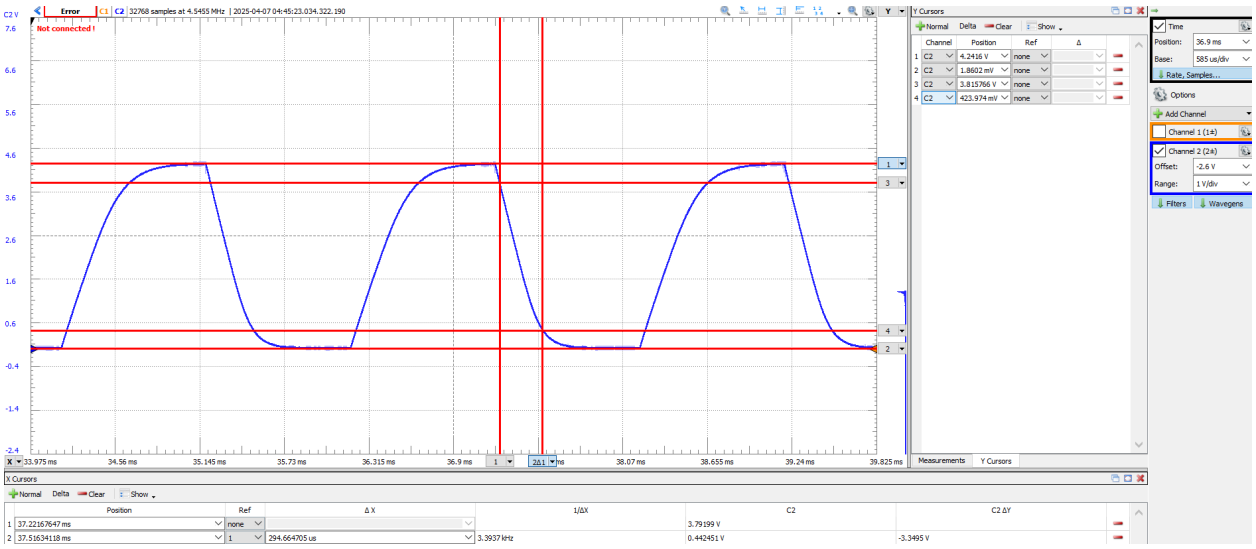

Figure 8: Measuring fall time with capacitor as load

In Figure 8, the output voltage swing remained at 4.2397 V, with the same 10% and 90% threshold levels. During the falling edge of the waveform, the time it took for the output to drop between these two points was measured using oscilloscope cursors and found to be 294.665 µs. This timing reflects the capacitor's discharge behavior, as the 100 nF capacitor at the output influences how quickly the voltage decreases.

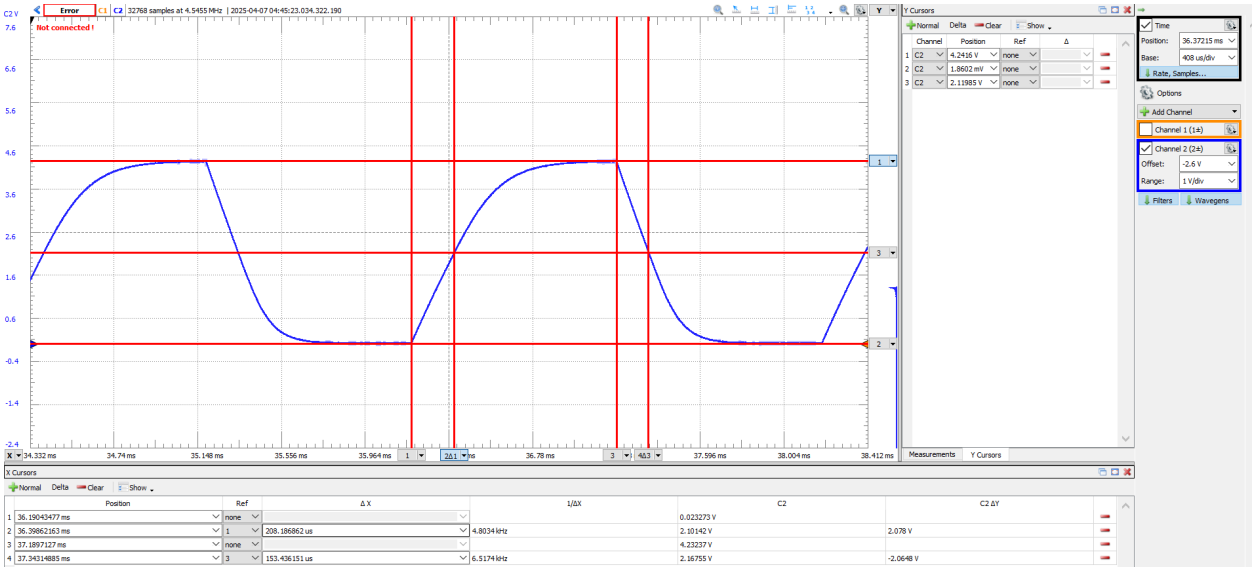

Figure 9: Measuring T_{PLH} and T_{PHL} with capacitor as load

Propagation delay was determined by measuring the time difference between the input and output signals as they crossed the 50% voltage level, which is the midpoint of the output swing, as shown in Figure 9. Based on the previously calculated voltage swing, the midpoint was calculated to be around 2.120 V. For the rising transition, the delay from the input rising edge to the output reaching this midpoint was 208.19

μs, representing τPLH. On the falling edge, the delay from the input falling to the output crossing the midpoint downward was 153.44 μs, representing τPHL. Using these values, the average propagation delay τP was calculated.

$$\tau P = \frac{\tau PLH + \tau PHL}{2} = \frac{208.19\ \mu s + 153.44\ \mu s}{2} = 180.82\ \mu s$$

This average provides a general measure of how quickly the XOR circuit responds to input changes.

References

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic Circuits, 8th ed. New York, NY, USA: Oxford Univ. Press, 2019. [Accessed Mar. 6, 2025]

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[3] National Semiconductor Corporation, “MOS Data Sheets - CD4007M/CD4007C Dual Complementary Pair Plus Inverter.” National Semiconductor, Feb. 1988. [Accessed Mar. 6, 2025]