COURSE AND EVALUATION PLAN

1. Course code	: **EC206**	2. Course title	: **Microprocessors**
3. L-T-P	: **3-1-0**	4 Credits	: **4**
5. Teaching department	: **E&C**	6. Course instructor	**: Dr. Aparna P.**

7. Pre-requisites : **-Nil-**

8. **Course Objectives**:

i. To introduce the stored program concept, computer organization, specifications of an Instruction Set Architecture.
ii. To introduce the ARM processor programmers model and the concept of assembly level program.
iii. To explain the functioning of processor, the processor modes and exceptions.
iv. To introduce the concept of interfacing the processor to peripherals.

9. **Course outcomes**: On completion of this course the student will

i. Have an insight to the stored program concept, computer organization, specifications of an Instruction Set Architecture.
ii. Know the family of ARM processors, the organization of a typical ARM processor.
iii. Be able to analyze and write assembly language programs for ARM processors.
iv. Understand the interrupts and exception handling in ARM processors.

10. **Course Coverage** (50 – Lecture schedule):

Module	**Contents**	**Lectures**
Introduction to Microprocessors	♦ Introduction to computer organization ♦ CISC, RISC, Concept of pipelining ♦ Evolution of Microprocessors.	L1-L4
Introduction to ARM processor	♦ ARM overview, Programming Model ♦ Processor and memory organization, concept of stack.	L5-L8
ARM Instruction set	♦ Data-processing Instructions ♦ Data Transfer Instructions, Control Instructions, Additional special instructions ♦ Addressing modes & Instruction Encoding	L9-L20
Self Study: HLL for ARM	♦ Architectural support for High-level languages	L20-L26
ARM Implementation, organization and execution.	♦ The data flow model for Data-processing Instructions, Data Transfer Instructions, Control Instructions ♦ ARM Instruction Datapath Timing	L27-L37

	♦ The 3-stage pipe line organization, pipeline hazards, PC behavior	
ARM Processor Modes and Exceptions.	♦ Seven Processor Modes in Detail ♦ Exception Types, vector table, exception Handling, Priority	L38-L44
Introduction to 16 bit Thumb instruction set (TIS**)**	♦ Need for TIS ♦ Thumb implementation and its encoding	L45-L46
ARM interfacing to peripherals	♦ Interfacing ARM to GPIO, UART, DAC	L47-L-50

11. **Reference Books:**
    1. "Assembly Language Programming ARM Cortex-M3" by Vincent Mahout, ISTE Ltd and John Wiley & Sons, Inc
    2. `https://www.arm.com/products/silicon-ip-cpu/cortex-m/cortex-m3`

12. **Evaluation Scheme :**
    I. Mid semester Exam : 25%
    II. Quizzes : 35%
    III. End semester Exam : 40%

Prepared By:

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Approved By

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